SPECIFICATIONS FOR
LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPEX PART NO.	**AM-320240LNTMQW00H-A**
APPROVED BY	
DATE	

APPROVED BY	CHECKED BY	ORGANIZED BY

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RECORD OF REVISION

Revision Date	Page	Contents	Editor
2016/1/18	-	New Release	Kokai
2016/3/23		Rename to AM320240LNTMQW00H. Update Outline dimension drawing	Kokai
2016/10/17		Modify Protect tape dimension.	Kokai
2017/5/16		Base on AM320240LNTMQW00H, add FPC golden finger design. Rename to AM320240LNTMQW00H-A. 	Kokai
2017/6/12		Add Packing drawing.	Kokai
2017/6/14		Add EPE Protect sheet (Anti-static)	Kokai
2017/8/17	22,23	Add FPC Au and Ni thickness. Update the drawing.	Kokai
2018/12/6		Modify LED back-light data.	Kokai

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1 Features

3.5 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) module. This module is composed of a 3.5” TFT-LCD panel, a driver circuit and backlight unit.

1.1 Construction: 3.5” a-Si color TFT-LCD, White LED Backlight.
1.2 Resolution (pixel): 320(R.G.B) X240.
1.3 Number of the Colors: 16.7M Dithering (R, G, B 8 bit digital each).
1.4 LCD type: Transmissive Color TFT LCD (normally White).
1.5 View Angle: 6 o’clock.
1.6 24Bit RGB Interface.
1.7 Interface: 54 pin.
1.8 Power Supply Voltage: 3.3V single power input. Built-in power supply circuit.

2 Physical specifications

Item	Specifications	Unit
Panel Size	3.5”	Inch
Display resolution(dot)	320 (W) x 240(H)	dot
Active area	70.08(W) x 52.56(H)	mm
Pixel pitch	0.219×0.219	Mm
Outline Dimension	79.9(W) ×68.9(H) ×3.15(T)	Mm
Number of colors	16M	
Viewing Direction	6 o’clock (Gray Inversion)	
Color Pixel Arrangement	RGB Vertical Stripe	
Luminance	400	Cd/m^2
Contrast Ratio	500	
LCD Surface Treatment	Anti-Glare	
Interface	24 bits parallel bus	
Back Light	White LED	
Operation Temperature	-20~70	℃
Storage Temperature	-30~80	℃
Driver IC	HX8238-D	
Weight	T.B.D	g

3 Electrical specification

3.1 Absolute max. ratings

Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power voltage	VDD	VSS-0.3	-	5.0	V	
Logic Input Signal Voltage	Vi	-0.3	--	VDD+0.3		
Back Light Forward Current	I_{LED}			25	mA	For each LED

3.2 DC Electrical specification

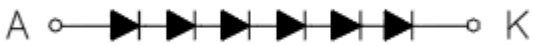
(GND=0V,Ta=25℃)

Item		Symbol	Values			Unit	Remark
			Min.	Typ.	Max.		
Power Supply Voltage		VDD	3.0	3.3	3.6	V	
Input Signal Voltage	Low Level	VIH	0	--	0.2*VDD		
	High Level	VIL	0.8*VDD	--	VDD		
Operatin mode Current		I_{DP}	-	10	12	mA	VDD=3.3V

3.3 LED back-light Unit Absolute max. ratings

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I_{LED}		20		mA	6LEDs
Forward Voltage	VF	16.2	18.0	19.2	V	IF=20mA
Reverse Current	IR			10	uA	VR=5V,1LED
Luminous Tolerance	IV-M	70	75		%	(MIV/MAX)×100
Peak forward Current	Ifp		60		mA	1LED
Reverse Voltage	VR		5		V	1LED
LED Lifetime	-	20000			Hr	

3.4 Internal Circuit Diagram



CURRENT IF=20mA

3.3 Interface specifications

No.	Symbol	I/O	Function	Remark
1	LED_Cathod	P	LED_Cathode	
2	LED_Cathod	P	LED_Cathode	
3	LED_Anode	P	LED_Anode	
4	LED_Anode	P	LED_Anode	
5	GND	-	Ground	
6	RESET	-	Reset Signal input. Active Low	
7	NC	-	No Connect	
8	NC	-	No Connect	
9	NC	-	No Connect	
10	NC	-	No Connect	
11	NC	-	No Connect	
12	D00	I	**Blue Data Bit 0**	
13	D01	I	**Blue Data Bit 1**	
14	D02	I	**Blue Data Bit 2**	
15	D03	I	**Blue Data Bit 3**	
16	D04	I	**Blue Data Bit 4**	
17	D05	I	**Blue Data Bit 5**	
18	D06	I	**Blue Data Bit 6**	
19	D07	I	**Blue Data Bit 7**	
20	D08	I	**Green Data Bit 0**	
21	D09	I	**Green Data Bit 1**	
22	D10	I	**Green Data Bit 2**	
23	D11	I	**Green Data Bit 3**	
24	D12	I	**Green Data Bit 4**	
25	D13	I	**Green Data Bit 5**	
26	D14	I	**Green Data Bit 6**	
27	D15	I	**Green Data Bit 7**	
28	D16	I	**Red Data Bit 0**	
29	D17	I	**Red Data Bit 1**	
30	D18	I	**Red Data Bit 2**	
31	D19	I	**Red Data Bit 3**	
32	D20	I	**Red Data Bit 4**	

No.	Symbol	I/O	Function	Remark
33	D21	I	**Red Data Bit 5**	
34	D22	I	**Red Data Bit 6**	
35	D23	I	**Red Data Bit 7**	
36	HSYNC	I	Horizontal Synchronous Signal	
37	VSYNC	I	Vertical Synchronous Signal	
38	CLK	I	Data Clock	
39	NC	-	No Connect	
40	NC	-	No Connect	
41	VDD	P	power supply（3.3V）	
42	VDD	P	power supply（3.3V）	
43	SPENA	I	Serial port data enable signal	
44	GND	P	Ground	
45	NC	-	No Connect	
46	GND	P	Ground	
47	NC	-	No Connect	
48	NC	-	No Connect	
49	SPCK	I	SPI Serial Clock	
50	SPDA	I/O	SPI Serial Data Input/output	
51	NC	-	No Connect	
52	DEN	I	Data enabling signal	
53	GND	P	Ground	
54	GND	P	Ground	

Note1: I/O definition:

I----Input O----Output P----Power/Ground

4. Input Signal Timing

4.1 AC Timing characteristic

(VDD=3.3V, GND=0V, TA=25℃)

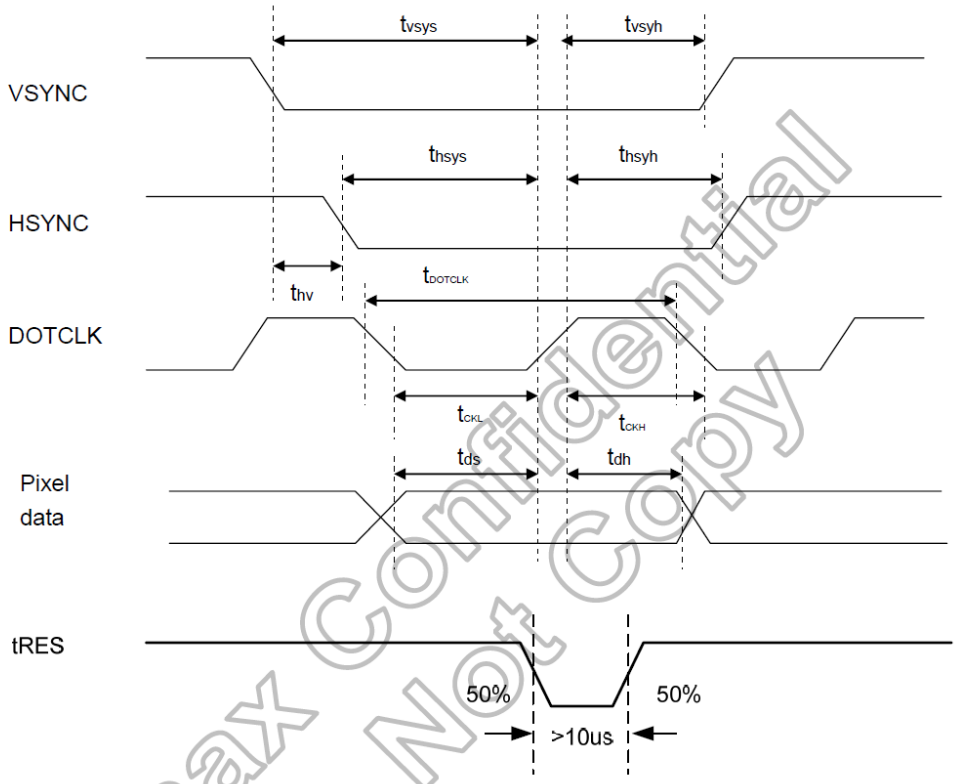


Figure 12. 1: Pixel timing

Characteristics	Symbol	Min.		Typ.		Max.		Unit
		24-bit	8-bit	24- bit	8-bit	24-bit	8-bit	
DOTCLK Frequency	fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Vertical Sync Setup Time	tvsys	20	10	-	-	-	-	ns
Vertical Sync Hold Time	tvsyh	20	10	-	-	-	-	ns
Horizontal Sync Setup Time	thsys	20	10	-	-	-	-	ns
Horizontal Sync Hold Time	thsyh	20	10	-	-	-	-	ns
Phase difference of Sync Signal Falling Edge	thv	1		-		240		tDOTCLK
DOTCLK Low Period	tCKL	50	15	-	-	-	-	ns
DOTCLK High Period	tCKH	50	15	-	-	-	-	ns
Data Setup Time	tds	12	10	-	-	-	-	ns
Data hold Time	tdh	12	10	-	-	-	-	ns
Reset pulse width	tRES	10		-		-		µs

Note: External clock source must be provided to DOTCLK pin of HX8238-D. The driver will not operate if absent of the clocking signal.

4.2 24 bit RGB mode for 320RGB x 240 (Sync Mode)

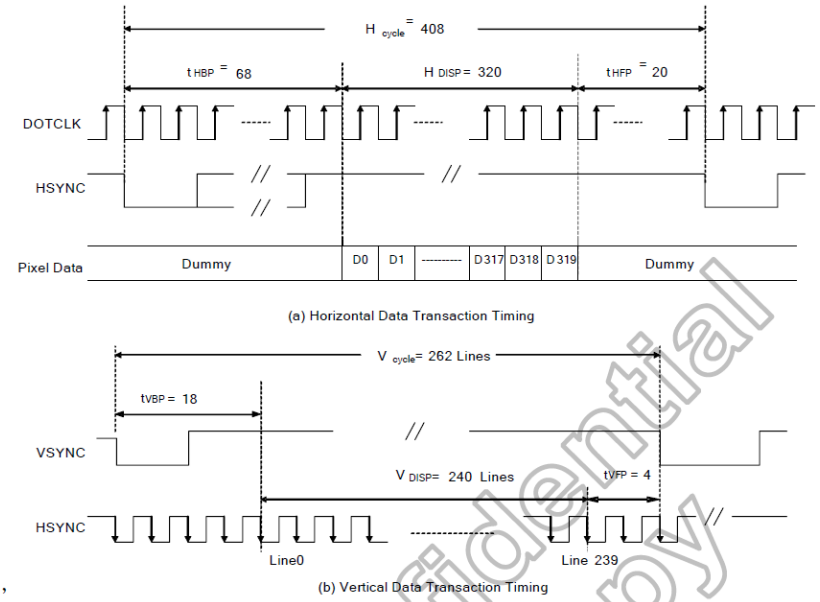


Figure 12. 2: Data transaction timing in parallel RGB (24-bit) interface (SYNC mode)

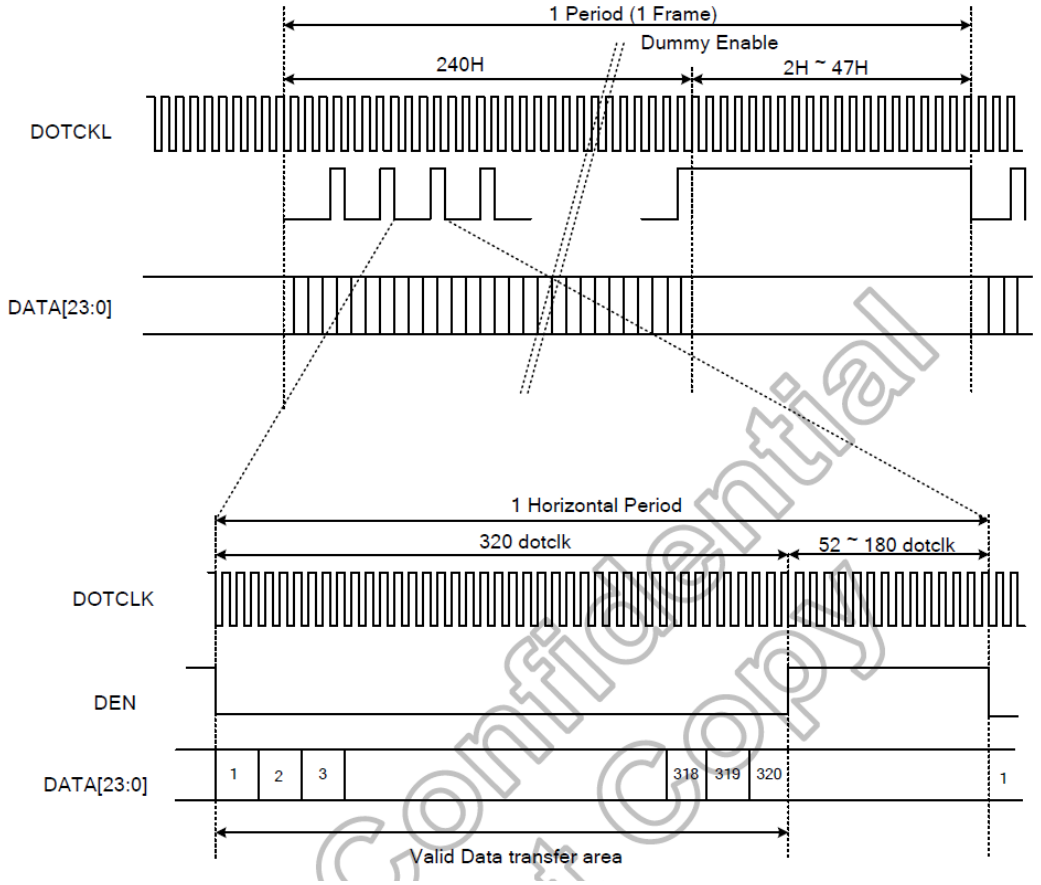
Characteristics		Symbol	Min.		Typ.		Max.		Unit
			24-bit	8-bit	24- bit	8-bit	24-bit	8-bit	
DOTCLK Frequency		fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period		tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Frequency (Line)		fH	-		14.9		22.35		KHz
Vertical Frequency (Refresh)		fV	-		60		90		Hz
Horizontal Back Porch		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Front Porch		tHFP	-	-	20	60	-	-	tDOTCLK
Horizontal Data Start Point		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Blanking Period		tHBP + tHFP	52	146	88	264	180	960	tDOTCLK
Horizontal Display Area		HDISP	-	-	320	960	-	-	tDOTCLK
Horizontal Cycle		Hcycle	372	1106	408	1224	500	1920	tDOTCLK
Vertical Back Porch		tVBP	-		18		-		Lines
Vertical Front Porch		tVFP	-		4		-		Lines
Vertical Data Start Point		tVBP	-		18		-		Lines
Vertical Blanking Period	NTSC	tVBP + tVFP	10		22		47		Lines
	PAL		20		33		120		
	PAL		12		25		112		
Vertical Display Area	NTSC	VDISP	-		240		-		Lines
	PAL				280(PALM=0)				
	PAL				288(PALM=1)				
Vertical Cycle	NTSC	Vcycle	250		262		287		Lines
	PAL		300		313		400		

Table 12. 2: Data transaction timing in normal operating mode

4.3 24 bit RGB mode for 320RGB x 240 (DE only Mode)

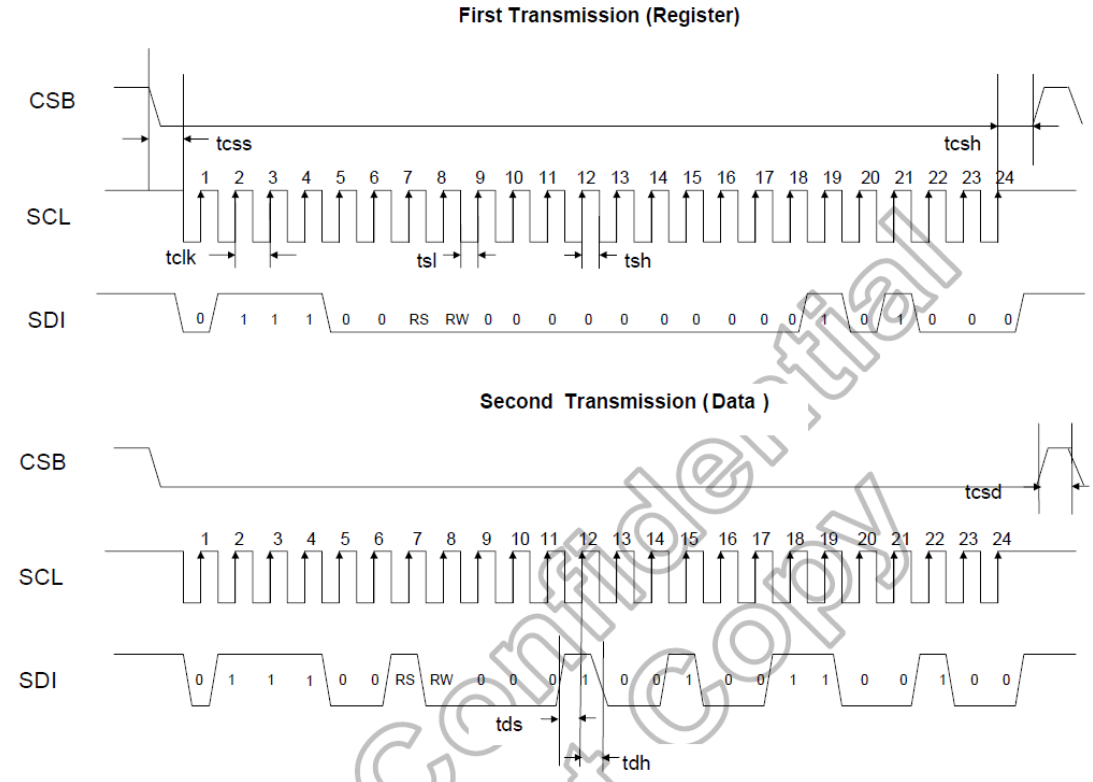
Characteristics	Symbol	Min.		Typ.		Max.		Unit
		24-bit	8-bit	24- bit	8-bit	24-bit	8-bit	
DOTCLK Frequency	fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Blanking Period	tHBP + tHFP	52	146	88	264	180	960	tDOTCLK
Horizontal Display Area	HDISP	-	-	320	960	-	-	tDOTCLK
Horizontal Cycle	Hcycle	372	1106	408	1224	500	1920	tDOTCLK
Vertical Blanking Period	tVBP + tVFP	2		-		47		Lines
Vertical Display Area	VDISP	-		240		-		Lines
Vertical Cycle	Vcycle	242		-		287		Lines

Table 12. 3: Data transaction timing in DE only operating mode



4.4 3-wire serial communication AC timing

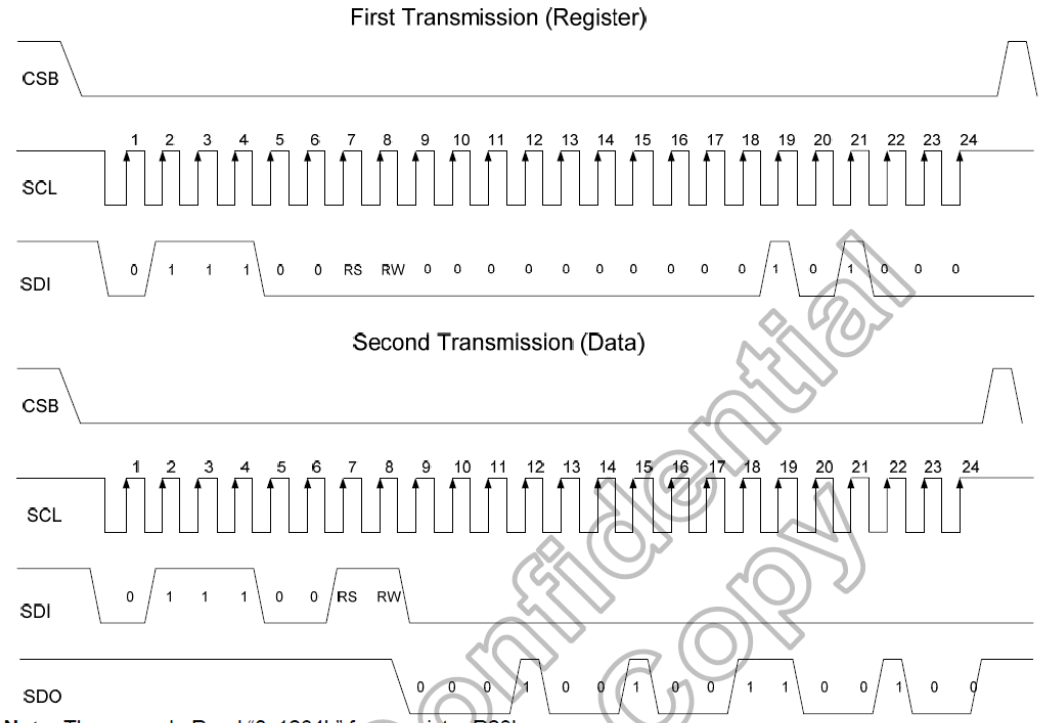
- Write SPI



Note: The example writes "0x1264h" to register R28h.
SPID connected to VSS.

Figure 12. 14: (a) SPI interface timing diagram & write SPI example

- Read SPI



Note: The example Read "0x1264h" from register R28h.

Figure 12. 15: (b) SPI interface timing diagram & read SPI example

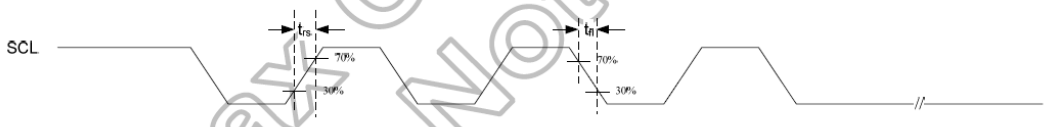


Figure 12. 16: Rising/Falling time

Characteristics	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Serial Clock Frequency	fclk	-	-	20	MHz
Serial Clock Cycle Time	tclk	50	-	-	ns
Clock Low Width	tsl	25	-	-	ns
Clock High Width	tsh	25	-	-	ns
Clock Rising Time	trs	-	-	30	ns
Clock Falling Time	tfl	-	-	30	ns
Chip Select Hold Time	tcsh	10	-	-	ns
Chip Select High Delay Time	tcsd	20	-	-	ns
Data Setup Time	tds	5	-	-	ns
Data Hold Time	tdh	10	-	-	ns

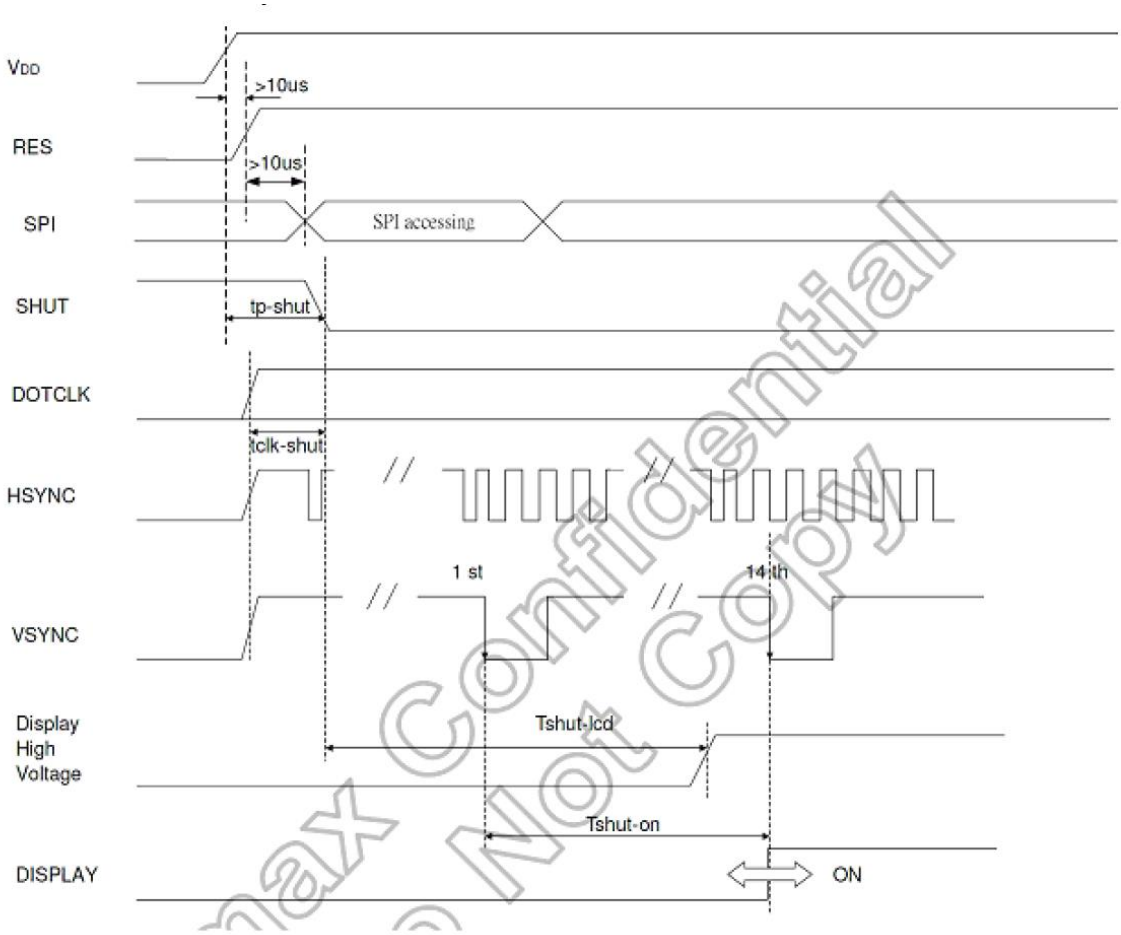
Table 12. 6: SPI timing

4.5 3-wire Control Registers List

Reg#	Register	R/W	R/S	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
SR	Status Read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0
R01h	Driver output control	0	1	0	RL	REV	PINV	BGR	SM	TB	CPE	0	0	0	0	0	0	0	0
R02h	LCD driver AC control	0	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BTF	BT2	BT1	BT0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
R04h	Data and color filter control	0	1	0	0	0	0	0	PALM	BLT1	BLT0	OEA1	OEA0	SEL2	SEL1	SEL0	SWD2	SWD1	SWD0
R05h	Function control	0	1	GHN	XDK	GDIS	LPF	DEP	CKP	VSP	HSP	DEO	DIT	0	PWM	0	FB2	FB1	FB0
R06h	Reserved	Reserved																	
R08h	LED control	0	1	0	0	0	PWMS	PWMF3	PWMF2	PWMF1	PWMF0	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0
R0Ah	Contrast/ Brightness control	0	1	0	BR6	BR5	BR4	BR3	BR2	BR1	BR0	0	0	0	CON4	CON3	CON2	CON1	CON0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	0	EQ2	EQ1	EQ0	0	0	0	0	0	0	0	0
R0Dh	Power control (2)	0	1	0	VRC2	VRC1	VRC0	0	0	VDS1	VDS0	0	0	VRH5	VRH4	VRH3	VRH2	VRH1	VRH0
R0Eh	Power control (3)	0	1	0	0	1	VDV6	VDV5	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0
R0Fh	Gate scan starting Position	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
R16h	Horizontal Porch	0	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	0	0	0	0	0	0
R17h	Vertical Porch	0	1	STH1	STH0	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
R1Eh	Power control (4)	0	1	0	0	0	0	0	0	0	0	nOTP	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
R27h	Reserved	Reserved																	
R28h	Reserved	Reserved																	
R29h	Reserved	Reserved																	
R2Bh	Reserved	Reserved																	
R30h	γ control (1)	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31h	γ control (2)	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32h	γ control (3)	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33h	γ control (4)	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34h	γ control (5)	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35h	γ control (6)	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36h	γ control (7)	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37h	γ control (8)	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R3Ah	γ control (9)	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3Bh	γ control (10)	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

Note: * means don't care
Software settings will override hardware pin (eg, BGR bits override BGR pin definition)

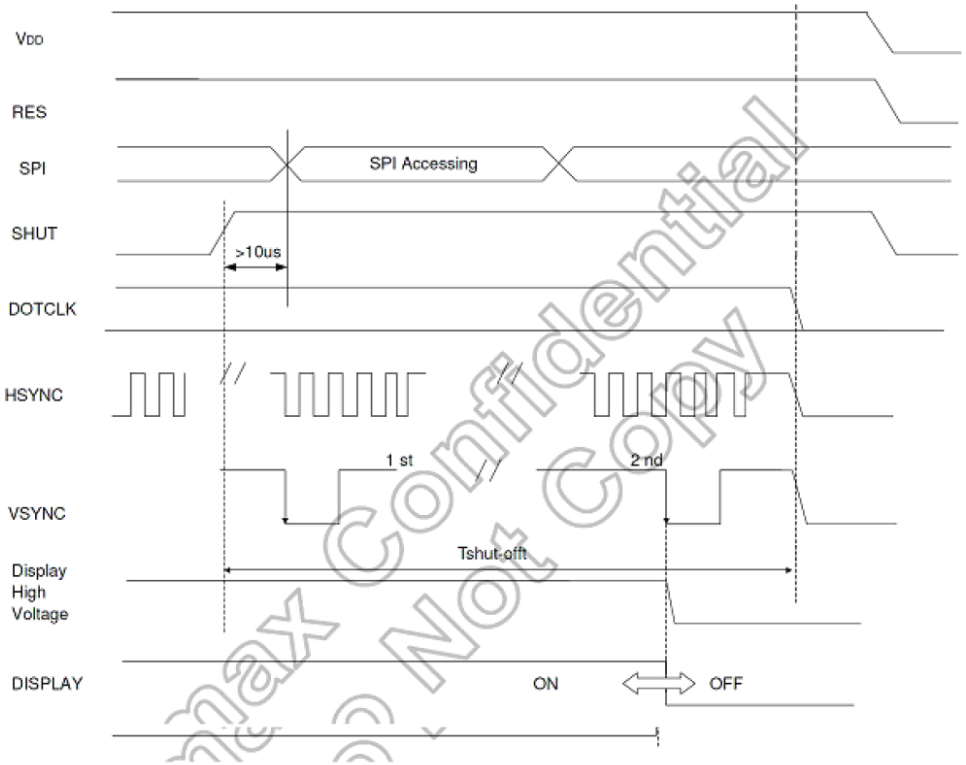
4.6 Power on sequence



Characteristics	Symbol	Min	Typ	Max	Units
VDDD / VDDIO on to falling edge of SHUT	tp-shut	1	-	-	us
DOTCLK	tclk-shut	1	-	-	clk
Falling edge of SHUT to LCD power on	tshut-lcd	-	-	128	ms
Falling edge of SHUT to display start - 1 line: 408 clk - 1 frame: 262 line -DOTCLK = 6.5MHz	tshut-on	-	-	14	frame
		-	166	232.4	ms

Note: It is necessary to input DOTCLK before the falling edge of SHUT.
Display starts at 10th falling edge of VSTNC after the falling edge of SHUT.

4.7 Power off sequence



Characteristics	Symbol	Min	Typ	Max	Unit
Rising edge of SHUT to display off - 1 line: 408 clk - 1 frame: 262 line - DOTCLK = 6.5MHz	tshut-off	2	-	-	frame
		33.4	-	-	ms
Input-signal-off to VDDD / VDDIO off	toff-vdd	1	-	-	us

Note: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.
Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.
If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

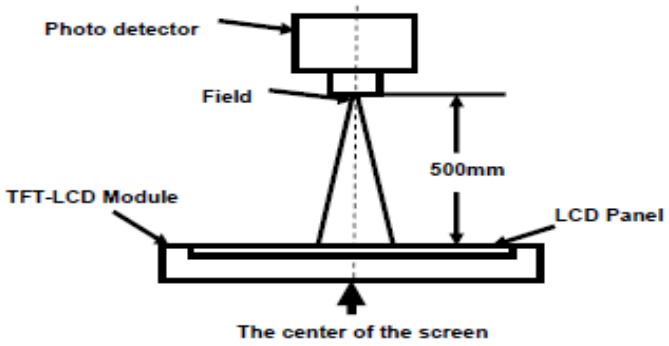
5 Optical Characteristic

Ta = 25℃

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ=0°	400	500			Note3
Brightness		B		350	400		cd/m2	
Chromaticity	White	X	θ=0° Φ=0	0.26	0.31	0.36		Measured by C light.
		Y		0.27	0.32	0.37		
	Red	X		0.56	0.61	0.66		
		Y		0.31	0.36	0.41		
	Green	X		0.30	0.35	0.40		
		Y		0.53	0.58	0.63		
	Blue	X		0.10	0.15	0.20		
		Y		0.02	0.07	0.12		
View Angles		θT	CR≧10	40	50		Degree	Note2 With EWV Polarizer
		θB		60	70			
		θL		60	70			
		θR		60	70			
Uniformity				70			%	
NTSC					57.6		%	Note5

Note1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical propertiesare measured at the center point of the LCD screen. All input terminals LCD panel must be groundwhen measuring the center area of the panel.



Note2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

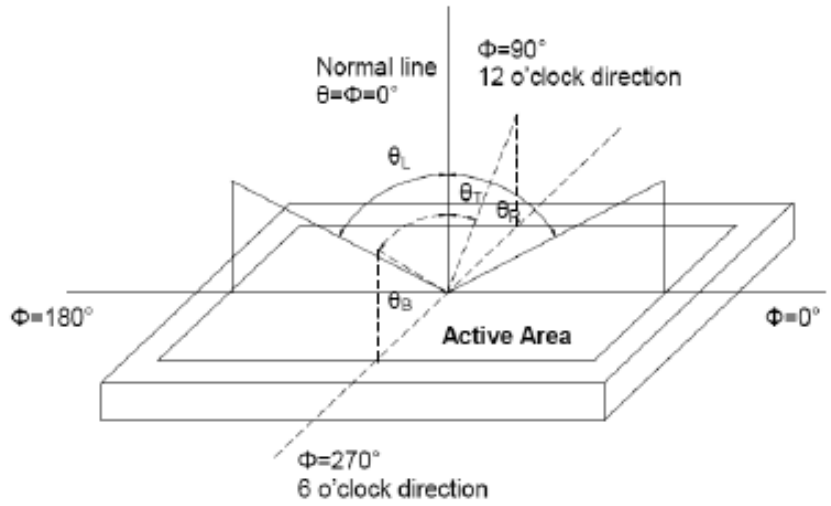


Fig. 6-1 Definition of

viewing angle Note3: Definition of contrast ratio:

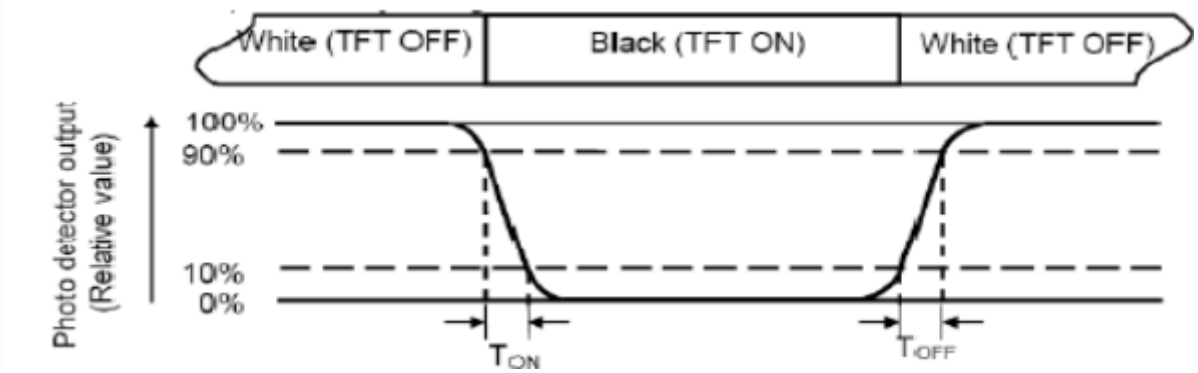
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

"White state ":The state is that the LCD is driven by Vwhite. "Black state": The state is that the LCD is driven by Vblack.

Vwhite: To be determined Vblack: To be

determined. Note4: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" stateand "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90%to 10%. And fall time (TOFF) is the time between photo detector



output intensity changed from 10% to90%.

Note5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD

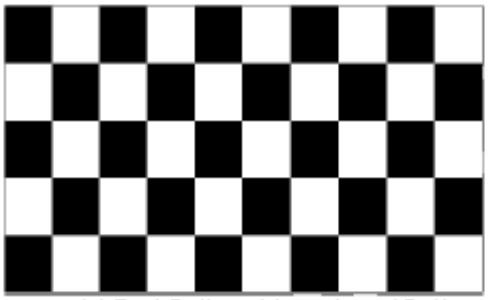
6 QUALITY ASSURANCE SYSTEM

6.1 TEMPERATURE AND HUMIDITY

Test items	Conditions	
High Temperature Storage	Ta=80℃,240hrs	
Low Temperature Storage	Ta=-30℃, 240hrs	
High Temperature Operation	Ta=70℃,240hrs	
Low Temperature Operation	Ta=-20℃,240hrs	
High Temperature High Humidity Operation	Ta=60℃, 90%RH,240hrs(no condensation)	
Thermal Shock	-20℃(0.5hr)~70℃(0.5hr)100 cycles	
Image Sticking	25℃; 4hrs	Note1

Note1:Condition of image sticking test :25℃±2℃

Operation with test pattern sustained for 4hrs,then change to gray pattern immediately.after5 mins,themura must be disappeared completely



(a) Test Pattern (chess board Pattern)

(b) Gray Pattern

7 USE PRECAUTIONS

7.1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

7.2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

7.3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or

fluorescent light.

3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

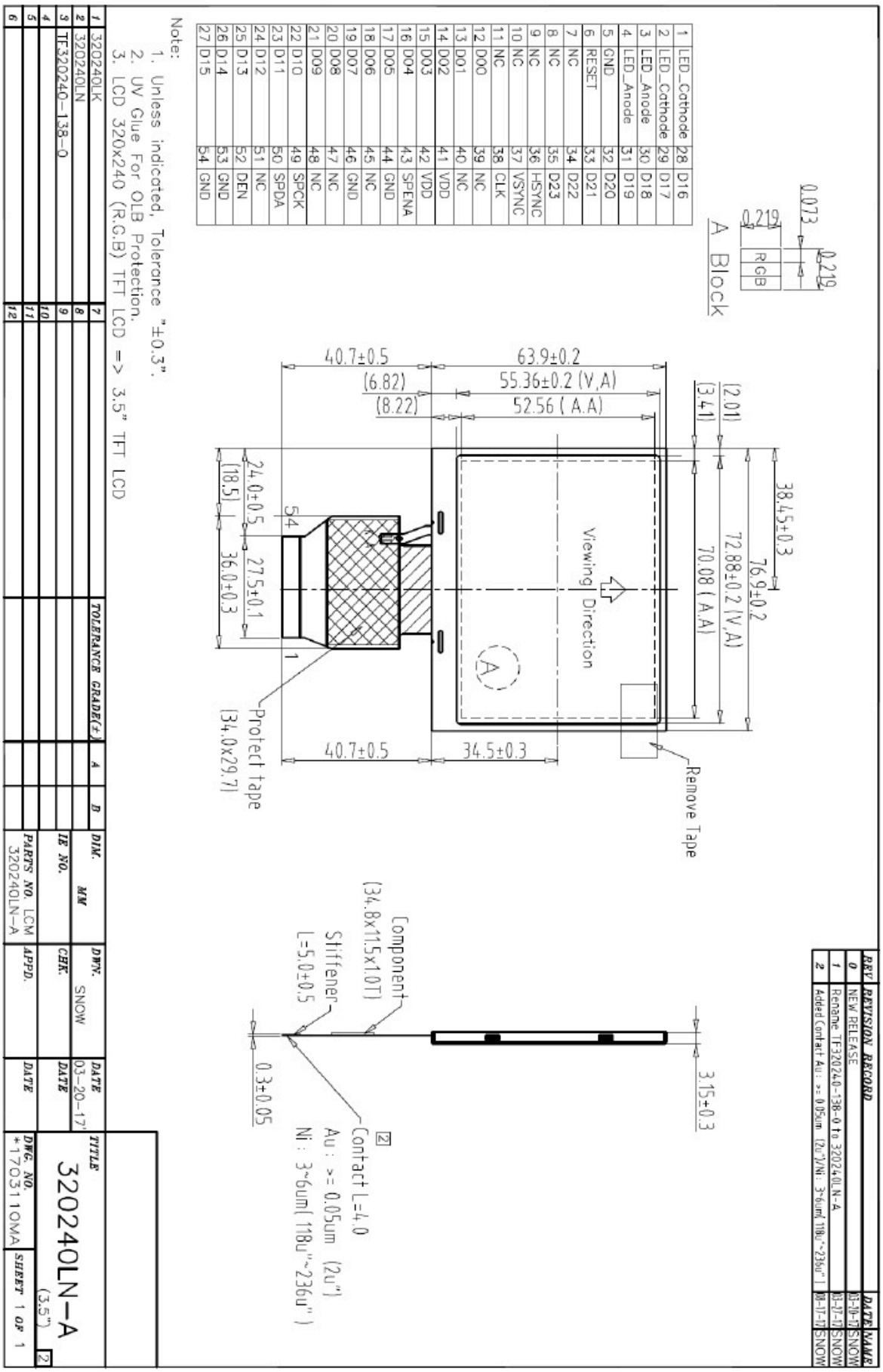
7.4 Operating precautions

1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.
8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

7.5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) Do not keep the LCD at the same display pattern continually. The residual image will happen and it will damage the LCD. Please use screen saver.
3) AMIPRE will provide one year warrantee for all products and three months warrantee for all repairing products.

8 OUTLINE DIMENSION



	LED_Cathode		D16
2	LED_Cathode	29	D17
3	LED_Anode	30	D18
4	LED_Anode	31	D19
5	GND	32	D20
6	RESET	33	D21
7	NC	34	D22
8	NC	35	D23
9	NC	36	HSYNC
10	NC	37	VSYNC
11	NC	38	CLK
12	D00	39	NC
13	D01	40	NC
14	D02	41	VDD
15	D03	42	VDD
16	D04	43	SPENA
17	D05	44	GND
18	D06	45	NC
19	D07	46	GND
20	D08	47	NC
21	D09	48	NC
22	D10	49	SPCK
23	D11	50	SPDA
24	D12	51	NC
25	D13	52	DEN
26	D14	53	GND
27	D15	54	GND

Note:
1. Unless indicated, Tolerance "±0.3".
2. UV Glue For OLB Protection.
3. LCD 320x240 (R.G.B) TFT LCD => 3.5" TFT LCD

REV.	REVISION RECORD	DATE	NAME
0	NEW RELEASE	03-14-17	SNOW
1	Rename TF320240-138-0 to 320240LN-A	03-17-17	SNOW
2	Added Contact Au : >= 0.05um (2u")/Ni : 3~6um(118u"~236u")	03-17-17	SNOW

	PARTS NO.	DIM.	DWN.	DATE
1	320240LK	TOLERANCE GRADE(+)	SNOW	03-20-17
2	320240LN	MM	CHK.	DATE
3	TF320240-138-0	IE NO.	APPD.	DATE
4				
5				
6				
7		A		
8		B		
9				
10				
11				
12				

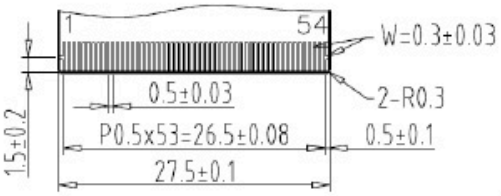
PARTS NO. LCM 320240LN-A

TITLE: 320240LN-A (3.5")

DWG. NO. *17031 1OMA

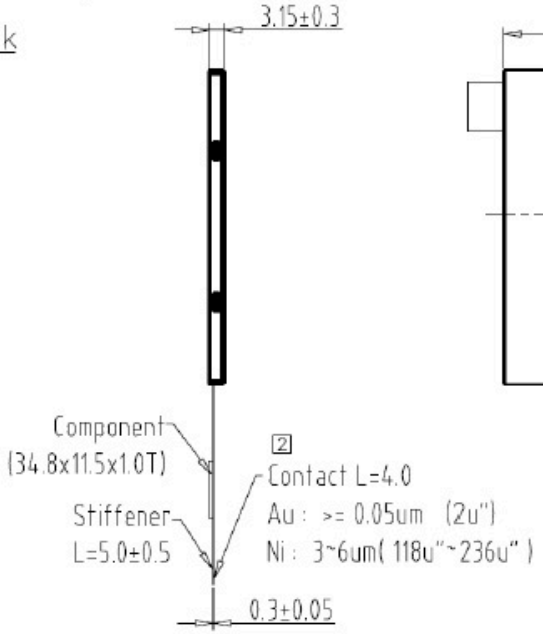
SHEET 1 OF 1

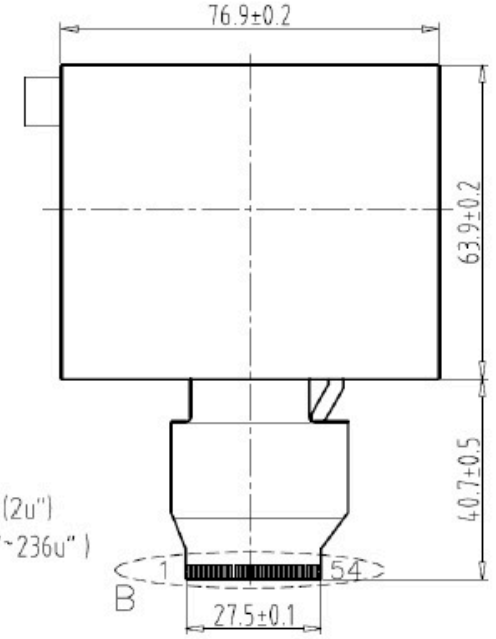
REV	REVISION RECORD	DATE	NAME
0	NEW RELEASE	03-20-17	SNOW
1	Rename TF320240-138-0 to 320240LN-A	03-27-17	SNOW
2	Added Contact Au : >= 0.05um (2u")/Ni : 3~6um(118u"~236u")	08-17-17	SNOW



B Block

1	LED_Cathode	28	D16
2	LED_Cathode	29	D17
3	LED_Anode	30	D18
4	LED_Anode	31	D19
5	GND	32	D20
6	RESET	33	D21
7	NC	34	D22
8	NC	35	D23
9	NC	36	HSYNC
10	NC	37	VSYNC
11	NC	38	CLK
12	D00	39	NC
13	D01	40	NC
14	D02	41	VDD
15	D03	42	VDD
16	D04	43	SPENA
17	D05	44	GND
18	D06	45	NC
19	D07	46	GND
20	D08	47	NC
21	D09	48	NC
22	D10	49	SPCK
23	D11	50	SPDA
24	D12	51	NC
25	D13	52	DEN
26	D14	53	GND
27	D15	54	GND





Back view

Note:
1. Unless indicated, Tolerance "±0.3".
2. UV Glue For OLB Protection.
3. LCD 320x240 (R.G.B) TFT LCD => 3.5" TFT LCD

				TOLERANCE GRADE(±)	A	B	DIM.	DWN.	DATE	TITLE
1	320240LK	7					MM	SNOW	03-20-17'	320240LN-A (3.5") 2
2	320240LN	8					IE NO.	CHK.	DATE	
3	TF320240-138-0	9								
4		10								
5		11					PARTS NO. LCM-1 320240LN-A	APPD.	DATE	DWG. NO. *1703111MA SHEET 1 OF 1
6		12								

9 Packing Drawing