Laird™
CONNECTIVITY

Datasheet

Sterling™ LWB+

Version 1.2

REVISION HISTORY

Version	Date	Notes	Contributors	Approver
1.0	26 Jan 2022	Initial version	Andrew Chen	Andrew Ross
1.1	17 Feb 2022	Clarified MSL Level 4 for LWB+ Series	Connie Lin	Jonathan Kaye
1.2	20 Feb 2022	Correct WL_Host_WAKE to pin-11	Andrew Chen	Andrew Ross

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CONTENTS

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Americas: +1-800-492-2320
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TABLE OF TABLES

Americas: +1-800-492-2320
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TABLE OF FIGURES

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1 SCOPE

This document describes key hardware aspects of the Laird Connectivity Sterling-LWB™ +.

2 INTRODUCTION

2.1 General Description

The Sterling LWB+ is a high performance 2.4 GHz WLAN and Bluetooth combo module based on latest-generation silicon (Infineon's AIROC™ CYW43439). With an industrial temperature rating, broad country certifications, and the availability of three different package styles, the Sterling LWB+ provides significant flexibility to meet various end user application needs. The Sterling LWB+ is the successor of Laird Connectivity Sterling LWB product series. Two SMT type modules are even pin-to-pin and drop replacement to the platform using Sterling LWB.

The on-module chip antenna package style for the Sterling LWB+ eliminates complexity for design integration, simplifies manufacturing assembly with larger pin outs, and features an advanced chip antenna that offers greater resistance to de-tuning than typical trace or chip antennas.

The module includes the MAC, baseband, and radio to support WLAN applications and an independent, high-speed UART is provided for the Bluetooth host interface. In addition, the latest Linux and Android drivers are supported directly by Laird Connectivity and Infineon.

Features

- IEEE 802.11 b/g/n (single stream n)
- Typical WLAN Transmit Power:
  - +18.0 dBm, 11 Mbps, CCK (b)
  - +16.0 dBm, 54 Mbps, OFDM (g)
  - +15.0 dBm, HT20 MCS7 (n)
- Typical WLAN Sensitivity:
  - -88 dBm, 8% PER,11 Mbps (b)
  - -75 dBm, 10% PER, 54 Mbps (g)
  - -72 dBm, 10% PER, MCS7 (n)
- Bluetooth v5.0 BR /EDR/LE
- Typical Bluetooth Transmit Power:
  - 6.5dBm BDR
  - 3.5dBm EDR
  - 6.5dBm BLE
- Typical Bluetooth Receive Sensitivity:
  - -91dBm, 1DH5/2DH5
  - -83dBm, 3DH5
  - -91dBm, BLE
- WLAN and Bluetooth coexistence
- Available in two footprint styles:
  - SMT Module: 15.5 mm x 21 mm
  - SiP: 12 mm x 12 mm
- Available with antenna trace pin, integrated chip antenna or MHF® 4 connector for external antenna
- Operating voltage: VBAT 3.2V to 4.8V (3.6V typical)
- Operating temperature: -40º to +85º C
- Operating Humidity: less than 85% R.H.
- Storage temperature: -40° to +125°C
- Storage Humidity: Less than 60% R.H
- Compact design based on Infineon CYW4349_A1 SoC
- Worldwide acceptance: FCC, ISED (Canada), EU, MIC (Japan), and AS/NZS
- BT SIG QDID: 100864
- REACH and RoHS compliant

Applications

- Security and building automation
- Internet of Things/M2M connectivity
- Smart gateways

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3 MODULE VARIANTS

The Sterling LWB+ Module is available in three different versions. Depending on the user's antenna and footprint needs, there is a variant to suite most application requirements. Laird Connectivity recommends that for simplicity of both the host PCB design, as well as the manufacturing process, that either the Chip Antenna or RF Connector version of the modules be used in your design.

3.1 453-00083 - Base SiP module

This module variant is supplied in a compact, 47 pin, 0.5 mm pitch LGA footprint. Unlike the other module variants, it requires the addition of either an off-module antenna or RF connector, as well as the associated matching components. In order to benefit from the EMC certifications on the module, strictly following the layout in the module application guide is required. This requires adherence to the PCB stack-up and layout around the antenna. The footprint of this module may require additional care during reflow and PCB assembly.

Figure 1: Sterling LWB+ base SiP module (453-00083)

3.2 453-00084 – MHF® 4 module

This module variant integrates the 453-00084 Base SiP Module, a MHF® 4 RF connector, and all associated RF matching components on a PCB. This integrated approach not only provides a MHF® 4 connector for connections to external antennas, but also simplifies and reduces the cost of the end users host board by simplifying the module PCB footprint.

Figure 2: Sterling LWB+ MHF® 4 module (453-00084)

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3.3 453-00085 – Chip Antenna module

This module variant integrates the 453-00085 Base SiP Module, a ceramic chip antenna, and all associated RF matching components on a PCB. This integrated antenna module simplifies and reduces the cost for the host integration of using the module.

Figure 3: Sterling LWB+ Chip Antenna module (453-00085)

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4 FUNCTIONAL DESCRIPTION

4.1 WLAN Features

- IEEE 802.11b/g/n 1x1 2.4 GHz Radio
  - Internal Power Amplifier (PA)
  - Internal Low Noise Amplifier (LNA)
  - Internal T/R Switch
  - Simultaneous BT/WLAN reception with a single antenna.
- SDIO V2.0 interface
- Media Access Controller (MAC)
- Physical Layer (PHY)
- Baseband Processor
- Standards
  - IEEE 802.11b, 802.11g, 802.11n (single stream)

4.2 Bluetooth Features

- Class 1 power amplifier with Class 1 capability
- HCI Interface using High Speed UART
- PCM for Audio Data
- High speed UART Host Controller Interface (HCI)
- Bluetooth v5.0 BR/EDR/LE

4.3 Wireless Security System Features

Supported modes:

- Open (no security)
- WEP
- WPA Personal
- WPA2 Personal
- WPA3
- WMM
- WMM-PS (U-APSD)
- WMM-SA
- WAPI
- AES (Hardware Accelerator)
- TKIP (host-computed)
- CKIP (SW Support)

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5 BLOCK DIAGRAMS

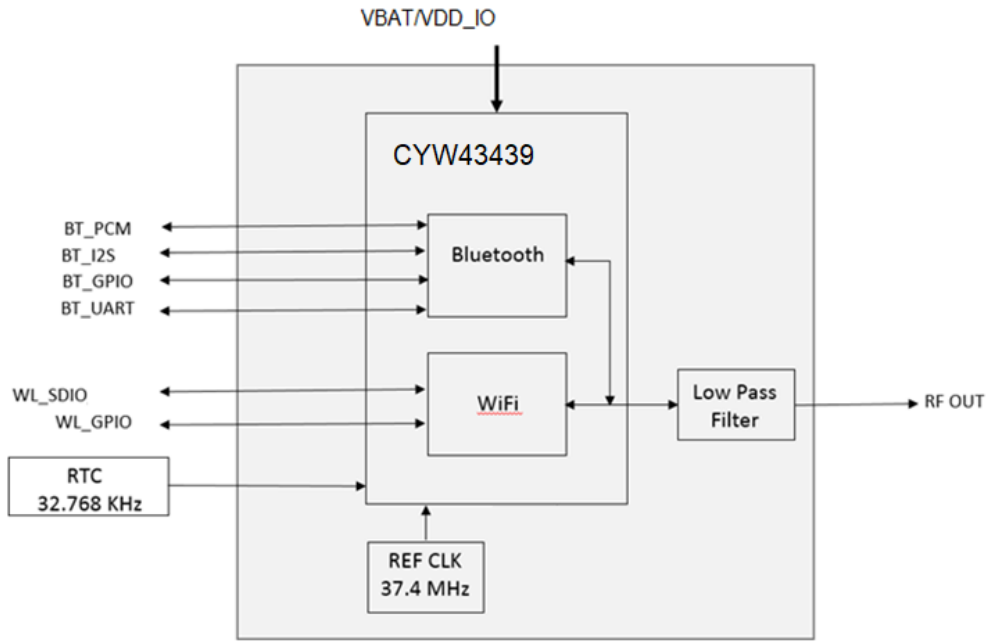

Figure 4: Sterling LWB+ base SiP module block diagram

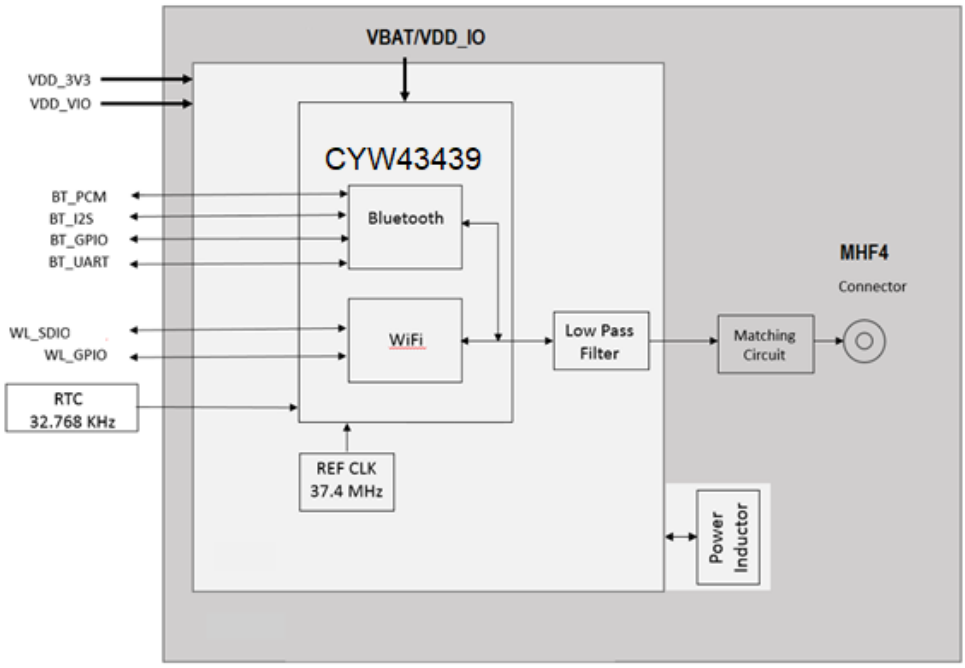

Figure 5: Sterling LWB+ MHF® 4 module block diagram

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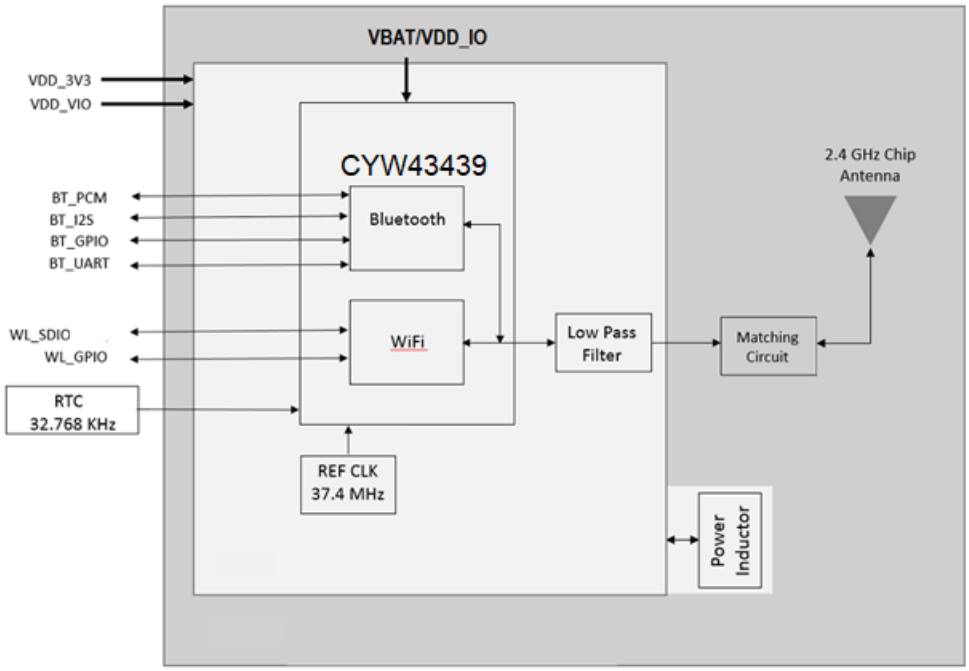

Figure 6: Sterling LWB+ chip antenna module block diagram

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6 GENERAL CHARACTERISTICS

Table 1: General Characteristics

Characteristic	Description
Model Name	Sterling LWB+
Product Description	Wi-Fi and Bluetooth Wireless Module
Dimension (SiP Module)	12 mm x 12 mm x 1.5 mm (W*L*T)
Dimension (Antenna Option Module)	15.5 mm x 21 mm x 2 mm (W*L*T)
Operating temperature	-40°C to 85°C
Storage temperature	-40°C to 125°C
Weight	TBD g ± 0.1g

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulators	-0.5		6	V
VDDIO	DC supply voltage for digital I/O	-0.5		3.9	V

7.2 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT	Power supply for Internal Regulators	3.2*	3.6	4.8*	V

Note: *Optimal RF performance is guaranteed only for 3.2V<VBAT<4.8V

7.3 Digital IO Pin DC Characteristics

Table 4: Digital I/O Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
For SDIO Interface VDDIO =1.8V					
VIH	Input high voltage	1.27	-	-	V
VIL	Input low voltage	-	-	0.58	V
VOH	Output High Voltage @ 2mA	1.4	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.45	V
For SDIO Interface VDDIO =3.3V					
VIH	Input high voltage	0.625 x VDDIO	-	-	V

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Symbol	Parameter	Minimum	Typical	Maximum	Unit
VIL	Input low voltage	-	-	0.25 x VDDIO	V
VOH	Output High Voltage @ 2mA	0.75 x VDDIO	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.125 x DDIO	V
Other Digital Interface VDDIO=1.8V					
VIH	Input high voltage	0.65 x VDDIO	-	-	V
VIL	Input low voltage	-	-	0.35 x VDDIO	V
VOH	Output High Voltage @ 2mA	VDDIO – 0.45	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.45	V
Other Digital Interface VDDIO=3.3V					
VIH	Input high voltage	2.00	-	-	V
VIL	Input low voltage	-	-	0.80	V
VOH	Output High Voltage @ 2mA	VDDIO – 0.4	-	-	V
VOL	Output Low Voltage @ 2mA	-	-	0.40	V

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7.4 WLAN RF Characteristics

7.4.1 WLAN RF TX Characteristics *(VBAT=3.3V, TA=25 °C)*

Table 5: WLAN Transmitter RF Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps DSSS (b) TX Output Power	1 Mbps BPSK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	18.0	-	dBm
11 Mbps DSSS (b) TX Output Power	11 Mbps CCK 802.11(b) Mask Compliance 35% EVM RMS power over TX packet	-	18.0	-	dBm
6 Mbps OFDM (g) TX Output Power	6 Mbps BPSK 802.11(g) Mask Compliance -5 dB EVM RMS power over TX packet	-	18.0	-	dBm
54 Mbps OFDM (g) TX Output Power	54 Mbps 64-QAM 802.11(g) Mask Compliance -25 dB EVM RMS power over TX packet	-	16.0	-	dBm
MCS0 OFDM (n) TX Output Power	6.5 Mbps BPSK 802.11(n) Mask Compliance -5 dB EVM RMS power over TX packet	-	18.0	-	dBm
MCS7 OFDM (n) TX Output Power	65 Mbps 64-QAM 802.11(n) Mask Compliance -27 dB EVM RMS power over TX packet	-	15.0	-	dBm

7.4.2 WLAN RF RX Characteristics *(VBAT=3.3V, TA=25 °C)*

Table 6: WLAN Receiver RF Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps DSSS (b) RX Sensitivity	8% PER	-	-94	-	dBm
11 Mbps DSSS (b) RX Sensitivity	8% PER	-	-88	-	dBm
6 Mbps OFDM (g) RX Sensitivity	10% PER	-	-90	-	dBm
54 Mbps OFDM (g) RX Sensitivity	10% PER	-	-75	-	dBm
MCS0 (6.5 Mbps) OFDM (n) RX Sensitivity	10% PER	-	-89	-	dBm
MCS7 65 Mbps OFDM (n) RX Sensitivity	10% PER	-	-72	-	dBm
11b RX Overload Level	8% PER, 11 Mbps	-10	-	-	dBm
11g RX Overload Level	10% PER, 54 Mbps	-20	-	-	dBm
11n RX Overload Level	10% PER, MCS7	-20	-	-	dBm

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7.5 Bluetooth RF Characteristics

7.5.1 Bluetooth TX RF Characteristics *(VBAT=3.3V, TA=25 °C)*

Table 7: Bluetooth Transmitter GFSK and EDR Characteristics

Parameter	Test Conditions	Min	Typical	Max	Bluetooth Spec	Unit
GFSK RF Output Power		-	6.5	-		dBm
EDR RF Output Power		-	3.5	-		dBm
Power Control Step Size		2	4	8	2-8	dB
EDR Relative Power		-4		1	-4/+1	dB

7.5.2 Bluetooth RX RF Characteristics *(VBAT=3.3V, TA=25 °C)*

Table 8: Bluetooth Receiver Characteristics

Parameter	Test Conditions	Min	Typical	Max	Bluetooth Spec	Unit
GFSK Sensitivity	BER=0.1%	-	-91	-	-70	dBm
EDR 2 Mbps Sensitivity	BER=0.01%	-	-91	-	-70	dBm
EDR 3 Mbps Sensitivity	BER=0.01%	-	-83	-	-70	dBm
BLE	PER = 30.8%	-	-91	-	-70	dBm

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7.6 Current consumption

7.6.1 WLAN Current consumption

Test Condition

1. All results are with the **Bluetooth off** (BT_REG_ON=LOW).
2. All results are run to **take 3 minutes** then record the test **average** and maximum value.
3. Power Save mode record 1 DTIM interval.

Table 9: Bluetooth Test conditions (VBAT = VDDIO = 3.6VDC)

No.	Item			VBAT=3.6V(mA)		
				Max	Avg.	
1	Leakage (OFF) *(1)				3.9µA	
2	Sleep*(3)			8.1µA	5.5µA	
3	Power Save DTIM1 (2.4GHz)*(4)(6)			27mA	1.2mA	
4	Power Save DTIM3 (2.4GHz)*(5)(6)			31mA	773uA	
Band (GHz)	**Mode**	**BW (MHz)**	**RF Power (dBm)**	**Transmit**		
				Max.	**Avg.**	**Duty(%)**
2.4	11b@1Mbps	20	18	303	301	96
	11g@54Mbps	20	16	194	192	49
	11n@MCS7	20	15	182	181	54
Band (GHz)	**Mode**	**BW(MHz)**		**Receive**		
				Max.	**Avg.**	
2.4	11b@1Mbps	20		37	35	
	11n@MCS7	20		37	34	

**Transmit Option: Packet Interval=500 / Packet length=1000*

Table 10: Bluetooth Test Conditions (VDDIO = 1.8VDC)

No.	Item			VDDIO=1.8 V	
				Max	Avg.
1	Leakage (OFF)*(1)			0.08µA	
2	Sleep*(3)			94µA	86µA
3	Power Save DTIM1 (2.4GHz)*(4)(6)			158µA	79µA
Band (GHz)	**Mode**	**BW (MHz)**	**RF Power (dBm)**	**Transmit**	
				Max.	**Avg.**
2.4	11b@1Mbps*(7)	20	18	52µA	48µA
Band (GHz)	**Mode**	**BW(MHz)**		**Receive**	
				Max.	**Avg.**
2.4	11b@1Mbps*(7)	20		62µA	48µA

(1) WLAN and Bluetooth OFF (WL_REG_ON=LOW, BT_REG_ON=LOW),DUT do not connected to VUB300 and ttyUSB0.
(2) No.2~6 Load the WLAN normal driver/firmware
(3) Run commad "wlfmac_x86 deepsleep 1" into sleep
(4) Associated with AP use ASUS RT-AC66U, DTIM = 1, Beacon Interval = 100ms
(5) Associated with AP use ASUS RT-AC66U, DTIM = 3, Beacon Interval = 100ms
(6) Run the following command and measured a current consumed across

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the DTIM duration "wlfmac_x86 mpc 1"
"wlfmac_x86 PM 2"
"wlfmac_x86 bcntrim 9"
(7) *Host SDIO-1.8V ,JP4 #1 #2*

7.6.2 Bluetooth Current consumption

Test Condition

1. The Bluetooth is in test mode run transmit or receive with a specified output power measure current consumption.
2. All results are with the **WLAN OFF(WL_REG_ON=LOW)**
3. All results are run to **take 3 minutes** then record the test **average** and maximum value.

Table 11: Bluetooth Current Consumption

No.	Mode	Packet Type	RF Power (dBm)	VBAT=3.6 V	
				Max.	Avg.
1	Sleep	n/a	n/a	39.8µA	18µA
2	Transmit*(1)	DH5	9.3	25.3mA	25.1mA
3	Receive*(1)	3DH5	n/a	11.2mA	11.1mA
4	Transmit*(2)	LE	8.9	28.1mA	28.0mA
5	Receive	LE	n/a	12.1mA	12.1mA

(1) BlueTool BB_Packet_Length=65535
(2) BlueTool Length_of_Test_Data=37

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8 PIN DEFINITIONS

8.1 Base SIP Pin Definitions

Note: PO = Power Output, PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, RF = Bi-directional RF Port, GND = Ground

Table 12: Sterling LWB+ SiP pin Description (453-00083)

Pin No	Name	I/O Type	Voltage Domain	Basic Description
1	GND	GND		Ground.
2	GND	GND		Ground.
3	WL_BT_ANT	RF		WLAN/BT RF TX/RX path.
4	GND	GND		Ground.
5	NC	Floating		Floating Pin, No connect to anything.
6	BT_WAKE_DEV	DI	VDDIO	HOST wake-up Bluetooth device
7	BT_HOST_WAKE	DO	VDDIO	Bluetooth device to wake-up HOST
8	CLK_REQ	DO	VDDIO	External system clock request—Used when the system clock is not provided by a dedicated crystal (for example, when a shared TCXO is used). Asserted to indicate to the host that the clock is required. Shared by BT, and WLAN.
9	GND	GND		Ground.
10	NC	Floating		Floating Pin, No connect to anything.
11	VBAT	PI	VBAT	3.2 to 4.8V power pin
12	WL_REG_ON	DI	VDDIO	Used by PMU to power up or power down the internal regulators used by the WLAN section. Also, when de-asserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.
13	WL_ HOST_WAKE (WL_GPIO_0)	DO	VDDIO	WLAN device to wake-up HOST
14	SDIO_DATA_2 (JTAG_TDO)	DIO	VDDIO	SDIO Data Line 2
15	SDIO_DATA_3 (JTAG_TRS TN)	DIO	VDDIO	SDIO Data Line 3
16	SDIO_CMD	DIO	VDDIO	SDIO Command Input
17	SDIO_DATA_0 (JTAG_TMS)	DIO	VDDIO	SDIO Data Line 0
18	SDIO_CLK (JTAG_TCK)	DI	VDDIO	SDIO Clock Input
19	SDIO_DATA_1 (JTAG_TDI)	DIO	VDDIO	SDIO Data Line 1
20	GND	GND		Ground.

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Pin No	Name	I/O Type	Voltage Domain	Basic Description
21	SR_VLX_1	PO	1.4V	Internal Buck voltage generation output pin. Note: An external low pass filter with inductor (0603,2.2uH +/-20%, DCR<=0.2Ω) and capacitor (Ceramic, X5R, 0402, ESR <30 mΩ at 4 MHz, 4.7 µF ±20%, 10V) is needed. Keep the L-C ground return loop as smaller as possible and feed the voltage to the VIN_LDO pin with trace that rating up to 1.4A.
22	VDDIO	PWR	VDDIO	1.8V-3.3V VDDIO supply for WLAN and BT
23	VIN_LDO	PI	1.4V	Power input for internal LDO.
24	32KHZ_OSC_IN	DI	0.2~3.3V	External 32K or RTC clock
25	BT_PCM_OUT	DO	VDDIO	PCM data Out
26	BT_PCM_CLK	DIO	VDDIO	PCM Clock
27	BT_PCM_IN	DI	VDDIO	PCM data Input
28	BT_PCM_SYNC	DO	VDDIO	PCM Synchronization control
29	NC	Floating		Floating Pin, No connect to anything.
30	NC	Floating		Floating Pin, No connect to anything.
31	GND	GND		Ground.
32	NC	Floating		Floating Pin, No connect to anything.
33	GND	GND		Ground.
34	BT_REG_ON	DI	VDDIO	Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when de-asserted, this pin holds the Bluetooth section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.
35	NC	Floating		Floating Pin, No connect to anything.
36	GND	GND		Ground.
37	NC	Floating		Floating Pin, No connect to anything.
38	NC	Floating		Floating Pin, No connect to anything.
39	WL_GPIO_2	DIO	VDDIO	PROGRAMMABLE GPIO PIN
40	WL_GPIO_1	DIO	VDDIO	PROGRAMMABLE GPIO PIN
41	BT_UART_TXD	DO	VDDIO	High-Speed UART Data Out
42	BT_UART_RTS_N	DO	VDDIO	High-Speed UART RTS
43	BT_UART_RXD	DI	VDDIO	High-Speed UART Data In
44	BT_UART_CTS_N	DI	VDDIO	High-Speed UART CTS
45	NC	Floating		Floating Pin, No connect to anything.
46	NC	Floating		Floating Pin, No connect to anything.
47	NC	Floating		Floating Pin, No connect to anything.

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8.2 MHF®4 Pin Definitions

Note: PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, GND = Ground

Table 13: Sterling LWB+ MHF® 4 and chip antenna module pin descriptions

Pin No	Name	I/O Type	Voltage Domain	Description
1	GND	GND	GND	GROUND
2	BT_PCM_SYNC	DIO	VDD_VIO	PCM SYNC; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
3	BT_PCM_IN	DI	VDD_VIO	PCM DATA INPUT SENSING
4	BT_PCM_OUT	DO	VDD_VIO	PCM DATA OUTPUT
5	VDD_3V3	PI	VDD_VIO	WIFI AND BLUETOOTH POWER SUPPLY
6	GND	GND	GND	GROUND
7	NC	Floating	Floating	Floating Pin, No connect to anything
8	NC	Floating	Floating	Floating Pin, No connect to anything
9	WL_GPIO_2	DIO	VDD_VIO	PROGRAMMABLE GPIO PIN
10	WL_GPIO_1	DIO	VDD_VIO	PROGRAMMABLE GPIO PIN
11	WL_ HOST_WAKE (WL_GPIO_0)	DO	VDD_VIO	WLAN device to wake-up HOST
12	WL_REG_ON	DI	VDD_VIO	USED BY PMU TO POWER UP OR POWER DOWN THE INTERNAL REGULATORS USED BY THE WLAN SECTION. Note: When de-asserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.
13	CLK_REQ	DO	VDD_VIO	External system clock request—Used when the system clock is not provided by a dedicated crystal (for example, when a shared TCXO is used). Asserted to indicate to the host that the clock is required. Shared by BT, and WLAN.
14	GND	GND	GND	GROUND
15	NC	Floating	Floating	Floating Pin, No connect to anything
16	NC	Floating	Floating	Floating Pin, No connect to anything
17	NC	Floating	Floating	Floating Pin, No connect to anything
18	GND	GND	GND	GROUND
19	32KHZ_OSC_IN	DI	VDD_VIO	EXTERNAL SLEEP CLOCK INPUT Note: the clock signal level is accepted from 0.2 to 3.3V
20	VDD_VIO	PI	VDD_VIO	DC SUPPLY FOR I/O

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Pin No	Name	I/O Type	Voltage Domain	Description
				Note: 1.8V or 3.3V
21	BT_REG_ON	DI	VDD_VIO	USED BY PMU TO POWER UP OR POWER DOWN THE INTERNAL REGULATORS USED BY THE BLUETOOTH SECTION. Note: When de-asserted, this pin holds the WLAN section in reset. This pin has an internal 200k ohm pull down resistor that is enabled by default. It can be disabled through programming.
22	SDIO_D0 (JTAG_TMS)	DIO	VDD_VIO	SDIO DATA LINE 0
23	SDIO_D1 (JTAG_TDI)	DIO	VDD_VIO	SDIO DATA LINE 1
24	GND	GND	GND	GROUND
25	SDIO_D2 (JTAG_TDO)	DIO	VDD_VIO	SDIO DATA LINE 2
26	SDIO_CMD	DIO	VDD_VIO	SDIO COMMAND LINE
27	SDIO_D3 (JTAG_TRSTN)	DIO	VDD_VIO	SDIO DATA LINE 3
28	GND	GND	GND	GROUND
29	SDIO_CLK (JTAG_TCK)	DIO	VDD_VIO	SDIO CLOCK LINE
30	GND	GND	GND	GROUND
31	BT_UART_RTS_L	DO	VDD_VIO	BT UART REQUEST-TO-SEND
32	BT_UART_CTS_L	DI	VDD_VIO	BT UART CLEAR-TO-SEND
33	BT_UART_TXD	DO	VDD_VIO	BT UART TRANSMIT OUTPUT
34	BT_UART_RXD	DI	VDD_VIO	BT UART RECEIVE INPUT
35	NC	Floating	Floating	Floating Pin, No connect to anything
36	NC	Floating	Floating	Floating Pin, No connect to anything
37	NC	Floating	Floating	Floating Pin, No connect to anything
38	BT_PCM_CLK	DIO	VDD_VIO	PCM CLOCK; CAN BE MASTER (OUTPUT) OR SLAVE (INPUT)
39	BT_DEV_WAKE	DI	VDD_VIO	DEV_WAKE OR GENERAL-PURPOSE I/O SIGNAL
40	BT_HOST_WAKE	DO	VDD_VIO	HOST_WAKE OR GENERAL-PURPOSE I/O SIGNAL
41	GND	GND	GND	GROUND
42	GND	GND	GND	GROUND
43	GND	GND	GND	GROUND

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Pin No	Name	I/O Type	Voltage Domain	Description
44	GND	GND	GND	GROUND
45	GND	GND	GND	GROUND
46	GND	GND	GND	GROUND
47	GND	GND	GND	GROUND

9 Power States

9.1 Module power states

The Sterling-LWB+ WLAN power states are described as follows:

- **Active mode** – All WLAN blocks in the Sterling LWB+ powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- **Doze mode** – The radio, analog domains, and most of the linear regulators are powered down. The rest of the LWB+ remains powered up in an IDLE state. All main clocks (PLL, crystal oscillator) are shut down to reduce active power to the minimum. The 32.768 kHz LPO clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Doze mode, the primary power consumed is due to leakage current.
- **Deep-sleep mode** – Most of the chip, including analog and digital domains, and most of the regulators are powered off. Logic states in the digital core are saved and preserved to retention memory in the always-on domain before the digital core is powered off. To avoid lengthy hardware re-initialization, the logic states in the digital core are restored to their pre-deep-sleep settings when a wake-up event is triggered by an external interrupt, a host resume through the SDIO bus, or by the PMU timers.
- **Power-down mode** –The LWB+ effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators

9.2 MHF® 4 and Chip antenna module pin I/O states

Table 14: Sterling LWB+ MHF4 and Chip Antenna Module Pin I/O States

Pin #	Name	Keeper (b)	Active Mode	Low Power State/Sleep *(All Power Present)*	Power Down(c) WL_REG_ ON =0 BT_REG_O N = 0	Out of Reset: (VDD_VIO is present)		
						WL_REG_ON=1 BT_REG_ON= any	WL_REG_ ON =1 BT_REG_ ON = 0	WL_REG_O N =0 BT_REG_O N = 1
2	BT_PCM_SYNC	Y	Input No Pull (d)	Input No Pull (d)	High –Z No Pull	-	Input,PD	Input,PD
3	BT_PCM_I N	Y	Input No Pull (d)	Input No Pull (d)	High –Z No Pull	-	Input,PD	Input,PD
4	BT_PCM_ OUT	Y	Input No Pull (d)	Input No Pull (d)	High –Z No Pull	-	Input,PD	Input,PD
7	WIFI_GPIO_4	Y	TBD	Active Mode	High –Z No Pull (f)	Input,GCI GPIO[1] PU	Active Mode	Input,PU
8	WIFI_GPIO_3	Y	TBD	Active Mode	High –Z No Pull (f)	Input,GCI GPIO[0] PU	Active Mode	Input,PU
9	WIFI_GPIO_2	Y	TBD	Active Mode	High –Z No Pull (f)	Input,GCI GPIO[7] NoPull	Active Mode	Input, Strap, NoPull
10	WIFI_GPIO_1	Y	TBD	Active Mode	High –Z No Pull (f)	Input,PD	Active Mode	Input, Strap, PD

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Pin #	Name	Keeper (b)	Active Mode	Low Power State/Sleep *(All Power Present)*	Power Down(c) WL_REG_ ON =0 BT_REG_O N = 0	Out of Reset: (VDD_VIO is present)		
						WL_REG_ON=1 BT_REG_ON= any	WL_REG_ ON =1 BT_REG_ ON = 0	WL_REG_O N =0 BT_REG_O N = 1
11	WIFI_GPIO_0	Y	TBD	Active Mode	High –Z No Pull (f)	Input,SDIO OOB Int. NoPull	Active Mode	Input,NoPull
12	WL_REG_ ON	N	Input; PD (pull- down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (200K)	Input; PD (200K)	-
13	CLK_REQ	Y	Open drain or push-pull (Active high)	Open drain or push-pull (Active high)	PD	Open drain, (Active high)	Open drain, (Active high)	Open drain, (Active high)
21	BT_REG_ ON	N	Input; PD (pull- down can be disabled)	Input; PD (pull-down can be disabled)	Input; PD (of 200K)	Input; PD (200K)	Input; PD (200K)	Input; PD (200K)
22	SDIO_D0	N	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE - > Pull UP	SDIO MODE > No Pull	Input,PU
23	SDIO_D1	N	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE - > Pull UP	SDIO MODE > No Pull	Input,PU
25	SDIO_D2	N	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE - > Pull UP	SDIO MODE > No Pull	Input,PU
26	SDIO_CMD	N	SDIO MODE -> No Pull	SDIO MODE -> No Pull	SDIO MODE -> No Pull	SDIO MODE - >Pull UP	SDIO MODE -> No Pull	Input,PU
27	SDIO_D3	N	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE - > Pull UP	SDIO MODE > No Pull	Input,PU
29	SDIO_CLK	N	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE > No Pull	SDIO MODE - > No Pull	SDIO MODE > No Pull	Input
31	BT_UART_ RTS_L	Y	Output: No Pull	Output: No Pull	High-Z, No Pull	-	Input: PU	Output: NoPull
32	BT_UART_ CTS_L	Y	Input: NoPull	Input: No Pull	High- Z,No Pull	-	Input: PU	Input: NoPull
33	BT_UART_ TXD	Y	Output: No Pull	Output: No Pull	High- Z,No Pull	-	Input: PU	Output: NoPull
34	BT_UART_ RXD	Y	Input:PU	Input: No Pull	High- Z,No Pull	-	Input: PU	Input: NoPull
35	BT_I2S_CL K	Y	Input: No Pull (e)	Input: No Pull (e)	High-Z, No Pull	-	Input, PD	Output: Drive Low
36	BT_I2S_D0	Y	Input: No Pull (e)	Input: No Pull (e)	High-Z, No Pull	-	Input, PD	Input, PD
37	BT_I2S_W S	Y	Input: No Pull (e)	Input: No Pull (e)	High-Z, No Pull	-	Input, PD	Input, PD
38	BT_PCM_ CLK	Y	Input No Pull(d)	Input No Pull(d)	High –Z No Pull	-	Input, PD	Input, PD
39	BT_DEV_ WAKE	Y	I/O: PU,PD, No Pull	I/O: PU,PD, No Pull	High-Z, No Pull	-	Input, PD	Input, PD

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Pin #	Name	Keeper (b)	Active Mode	Low Power State/Sleep *(All Power Present)*	Power Down(c) WL_REG_ ON =0 BT_REG_O N = 0	Out of Reset: (VDD_VIO is present)		
						WL_REG_ON=1 BT_REG_ON= any	WL_REG_ ON =1 BT_REG_ ON = 0	WL_REG_O N =0 BT_REG_O N = 1
			(Programmable)	(Programmable)				
40	BT_HOST_ WAKE	Y	I/O: PU,PD, No Pull (Programmable)	I/O: PU,PD, No Pull (Programmable)	High-Z, No Pull	-	Input, PD	Output, Drive Low

The following notations are used:

- I: Input signal
- O: Output signal
- I/O: Input/Output signal
- PU = Pulled up
- PD = Pulled down
- No Pull = Neither pulled up nor pulled down

Notes:

4. PU = pulled up, PD = pulled down.
5. N = pad has no keeper. Y = pad has a keeper. Keeper is always active except in the power-down state. If there is no keeper, and it is an input and there is NoPull, then the pad should be driven to prevent leakage due to floating pad, for example, SDIO_CLK.
6. In the Power-down state (xx_REG_ON = 0): High-Z; NoPull => The pad is disabled because power is not supplied.
7. Depending on whether the PCM interface is enabled and the configuration is master or slave mode, it can be either an output or input.
8. Depending on whether the I2S interface is enabled, and configuration is master or slave mode, it can be either an input or output.
9. The GPIO pull states for the active and low-power states are hardware defaults. They can all be subsequently programmed as a pull-up or pull-down.
10. Strap state enables Serial Wire Debugging.

10 Crystal Oscillator Requirement

Table 15: Crystal Oscillator Specification

32.768 KHz Oscillator	
Frequency Accuracy	200 ppm
Duty Cycle	30% – 70%
Input Signal Amplitude	200-3300 mV, peak-peak
Signal Type	Square or Sine Wave
Clock Jitter	<10,000 ppm

IMPORTANT: A 32.768 KHz crystal is required for the module to be functional. The module will not boot without this crystal.

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11 Power-On Signal Timing Diagrams

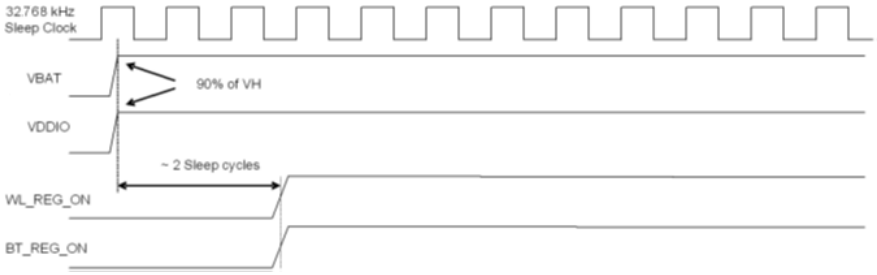

Figure 7: WLAN = ON, Bluetooth = ON

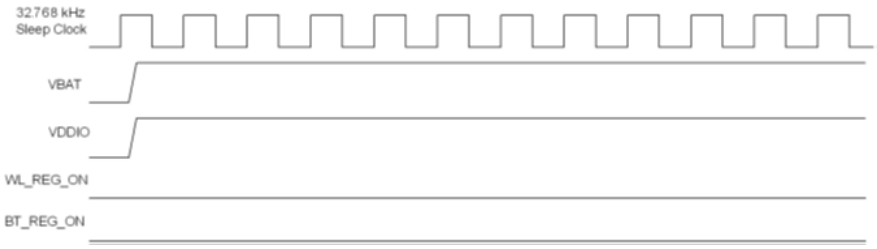

Figure 8: WLAN = ON, Bluetooth = ON

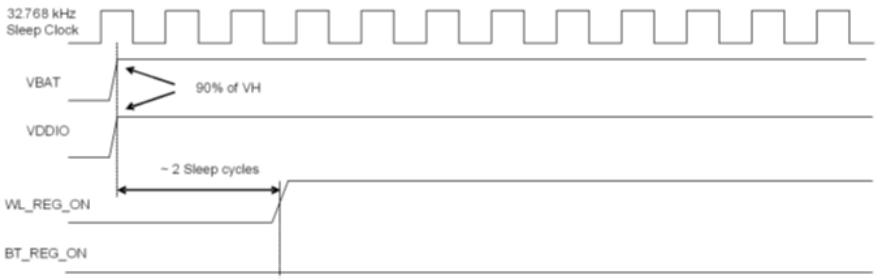

Figure 9: WLAN = ON, Bluetooth = OFF

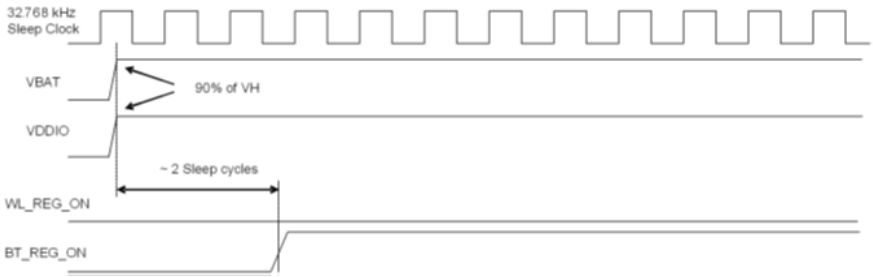

Figure 10: WLAN = OFF, Bluetooth = ON

Note: For both the WL_REG_ON and BT_REG_ON pins, there should be at least a 10ms time delay between consecutive toggles (where both signals have been driven low). This allows time for the CBUCK regulator to discharge. If this delay is not followed, then there may be a VDDIO in-rush current on the order of 36 mA during the next PMU cold start.

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12 HOST INTERFACE

12.1 WLAN SDIO interface

The Sterling LWB+ module WLAN section supports SDIO version 2.0. for both 1-bit (25 Mbps) and 4-bit modes (100 Mbps), as well as high speed 4-bit mode (50 MHz clocks—200 Mbps).

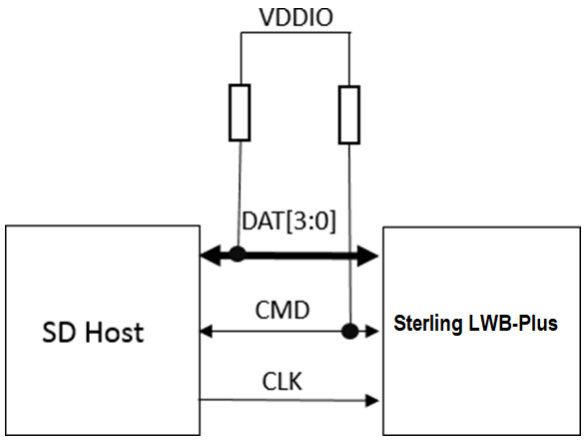

Figure 11: Signal connections to SDIO host (SD 4-bit mode)

Note: Pull-ups (10K to 100K) are required on data and CMD lines. This is required during all operating states by either external resistors or through pull-ups on the host device.

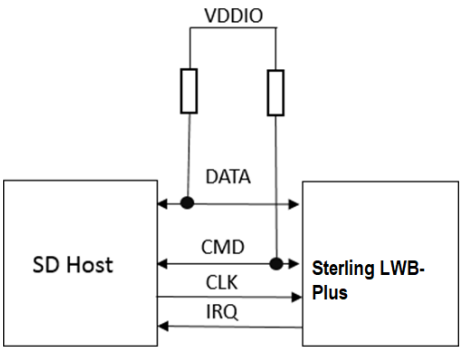

Figure 12: Signal connections to SDIO host (SD 1-bit mode)

Note: Pull-ups (10K to 100K) are required on data and CMD lines. This is required during all operating states by either external resistors or through pull-ups on the host device.

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12.2 Bluetooth UART interface

The Sterling LWB+ uses a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. The baud rate may be selected through a vendor specific UART HCI command to a value other than the default rate of 115.2 kbps.

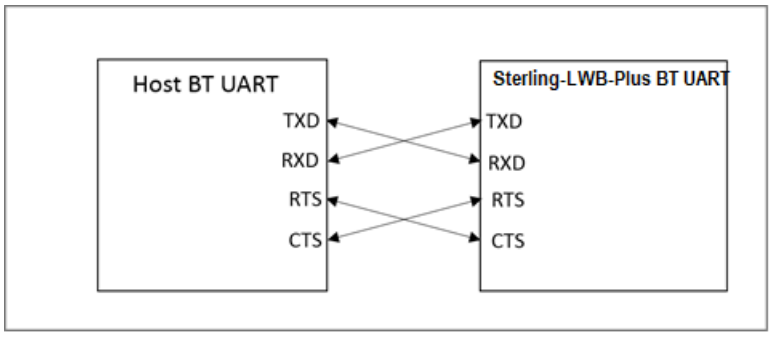

Figure 13: UART connection from Sterling-LWB to host

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13 MECHANICAL SPECIFICATIONS

13.1 Base SIP Module Footprint

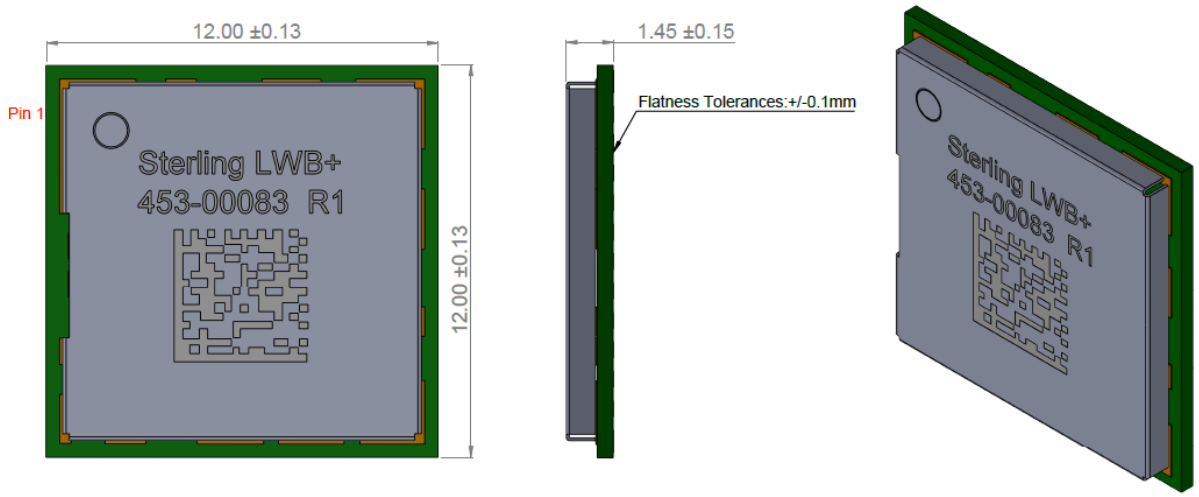

Figure 14: Sterling LWB+ base SiP module dimension

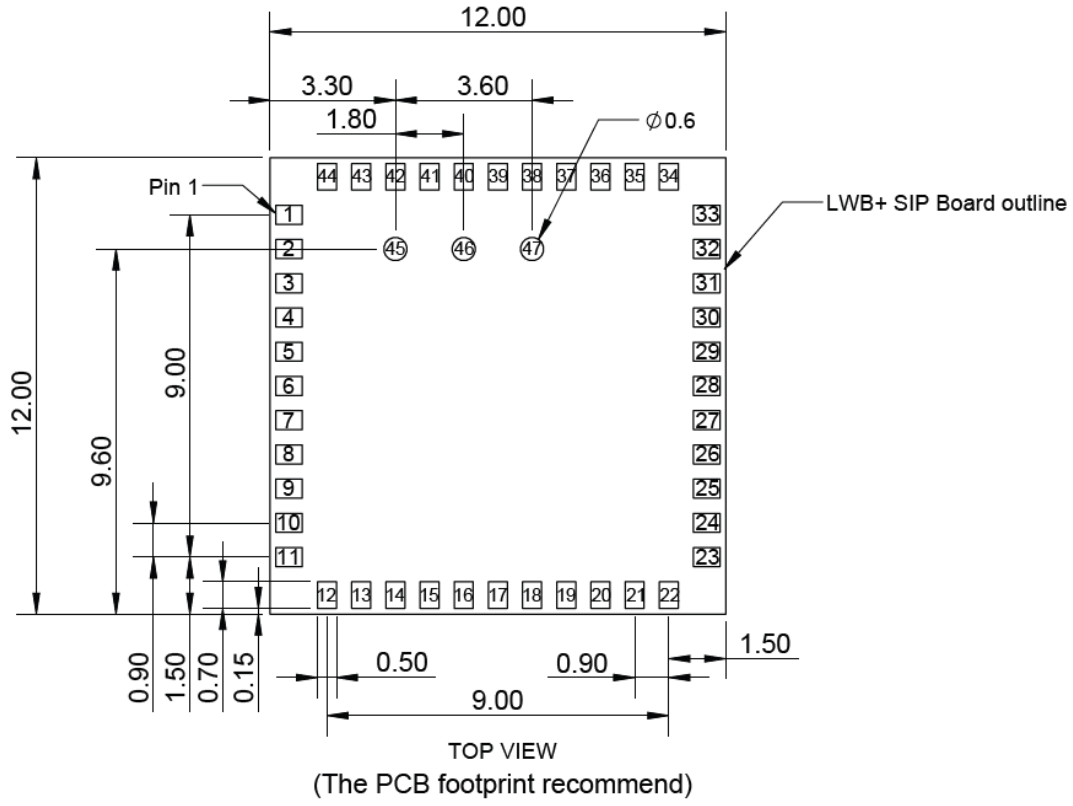

Figure 15: Sterling LWB+ base SiP module pinout (top view)

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13.2 MHF®4 and Chip Antenna module footprint

Note that the following footprint and pin definitions apply to the Sterling LWB+ MHF® 4 and Chip Antenna variants of the module (453-00084). There are two module footprints depending on which variant of the module is being used, so it is important to make certain you are using the correct version on your design.

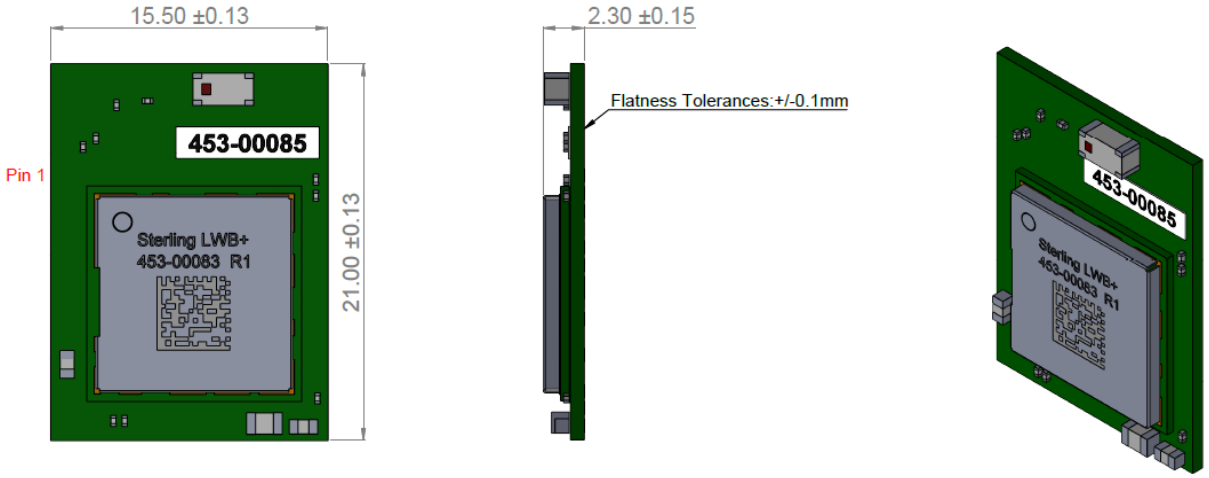

Figure 16: Sterling LWB+ MHF® 4 and chip antenna module dimension

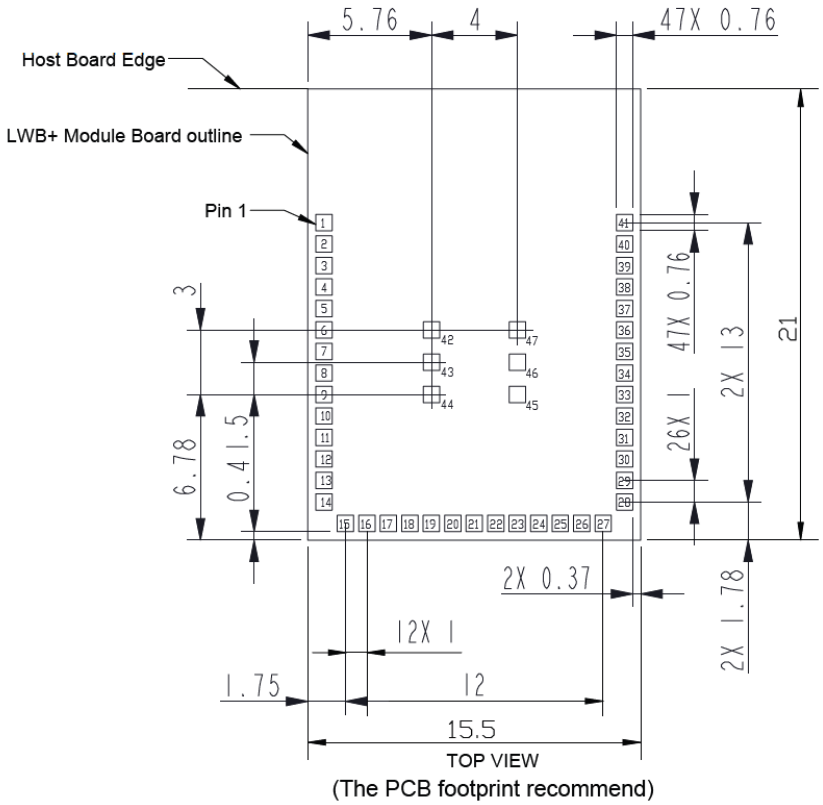

Figure 17: Sterling LWB+ MHF® 4 and chip antenna module pinout (top view)

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14 SOLDERING RECOMMENDATIONS

14.1 Reflow for lead Free Solder Paste

- Optimal solder reflow profile depends on solder paste properties and should be optimized as part of an overall process development.
- It is important to provide a solder reflow profile that matches the solder paste supplier's recommendations.
- Temperature ranges beyond that of the solder paste supplier's recommendation could result in poor solderability.
- All solder paste suppliers recommend an ideal reflow profile to give the best solderability.

14.2 Recommended Reflow Profile for lead Free Solder Paste

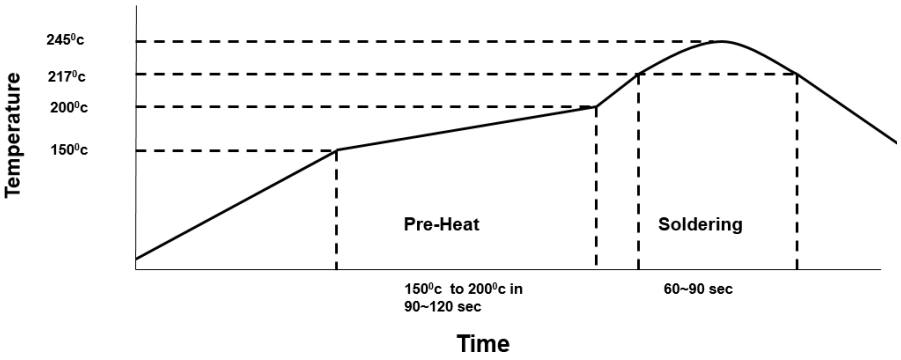

Figure 18: Recommended Reflow Profile

15 WI-FI / BLUETOOTH MAC ID

For the Sterling LWB+, the Wi-Fi MAC ID and Bluetooth MAC ID is preprogrammed during production for each module. The Bluetooth MAC ID is the Wi-Fi MAC ID plus one and Wi-Fi MAC ID is shown in the barcode on the shielding can.

Table 16: Example MAC ID assignments

	Wi-Fi MAC ID	Bluetooth MAC ID
Module 1	C0EE40B00000	C0EE40B00001
Module 2	C0EE40B00002	C0EE40B00003
Module 3	C0EE40B00004	C0EE40B00005
Module 4	C0EE40B00006	C0EE40B00007

16 MISCELLANEOUS

16.1 Cleaning

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently

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16.2 Rework

The Sterling LWB+ module can be unsoldered from the host board if the Moisture Sensitivity Level (MSL) requirements are met as described in this datasheet.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions terminate warranty coverage.

16.3 Handling and Storage

16.3.1 Handling

The Sterling LWB+ modules contain a highly sensitive electronic circuitry. Handling without proper ESD protection may damage the module permanently

16.3.2 Moisture Sensitivity Level (MSL)

The Sterling-LWB+ SIP and SMT modules are MSL level 4.

Per J-STD-020, devices rated as MSL 4 and not stored in a sealed bag with desiccant pack should be baked prior to use.

Devices are packaged in a Moisture Barrier Bag with a desiccant pack and Humidity Indicator Card (HIC). Devices that will be subjected to reflow should reference the HIC and J-STD-033 to determine if baking is required.

If baking is required, refer to J-STD-033 for bake procedure.

16.3.3 Storage

Per J-STD-033, the shelf life of devices in a Moisture Barrier Bag is 12 months at <40C and <90% room humidity (RH).

Do not store in salty air or in an environment with a high concentration of corrosive gas, such as Cl2, H2S, NH3, SO2, or NOX. Do not store in direct sunlight.

The product should not be subject to excessive mechanical shock.

16.3.4 Repeated Reflow Soldering

Only a single reflow soldering process is encouraged for host boards.

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17 REGULATORY

Note: For complete regulatory information, refer to the Sterling LWB+ Regulatory Information document which is also available from the Sterling LWB+ product page.

The Sterling LWB+ holds current certifications in the following countries:

Country/Region	Regulatory ID
USA (FCC)	SQG-LWBPLUS
EU	N/A
Canada (ISED)	3147A-LWBPLUS
Japan (MIC)	201-210737
Australia	N/A
New Zealand	N/A

18 ORDERING INFORMATION

Table 17: Orderable Sterling-LWB+ part numbers

Order Number	Description
453-00083C	Module, Sterling-LWB+, SIP, Cut Tape
453-00083R	Module, Sterling-LWB+, SIP, Tape and Reel
453-00084C	Module, Sterling-LWB+, MHF4, Cut Tape
453-00084R	Module, Sterling-LWB+, MHF4, Tape and Reel
453-00085C	Module, Sterling-LWB+, Chip Antenna, Cut Tape
453-00085R	Module, Sterling-LWB+, Chip Antenna, Tape and Reel
453-00084-K1	Development Kit, Sterling-LWB+, MHF4
453-00085-K1	Development Kit, Sterling-LWB+, Chip Antenna

Table 18: Module accessories

	Order Number	Description
	001-0001	2.4 GHz dipole antenna with reverse polarity SMA connector
	080-0001	U.FL to reverse polarity SMA bulkhead cable 105 mm

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	001-0014	2.4 GHz FlexPIFA antenna
	001-0015	2.4 GHz FlexNotch antenna
	001-0030	2.4 GHz Metal FlexPIFA antenna with U.FL cable, 100 mm

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19 BLUETOOTH SIG QUALIFICATION

19.1 Overview

The Sterling LWB+ module is listed on the Bluetooth SIG website as a qualified Controller Subsystem.

Design Name	Owner	Declaration ID	Model Number	Link to listing on the SIG website
Sterling LWB+	Laird	D056404	453-00083R	https://launchstudio.bluetooth.com/ListingDetails/142637
Sterling LWB+	Laird	D056404	453-00083C	https://launchstudio.bluetooth.com/ListingDetails/142637
Sterling LWB+	Laird	D056404	453-00084R	https://launchstudio.bluetooth.com/ListingDetails/142637
Sterling LWB+	Laird	D056404	453-00084C	https://launchstudio.bluetooth.com/ListingDetails/142637
Sterling LWB+	Laird	D056404	453-00085R	https://launchstudio.bluetooth.com/ListingDetails/142637
Sterling LWB+	Laird	D056404	453-00085C	https://launchstudio.bluetooth.com/ListingDetails/142637
Sterling LWB+	Laird	D056404	453-00084-K1	https://launchstudio.bluetooth.com/ListingDetails/142637
Sterling LWB+	Laird	D056404	453-00085-K1	https://launchstudio.bluetooth.com/ListingDetails/142637

It is a mandatory requirement of the Bluetooth Special Interest Group (SIG) that every product implementing Bluetooth technology has a Declaration ID. Every Bluetooth design is required to go through the qualification process, even when referencing a Bluetooth Design that already has its own Declaration ID. The Qualification Process requires each company to register as a member of the Bluetooth SIG – www.bluetooth.org

The following is a link to the Bluetooth Registration page: https://www.bluetooth.org/login/register/

For each Bluetooth Design, it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/fees

For a detailed procedure of how to obtain a new Declaration ID for your design, please refer to the following SIG document, (login is required to views this document):

https://www.bluetooth.org/DocMan/handlers/DownloadDoc.ashx?doc_id=283698&vId=317486

19.2 Qualification Steps When Referencing a Laird Connectivity Controller Subsystem Design

To qualify your product when referencing a Laird Connectivity Controller Subsystem design, follow these steps:

1. To start a listing, go to: https://www.bluetooth.org/tpg/QLI_SDoc.cfm

   Note: A username and password are required to access this site.

2. In step 1, select the option, New Listing and Reference a Qualified Design.
3. Enter *99404* in the Controller Subsystem table entry.
4. Enter your complimentary Host Subsystem and optional Profile Subsystem QDID in the table entry.
5. Select your pre-paid Declaration ID from the drop-down menu or go to the Purchase Declaration ID page.

   Note: Unless the Declaration ID is pre-paid or purchased with a credit card, you cannot proceed until the SIG invoice is paid.

6. Once all the relevant sections of step 1 are finished, complete steps 2, 3, and 4 as described in the help document accessible from the site.

   Your new design will be listed on the SIG website and you can print your Certificate and DoC.

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For further information please refer to the following training material:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/listing-process-updates

If you require assistance with the qualification process please contact our recommended Bluetooth Qualification Expert (BQE), Steve Flooks, steve.flooks@eurexuk.com.

Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852-2762-4823

20 Additional Assistance

Please contact your local sales representative or our support team for further assistance:

Laird Connectivity
Support Centre: https://www.lairdconnect.com/resources/support
Email: wireless.support@lairdconnectivity.com
Phone: Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852 2923 0610
Web: https://www.lairdconnect.com/products

Note: Information contained in this document is subject to change.