Laird™
CONNECTIVITY

Datasheet

Summit SOM 8M Plus

Version 1.1

REVISION HISTORY

Version	Date	Notes	Contributors	Approver
1.0	29 June 2022	Initial Release	Andy Dobbing Dan Kephart Chris Trowbridge	Andrew Chen
1.1	16 Aug 2022	Fixes to LE data rates in Wireless interface and Table 6	Dave Drogowski Dan Kephart	Andrew Chen

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1 SCOPE

This document describes key hardware aspects of Laird Connectivity's Summit SOM 8M Plus system-on-module which is based on the i.MX8M Plus processor family and the NXP 88W8997 Wi-Fi/BT combo radio. Data in this document is drawn from several sources and includes information found in the documentation for NXP's i.MX8M Plus and 88W8997.

Note: Information in this document is subject to change. Contact us for the most updated version of this document.

2 INTRODUCTION

The Summit SOM 8M Plus is an integrated platform solution with Quad Cortex®-A53 processors operating up to 1.6 GHz and pre-certified dual-band Wi-Fi (2X2 MIMO, 802.11a/b/g/n/ac) with Bluetooth 5.3 dual mode connectivity.

Quad Arm® Cortex®-A53 processors are integrated with an NPU of 2.3 TOPS that greatly accelerates machine learning inference. The vision engine is composed of two MIPI-CSI camera inputs and an HDR-capable Image Signal Processor (ISP) capable of 375 MPixels/s. The advanced multimedia capabilities include several display interfaces, HDMI 2.0a (eARC), MIPI-DSI, and LVDS. These interfaces can utilize the onboard 1080p60 video encode and decode in H.265 and H.264 format, along with an onboard GPU that is a 3D and 2D graphic accelerator supporting 1 GPixel/s, OpenVG 1.1, Open GL ES3.1, Vulkan, and Open CL 1.2 FP. Multiple audio and microphone interfaces are available along with the audio processing capabilities of the HiFi 4 DSP operating at 800MHz for Immersive Audio and Voice systems.

The Summit SOM 8M Plus features an Arm® Cortex®-M7 microcontroller running at 800 MHz for customer applications to offload the Cortex®-A53 processor for real time and low power operation. A variety of robust control networks for industrial application are possible via CAN-FD interfaces, SPI, I2C, UART, USB 3.0, and dual Gb Ethernet including one supporting Time Sensitive Network for low latency applications.

The Summit SOM 8M Plus is pre-calibrated and integrates the complete transmit/receive RF paths including diplexer, switches, reference crystal oscillator and power manage units (PMU). Two RF connectors (U. FL) on the module provide the most flexibility of antenna selection and installation for the best antenna performance. Several high-performance antennas are certified with the Summit SOM 8M Plus. A detailed antenna list is shown in the Certified Antennas section.

The SOM 8M Plus provides IEEE 802.11 ac (wave 2) 2X2 MIMO Wi-Fi capability with data rates up to MCS9 (866.7 Mbps) as well as a BT 5.3 radio solution.

- Supports **Adaptive World Mode:** ship a single SKU worldwide
- Supports the latest **WPA3-Personal, WPA3-Enterprise**, and **WPA3-Enterprise SuiteB 192-bit** security standards.
- Hardware LTE coexistence integrates seamlessly w/ LTE modules
- Bluetooth 5.3 (Basic Rate, Enhanced Data Rate and Bluetooth Low Energy) 2MPHY.

The radio interface can be configured for operation over PCIE 2.0 (WLAN)/UART(BT) for high throughput requirements or, where reduction in power usage is a higher priority in the end solution, SDIO 3.0 (WLAN)/UART(BT).

The Summit SOM 8M Plus wireless SOM has three standard product SKUs providing different memory sizes with custom memory configuration available. Please contact Laird Connectivity Sales and Support for further information. Ordering information is listed in Table 1.

Table 1: Product ordering information

Order Model	Description
453-00070R	Module, Summit SOM 8M Plus, Quad Core CPU, 512MB LPDDR4, 8GB eMMC, Tape and Reel
453-00070C	Module, Summit SOM 8M Plus, Quad Core CPU, 512MB LPDDR4, 8GB eMMC, Cut Tape
453-00071R	Module, Summit SOM 8M Plus, Quad Core CPU, 1GB LPDDR4, 8GB eMMC, Tape and Reel
453-00071C	Module, Summit SOM 8M Plus, Quad Core CPU, 1GB LPDDR4, 8GB eMMC, Cut Tape
453-00072R	Module, Summit SOM 8M Plus, Quad Core CPU, 2GB LPDDR4, 16GB eMMC, Tape and Reel
453-00072C	Module, Summit SOM 8M Plus, Quad Core CPU, 2GB LPDDR4, 16GB eMMC, Cut Tape

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Order Model	Description
453-00070-K1	Development Kit, Summit SOM 8M Plus, Quad Core CPU, 512MB LPDDR4, 8GB eMMC
453-00071-K1	Development Kit, Summit SOM 8M Plus, Quad Core CPU, 1GB LPDDR4, 8GB eMMC
453-00072-K1	Development Kit, Summit SOM 8M Plus, Quad Core CPU, 2GB LPDDR4, 16GB eMMC
110-00770	Heat Sink, 41.5mm x 39.5mm x 22.54mm, Summit SOM 8M Plus

Note: Standard Summit SOM 8M Plus modules come blank from the factory. Please ensure your designs have a method of programming the module once installed on your main board designs. Laird Connectivity recommends placing a microSD card slot on your board designs for programming the modules. If you desire modules pre-programmed with software from our factory, please contact our sales team for pricing and to arrange a unique, orderable part number. For pre-programing modules that will need secure and encrypted boot, please contact our sales team and ask for more information on our Summit Suite Chain of Trust product offering.

3 Summit SOM 8M Plus Features Summary

The Summit SOM 8M Plus module is based on i.MX 8M Plus from NXP which offers a variety of interfaces and different memory configuration. Most of these interfaces are multiplexed and not able to be used simultaneously. Key features of Summit SOM 8M plus are described in Table 2.

Table 2: Key Features of Summit SOM 8M Plus

Feature	Description
CPU	▪ Quad Cortex®-A53 processors operation up to 1.6 GHz ▪ 32 KB L1 Instruction Cache ▪ 32 KB L1 Data Cache ▪ 512 KB unified L2 cache ▪ Cortex®-M7 core platform operating up to 800 MHz ▪ 32 KB L1 Instruction Cache ▪ 32 KB L1 Data Cache ▪ 256 KB tightly coupled memory (TCM) ▪ ARM Neon™ extension
Image Sensor Processor (ISP)	▪ 375 Mpixel/s HDR ISP supporting configurations, such as 12MP@30fps, 4kp45, or 2x 1080p80
Memory interface	▪ On module: 32-bits LPDDR4 with inline ECC (size, please refer to Table 1) ▪ On module: 8-bits eMMC 5.1 with SDR104 speed. (Size, please refer to Table 1) ▪ eMMC 5.1Flash ▪ SPI ▪ FlexSPI Flash with support for XIP (for Cortex®-M7 in low-power mode) and support for either one Octal SPI, or parallel read mode of two identical Quad SPI FLASH devices.
Graphic Processing Unit	▪ GC7000UL with OpenCL and Vulkan support ▪ 2 shaders ▪ 166 million triangles/sec ▪ 1.0 giga pixel/sec ▪ 16 GFLOPs 32-bit ▪ Supports OpenGL ES 1.1, 2.0, 3.0, OpenCL 1.2, Vulkan ▪ Core clock frequency of 1000 MHz ▪ Shader clock frequency of 1000 MHz ▪ GC520L for 2D acceleration ▪ Render target compatibility between 3D and 2D GPU (super tile status buffer)
Video Processing Unit	Video Decode ▪ 1080p60 HEVC/H.265 Main, Main 10 (up to level 5.1) ▪ 1080p60 VP9 Profile 0, 2 ▪ 1080p60 VP8

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Feature	Description
	▪ 1080p60 AVC/H.264 Baseline, Main, High decoder Video Encode ▪ 1080p60 AVC/H.264 encoder ▪ 1080p60 HEVC/H.265 encoder
Neutral Processing Unit (NPU)	2.3 TOP/s Neural Network performance ▪ Keywords detect, noise reduction, beamforming ▪ Speech recognition (i.e., Deep Speech 2) ▪ Image recognition (i.e., ResNet-50)
HDMI 2.0a Tx	HDMI 2.0a Tx supporting one display ▪ Resolutions of 720 x 480p60, 1280 x 720p60, 1920 x 1080p60, 1920 x 1080p120, 3840 x 2160p30 ▪ Pixel clock up to 297 MHz Audio support ▪ 32-channel audio output support ▪ 1 SPDIF audio eARC input support
LCDIF Display Controller	Supports up to 1920x1200p60 display per LCDIF if no more than 2 instances used simultaneously, or 2x 1080p60 + 1x 4kp30 on HDMI if all 3 instances used simultaneously. ▪ One LCDIF drives MIPI DSI, up to UWHD and WUXGA ▪ One LCDIF drives LVDS Tx, up to 1920x1080p60 ▪ One LCDIF drives HDMI Tx, up to 4kp30
MIPI Interface	4-lane MIPI DSI interface Two instances of 4-lane MIPI CSI interface and HDR ISP ▪ 2x ISP supporting 375 Mpixel/s aggregate performance and up to 3-exposure HDR processing. ▪ When one camera is used, supports up to 12MP@30fps or 4kp45 ▪ When two cameras are used, each supports up to 1080p80 ▪ Maximum resolution limited to resolutions achievable with a 250 MHz pixel clock and active pixel rate of 200 Mpixel/s with 24-bit RGB. This includes resolutions such as: – 1080 p60 – WUXGA (1920X1200) at 60 Hz – 1920x1440 at 60 Hz – WHD (2560X1080) at 60 Hz – MIPI DSI: WQHD (2560x1440) can be supported by reduced blanking mode
Audio	▪ Cadence® Tensilica® HiFi 4 DSP, operating up to 800 MHz ▪ SPDIF input and output, including a raw capture input mode ▪ Six external synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, codec/DSP, and DSD interfaces, comprising one SAI with 8 TX and 8 RX lanes, one SAI with 4 TX and 4 RX lanes, two SAI with 2 TX and 2 RX lanes, and two SAI with 1 TX and 1RX lane. ▪ All ports support 49.152 MHz BCLK. ▪ ASRC supports processing 32 audio channels, 4 context groups, 8 kHz to 384 kHz sample rate, and 1/16 to 8x sample rate conversion ratio. ▪ eARC/ARC ▪ 8-channel PDM mic input
Connectivity	▪ Two USB 3.0 Type C controllers with integrated PHY (also supported USB 2.0) interfaces ▪ Two Ultra Secure Digital Host Controller (uSDHC) interfaces ▪ Two Ethernet controllers (both capable of simultaneous operation) ▪ Two Controller Area Network (FlexCAN) modules, each optionally supporting flexible data-rate (FD) **Note:** Legacy CAN mode supports both Mailbox (MB) and RX FIFO (with DMA support) operation. Flexible Data (FD) mode supports MB operation only. There is no enhanced RX FIFO or DMA support in FD mode. ▪ Four Universal Asynchronous Receiver/Transmitter (UART) modules

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Feature	Description
	▪ Six I2C modules ▪ Three SPI modules
Security	▪ Resource Domain Controller (RDC) ▪ Arm® TrustZone® (TZ) architecture ▪ On-chip RAM (OCRAM) secure region protection using OCRAM controller ▪ High Assurance Boot (HAB) ▪ Cryptographic Acceleration and Assurance Module (CAAM) ▪ Secure Non-Volatile Storage (SNVS) ▪ Secure JTAG Controller (SJC)
Debug Interface	▪ Secure JTAG Controller (SJC) ▪ Two Debug UART port for Quad Cortex®-A53 processors and Cortex®-M7.
RF output	▪ Two RF output with U. FL connectors provide flexible of external antenna selection for optimize performance. ▪ Main antenna: Support both Wi-Fi and BT ▪ Aux Antenna: Support Wi-Fi only.
MAC address	▪ MAC address etch on the shielding cover is the first MAC address for Wi-Fi ▪ The following 3 MAC address are reserved for Wi-Fi. ▪ The BT MAC address is the etched number + 3

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4 BLOCK DIAGRAM

The figure below shows the block diagram of the Summit SOM 8M Plus which contains the NXP i.MX 8MPlus processor, PMIC (PCA9450CHN and 88PG823) and the Wi-Fi SOC 88W8997.

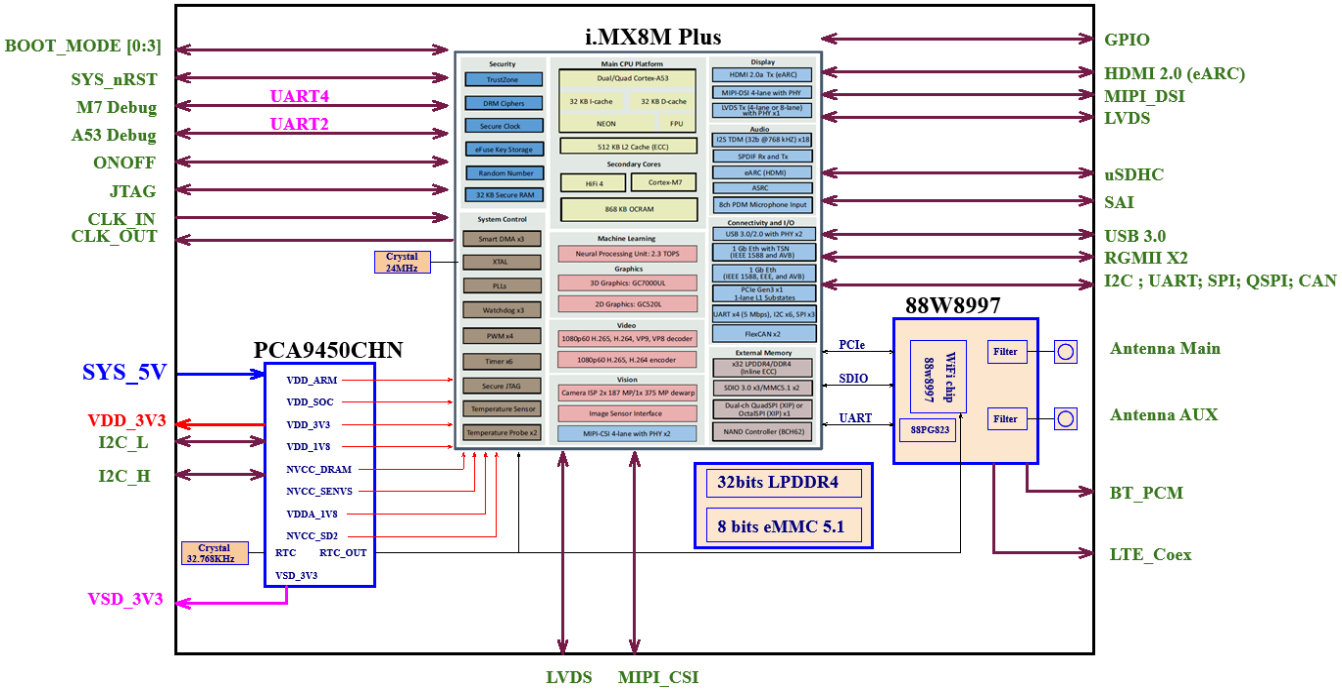

Figure 1: Block diagram of Summit SOM 8M Plus

Detailed connections between the 88W8997 and the I.MX8M plus are detailed in below table.

Table 3: 88W8997 to i.MX 8MN Plus Connections

	88W8997	i.MX8M Plus
SDIO	SD_CLK/SD_CMD/SD_DATA0-3	SD1_CLK/SD1_CMD/SD1_DATA0-3
PCIe	PCIE_RCLK_P/PCIE_RCLK_N/PCIE_TX_P/PCIE_TX_N/ PCIE_RX_P/PCIE_RX_N/PCIE_WAKEn/PCIE_CLKREQn/ PCIE_W_DISABLEn/PCIE_PERSTn	PCIE_REF_PAD_CLK_P/PCIE_REF_PAD_CLK_N/PCIE_RXN_P/ PCIE_RXN_N/PCIE_TXN_P/PCIE_TXN_N/I2C4_SDA/I2C4_SCL/ SD1_DATA5/SD1_DATA4
UART	UART_SOUT/UART_SIN/UART_CTSn/UART_RTSn	ECSPI1_SCLK/ECSPI1_MOSI/ECSPI1_MISO/ECSPI1_SS0
WoW	GPIO[0]	NAND_DQS
WoBT	GPIO[3]	SD1_STROBE
Wi-Fi BS	CONFIG_HOST[0]	SD1_DATA6
Wi-Fi BS	CONFIG_HOST[1]	SD1_DATA7

Note: CONFIG_HOST[2] is 49.9K to ground.

CONFIG_HOST[2-0]=”0,0,0” for SDIO (Wi-Fi) and UART (BT); CONFIG_HOST[2-0]=”0,1,10” for PCIE (Wi-Fi) and UART (BT).

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5 DC Power Tree

The Summit SOM 8M Plus requires a primary 5V power supply (VSYS_5V) input. This supply is the main power domain to the on-module NXP PCA9450CHN power management IC (PMIC), which generates all required supply voltages for the module components. The PMIC has 32.768KHz crystal oscillator and buffer built-in which generates the real-time clock (RTC) for the NXP processor and Wi-Fi radio.

The PMIC generates the following power domains that are available on the following SOM module pads:

- VDD_3V3
- VSD_3V3

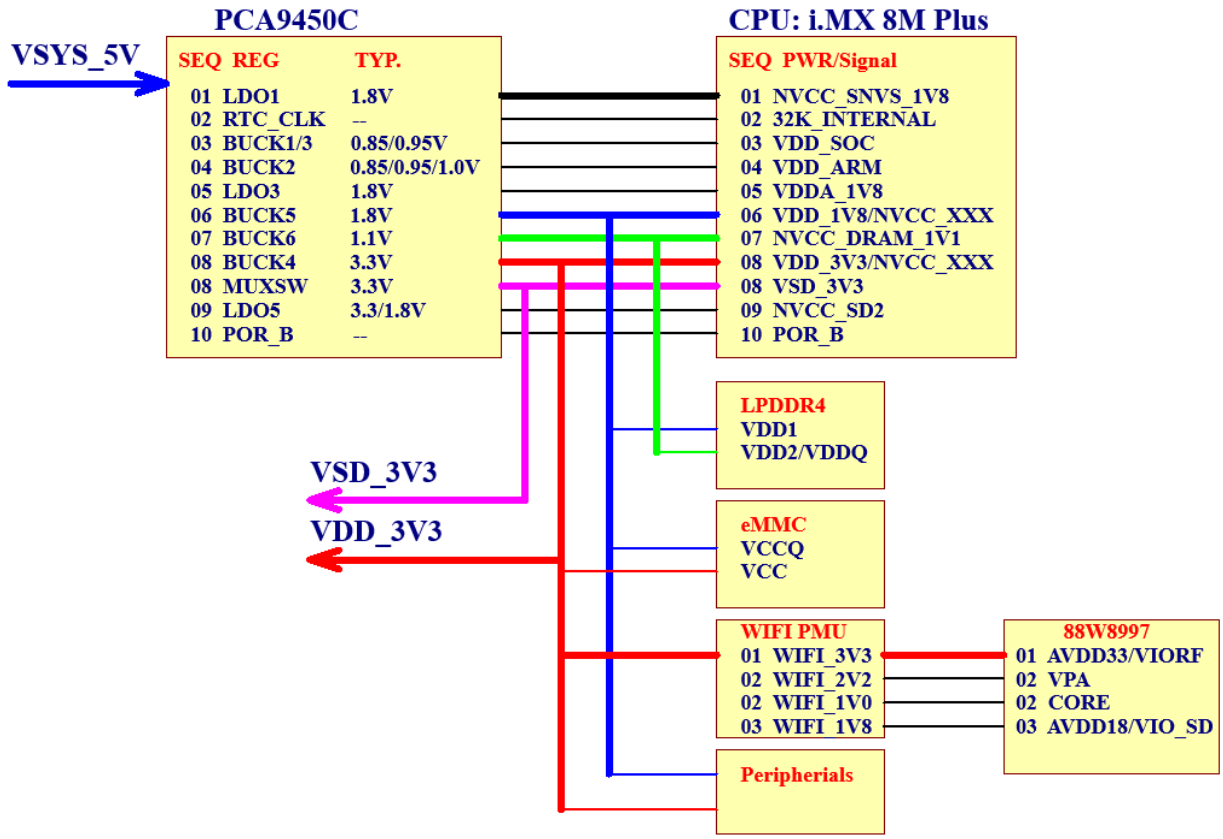

Figure 2: DC power tree of Summit SOM 8M Plus

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5.1 Power Modes Diagram

NXP PCA9450CHN has eight power modes: OFF, READY, SNVS, RUN, STANDBY, PWRDN, PWRUP and FAULT_SD. Below figure shows the state transition diagram showing the conditions to enter and exit each state.

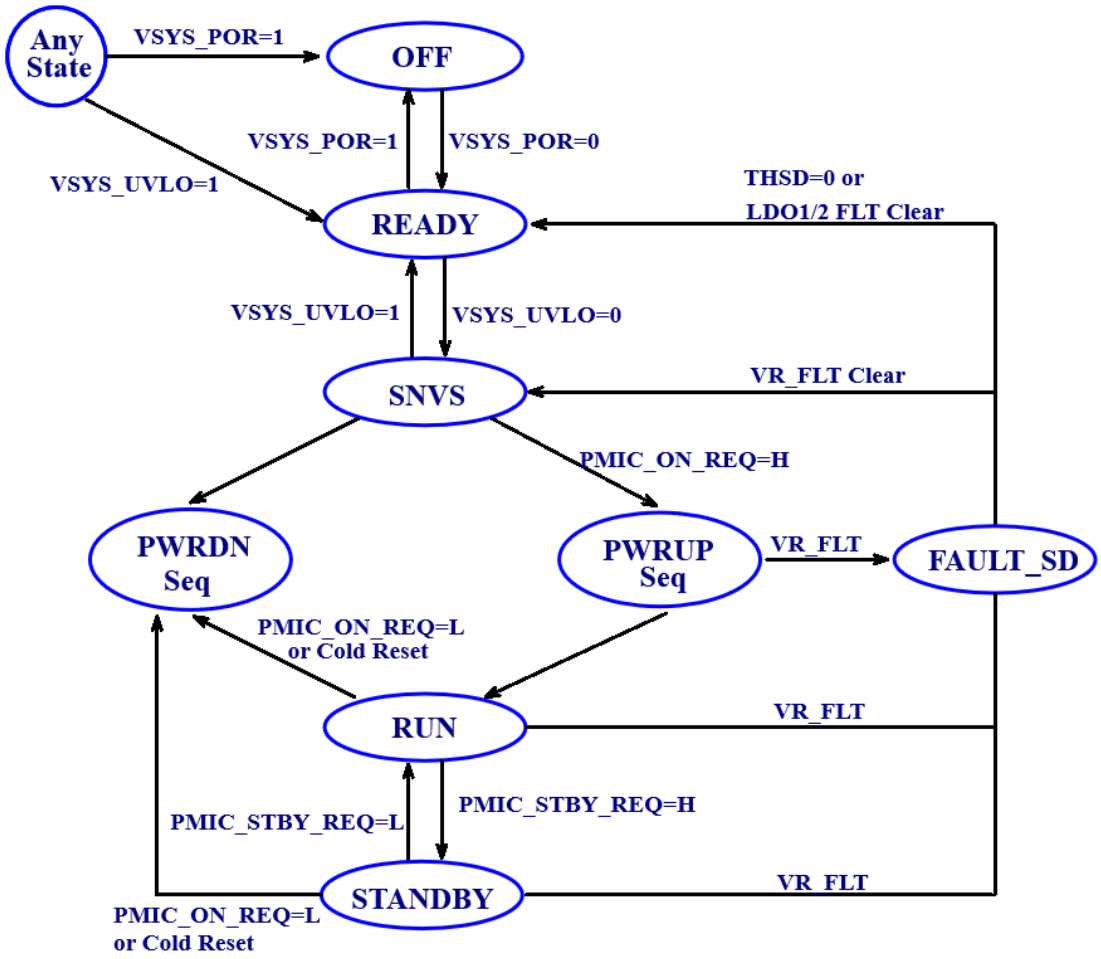

Figure 3: State transition diagram for PMIC

- **OFF mode:**
  PMIC will enter OFF mode from any state when the main power source VSYS_5V falls below V_{sys_POR} threshold (2.2 to 2.6V; typ.=2.4V). All regulators are OFF and all registers are reset in this mode.
- **READY Mode:**
  PMIC enters READY mode when VSYSY_5V is higher than V_{sys_POR}. The internal LDO VINT is enabled and loads the MTP data to registers. Once the MTP data loading is complete, the state machine is ready to transition to SNVS mode.
- **SNVS Mode:**
  PMIC will enter SNVS (Secure Non-Volatile Storage mode) when VSYS_5V exceeds the V_{sys_UVLO} threshold. LDO1 is powered up and the 32.778KHz buffer starts running. RTC_RESET_B is pulled high after both LDO1 and LDO2 voltage come up.

Note: PMIC_ON_REQ input is masked until RTC_RESET_B is released. PMIC will start power up sequence if PMIC_ON_REQ is asserted high in this mode.

- **PWRUP Mode:**
  After RTC_RESET_B is released in SNVS mode, the PMIC starts power up with a pre-defined sequence with PMIC_ON_REQ asserted high.

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During PWRUP mode, PMIC_STBY_REQ signal is masked until POR_B is released. The PWRUP mode ends up releasing POR_B and the PMIC is transitioned to RUN mode.

- **PWRDN Mode:**
  When PMIC_ON_REQ is low in RUN or STANDBY mode, PMIC enters PWRDN mode, where it starts with pulling down POR_B. and then by turning off each power rail before transitioning to SNVS mode.
- **RUN Mode:**
  PMIC operates in RUN mode when PMIC_ON_REQ is driven high and PMIC_STBY_REQ is driven low. When PMIC_STBY_REQ is asserted high in this mode, it is transitioned to STANDBY mode. PMIC_ON_REQ is asserted low, it moves to PWRDN mode.
- **STANDBY Mode:**
  PMIC is transitioned to STANDBY mode from RUN mode when both PMIC_ON_REQ and PMIC_STBY_REQ are driven low. If PMIC_ON_REQ is asserted low, then it is transitioned to PWRDN mode. If PMIC_STBY_REQ is driven low, it is transitioned to RUN mode.

Power Mode	VSYS_5V	PMIC_ON_REQ	PMIC_STBY_REQ
OFF	VSYS_5V<V_{SYS_POR}	x	x
READY	VSYS_5V>V_{SYS_POR}	x	x
SNVS	VSYS_5V>V_{SYS_UVLO}	LOW	x
STANDBY	VSYS_5V>V_{SYS_UVLO}	HIGH	HIGH
RUN	VSYS_5V>V_{SYS_UVLO}	HIGH	LOW

- **FAULT_SD Mode:**
  PCA9450CHN has three kinds of Fault sources.
  - **Thermal shutdown**: Transition to SNVS mode or READY mode after Fault_SD mode.
    When junction temperature reach to 150℃, it enters FAULT_SD mode after 120 μ s where regulators are tuned off simultaneously. It stays at FAULT_SD mode until the junction temperature fall below 150℃, then move to READY state if any of LDO1 and LDO2 is fault is triggered. And it will move to SNVS mode if either LDO1 or LDO2 fault is triggered.
  - **Voltage regulator fault during power up:** Transition to READY mode after FAULT_SD mode.
    Any POK of voltage regulator doesn't come up within 10ms after regulator is enabled during power up sequence, it stops power-up sequence and then moves into FAULT_SD mode where all regulators are turned off.
  - **Voltage regulator fault in STBY and RUN MODE:** Move to FAULT_SD mode in 100ms after fault is detected. Transition to SNVS mode or READY mode after FAULT_SD mode.

6 BOOTSTRAP

The Summit SOM 8M Plus module can be configured to boot from a different interface by selecting the BOOT_Mode [3-0]. These bits are latched externally during boot-up.

BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	BOOT MODE
0	0	0	0	Boot from Internal Fuses
0	0	0	1	USB Serial Download
0	0	1	0	uSDHC3 (eMMC boot only, SD3 8-bit) Default.
0	0	1	1	uSDHC2 (SD boot, SD2)
0	1	0	0	NAND 8-bit single device 256 pages.
0	1	0	1	NAND 8-bit single device 512 pages
0	1	1	0	QSPI 3B Read
0	1	1	1	QSPI Hyperflash 3.3V
1	0	0	0	ECSPI Boot
1	0	0	1	Reserved
1	0	1	0	Reserved
1	0	1	1	Reserved

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BOOT_MODE3	BOOT_MODE2	BOOT_MODE1	BOOT_MODE0	BOOT MODE
1	1	0	0	Reserved (Boot on I2C connected to BOOT PIN[3:2]
1	1	0	1	Reserved
1	1	1	0	Infinite Loop Mode
1	1	1	1	Test Mode

Caution: BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3, JTAG_MOD and POR_B must be pulled to "111111" for i.MX8M Plus to enter Boundary Scan Mode.

7 WIRELESS INTERFACE

The Summit SOM 8M Plus module supports IEEE 802.11 a/b/g/n/ac WLAN, 2x2 MIMO combo solution with support for Bluetooth 5.3 with 2Mbps LE. The following sections details the specifications for the wireless interface available on this SOM module.

Wi-Fi on the Summit SOM 8M Plus module supports 20/40MHz bandwidth when operated at 2.4GHz and 20/40/80 MHz bandwidth when operated at 5GHz band.

Bluetooth supports both basic rate, enhanced data rate and Bluetooth low energy.

- **Wi-Fi and Bluetooth Modulation and data rate:**
  2.4GHz: 11b, 11g, 11n (HT20, HT40).
  5GHz: 11a, 11n (HT20, HT40), 11 ac (HT20, HT40, HT80)

Wi-Fi Mode	Modulation	Coding	Rate
802.11b	DBPSK	-	1
	DQPSK	-	2
	CCK	-	5.5
	CCK	-	11
802.11ag	BPSK	1/2	6
	BPSK	3/4	9
	QPSK	1/2	12
	QPSK	3/4	18
	16QAM	1/2	24
	16QAM	3/4	36
	64QAM	2/3	48
	64QAM	3/4	54

Bluetooth Mode	Modulation	Rate
Basic Rate (BR)	GFSK	DH1/DH3/DH5
Enhanced Data Rate (EDR)	GFSK π/4-DPSK GFSK 8-DPSK	2DH1/2DH3/2DH5 3DH1/3DH3/3DH5
Bluetooth Low Energy (BLE)	GFSK LE 1M GFSK LE 2M	1M 2M

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Table 4: Wi-Fi 11n/11ac data rates

802.11ac / 802.11n	HT MCS Index	VHT MCS Index	Spatial Streams	Modu.	Coding	20 MHz		40 MHz		80 MHz	
						No SGI	SGI	No SGI	SGI	No SGI	SGI
	0	0	1	BPSK	1/2	6.5	7.2	13.5	15	29.3	32.5
	1	1	1	QPSK	1/2	13	14.4	27	30	58.5	65
	2	2	1	QPSK	3/4	19.5	21.7	40.5	45	87.8	97.5
	3	3	1	16-QAM	1/2	26	28.9	54	60	117	130
	4	4	1	16-QAM	3/4	39	43.3	81	90	175.5	195
	5	5	1	64-QAM	2/3	52	57.8	108	120	234	260
	6	6	1	64-QAM	3/4	58.5	65	121.5	135	263.3	292.5
	7	7	1	64-QAM	5/6	65	72.2	135	150	292.5	325
		8	1	256-QAM	3/4	78	86.7	162	180	351	390
		9	1	256-QAM	5/6	N/A	N/A	180	200	390	433.3
	8	0	2	BPSK	1/2	13	14.4	27	30	58.5	65
	9	1	2	QPSK	1/2	26	28.9	54	60	117	130
	10	2	2	QPSK	3/4	39	43.3	81	90	175.5	195
	11	3	2	16-QAM	1/2	52	57.8	108	120	234	260
	12	4	2	16-QAM	3/4	78	86.7	162	180	351	390
	13	5	2	64-QAM	2/3	104	115.6	216	240	468	520
	14	6	2	64-QAM	3/4	117	130.3	243	270	526.5	585
	15	7	2	64-QAM	5/6	130	144.4	270	300	585	650
		8	2	256-QAM	3/4	156	173.3	324	360	702	180
		9	2	256-QAM	5/6	N/A	N/A	360	400	780	866.7

Data rate (Mbps), SGI (Short Guard Interval), No SGI (Non-Short Guard Interval)

Table 5: Wi-Fi RF Channels

RF band	Channel Bandwidth	Channel Spacing	Channel Number (Center Frequency MHz)
2.4GHz	20MHz	5MHz	**1**(2412), **2**(2417), **3**(2422), **4**(2427), **5**(2432), **6**(2437), **7**(2442), **8**(2447), **9**(2452), **10**(2457), **11**(2462), **12**(2467), **13**(2472), **14**(2448)
	40MHz	5MHz	**3**(2442), **11**(2462)
5GHz	20MHz	20MHz	**36**(5180), **40**(5200), **44**(5220), **48**(5240), **52**(5260), **56**(5280), **60**(5300), **64**(5320), **100**(5500), **104**(5520), **108**(5540), **112**(5560), **116**(5580), **120**(5600), **124**(5620), **128**(5640), **132**(5660), **136**(5680), **140**(5700), **144**(5720), **149**(5745, **153**(5765), **157**(5785), **161**(5805), **165**(5825)
	40MHz	40MHz	**38**(5190), **46**(5230), **54**(5270), **62**(5310), **102**(5510), **110**(5550), **118**(5590), **126**(5630), **134**(5670), **142**(5710), **151**(5755), **159**(5795),
	80MHz	80MHz	**42**(5210), **58**(5290), **106**(5530), **122**(5610), **138**(5690), **155**(5775),

Note: Available RF channels and their maximum transmit power are detailed in Laird Connectivity's Regulatory Utility (LRU). Please contact Laird Connectivity for updated information.

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	2.4GHz				5GHz					
					UNII-1	UNII-2	UNII-2-EXT		UNII-3	ISM
Reg. Domain	1-11	12	13	14	36-48	52-64	100-140	144	149-161	165
FCC	✔	**NO**	**NO**	**NO**	✔	✔**(DFS)**	✔**(DFS)**	✔**(DFS)**	✔	✔
ETSI	✔	✔	✔	**NO**	✔	✔**(DFS)**	✔**(DFS)**	**NO**	✔**(SRD)**	✔**(SRD)**
MIC	✔	✔	✔	✔**(11b)**	✔	✔**(DFS)**	✔**(DFS)**	**NO**	**NO**	**NO**
KC	✔	✔	✔	**NO**	✔	✔**(DFS)**	✔**(DFS)**	✔**(DFS)**	✔	✔

Note: DFS: Dynamic Frequency Selection
SRD: Short Range Device (25mW max power)
For countries not listed above, please contact Laird Connectivity for the updated regulatory certification status for WW country.

Table 6: RF Performance

Wi-Fi RF performance	**Condition**			**Typical values AVG with No GAP**	**Note:**
	Mode	Bandwidth	Rate		
Transmit power	802.11b	20MHz	1-11 Mbps	18dBm (63mW)	✣ Power values are “conductive power” which measured at each RF output port. ✣ HT20: 20 MHz-wide channels HT40: 40 MHz-wide channels HT80: 80 MHz-wide channels ✣ Tolerance is +/-2dB at room temperature and is extended to +/-2.5dB across operating temperature. ✣ The transmit power on each channel varies per individual country regulations. Please contact Laird Connectivity for the power table of each individual country.
	802.11g	20MHz	6-36 Mbps	18dBm (63mW)	
		20MHz	48-54 Mbps	16dBm (40mW	
	802.11a	20MHz	6-36 Mbps	18dBm (63mW)	
		20MHz	48-54 Mbps	16dBm (40mW	
	802.11n (2G/5G)	20MHz HT20	MCS0-4; MCS8-12 MCS5-7; MCS13-15	18dBm (63mW) 16dBm (40mW)	
		40MHz HT40	MCS0-4; MCS8-12 MCS5-7; MCS13-15	16dBm (40mW) 14dBm (25mW)	
	802.11ac (5G)	20MHz VHT20	MCS0-7 MCS8	18dBm (63mW) **15dBm** (31.6mW)	
		40MHz VHT40	MCS0-7 MCS8-9	16dBm (40mW) **12dBm** (15.8mW)	
		80MHz VHT80	MCS0-7 MCS8-9	12dBm (15.8mW) **9dBm** (10mW)	

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Bluetooth RF performance	Condition		Typical Values (dBm)	Note
	Mode	Rate		
Transmit Power	BR	DH1/DH3/DH5	7dBm (6.3mW)	✤ Tolerance is +/-2dB at room temperature and is extended to +/-2.5dB across operating temperature. ✤ CH0/CH78 (BR&EDR) and CH0/CH39 (LE) typical values will be 1 to 1.5dB lower than the other channels due to built-in BAW filter on the SOM module for LTE coex.
	EDR	2DH1/2DH3/2DH5 3DH1/3DH3/3DH5	7dBm (6.3mW)	
	LE	1M/2M	6.5dBm (4.4mW)	

Wi-Fi RF performance	Condition with PER<10%			Values (dBm)		Note:
	Mode	Bandwidth	Rate	Typ.	Max.	
Receiver sensitivity	802.11b	20MHz	1 Mbps (PER<8%)	-95	-92	✤ Sensitivity values are measured at each RF port through conductive measurement. ✤ 2.4GHz CH13 typical values will be 4-6dB worse compared to the other channels.
		20MHz	11 Mbps (PER<8%)	-90	-87	
	802.11g	20MHz	6 Mbps	-91	-88	
		20MHz	54 Mbps	-75	-72	
	802.11a	20MHz	6 Mbps	-89	-86	
		20MHz	54 Mbps	-74	-71	
	802.11n (2G)	20MHz HT20	MCS0-4; MCS8-12 MCS5-7; MCS13-15	-91 -73	-88 -70	
	802.11n (5G)	20MHz HT20	MCS0-4; MCS8-12 MCS5-7; MCS13-15	-89 -70	-86 -67	
	802.11n (2G)	40MHz HT40	MCS0-4; MCS8-12 MCS5-7; MCS13-15	-85 -70	-82 -67	
	802.11n (5G)	40MHz HT40	MCS0-4; MCS8-12 MCS5-7; MCS13-15	-86 -69	-83 -66	
	802.11ac (5G)	20MHz VHT20	MCS0-7 MCS8	-89 -67	-86 -64	
		40MHz VHT40	MCS0-7 MCS8-9	-86 -63	-83 -60	
		80MHz VHT20	MCS0-7 MCS8-9	-81 -55	-78 -52	

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Bluetooth RF performance	Condition		Values (dBm)		Note
	Mode	Rate	Typ.	Max	
Receiver sensitivity	BR	DH1/DH3/DH5	-95	-92	✤ Sensitivity definition: BER: BR<0.1%; EDR<0.01% PER: LE<30.8% ✤ Typical values of CH78 (BR/EDR) and CH39 (LE) will be 4-6dB worse compared to the other channels.
	EDR	2DH1/2DH3/2DH5	-94	-91	
		3DH1/3DH3/3DH5	-88	-85	
	LE	1M	-98	-95	
		2M	-95	-92	

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8 Electrical Characteristic and Power Consumption

8.1 Absolute Maximum Ratings

Table 2 summarizes the absolute maximum ratings and Table 3 lists the recommended operating conditions for the Summit SOM 8M Plus product series. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 2: Absolute maximum ratings

Symbol (Domain)	Parameter	Min.	Max	Unit
VSYS_5V	Input voltage for the SOM	-0.5	+6.0	V
I/O Input/output voltage range	Any I/O pin referred to VDD_1V8; VDDA_1V8; WI-FI_1V8; NVCC_SNVS_1V8	-0.3	+2.1	V
I/O Input/output voltage range	Any I/O pin referred to VDD_3V3; VSD_3V3; NVCC_SD2	-0.3	+3.6	V
$T_{STORAGE}$	Storage Temperature Range	-40	+125	°C
ANT0; ANT1	Maximum RF input (reference to 50-Ω input)	NA	+10	dBm
ESD	Electrostatic discharge tolerance	-2000	+2000	V

8.2 Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
VSYS_5V	Input voltage for the SOM	2.7	5.0	5.5	V
I/O Input/output voltage range	Any I/O pin referred to VDD_1V8; VDDA_1V8; WI-FI_1V8; NVCC_SNVS_1V8	1.71	1.8	1.89	V
I/O Input/output voltage range	Any I/O pin referred to VDD_3V3; VSD_3V3; NVCC_SD2	3.0	3.3	3.6	V
T-ambient	Operating Ambient temperature	-40	25	85	°C

Note: The operating ambient temperature ratings are highly dependent on the design-case, such as the enclosure design, system design, processor activity, GPU/VPU activity, and peripherals used.

Running over 70° C ambient temperature typically requires the implementation of thermal management strategies such as passive (heatsink/spreader). Please contact Laird Connectivity if you need information and guidance for thermal management.

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8.3 DC current consumption

The following table shows the current consumption of continuous transmit mode

Mode	Rate	CPU loading	TX power	Current (A)		
				Min.	Avg.	Max.
11b	1Mbps	100%	20dBm	1.17	1.25	1.4
		50%		1.01	1.15	1.41
		25%		1.01	1.1	1.41
	11Mbps	100%	20dBm	1.18	1.28	1.42
		50%		1.04	1.18	1.44
		25%		1.04	1.12	1.43
11g	6Mbps	100%	20dBm	1.13	1.22	1.35
		50%		0.968	1.12	1.39
		25%		0.967	1.06	1.37
	54Mbps	100%	18dBm	1	1.11	1.27
		50%		0.871	1.01	1.28
		25%		0.87	0.954	1.3
11gn (HT20)	MCS0	100%	20dBm	1.15	1.24	1.38
		50%		0.995	1.14	1.4
		25%		0.994	1.08	1.42
	MCS7	100%	18dBm	1.02	1.12	1.31
		50%		0.877	1.02	1.27
		25%		0.875	0.971	1.28
	MCS8	100%	20dBm	1.14	1.24	1.42
		50%		0.998	1.14	1.38
		25%		0.998	1.08	1.41
	MCS15	100%	18dBm	1.02	1.13	1.28
		50%		0.884	1.02	1.27
		25%		0.882	0.968	1.27
11gn (HT40)	MCS0	100%	18dBm	1.04	1.13	1.28
		50%		0.887	1.03	1.28
		25%		0.887	0.969	1.32
	MCS7	100%	16dBm	0.939	1.04	1.2
		50%		0.798	0.941	1.19
		25%		0.797	0.89	1.2
	MCS8	100%	18dBm	1.03	1.14	1.29
		50%		0.895	1.03	1.27
		25%		0.892	0.981	1.28
	MCS15	100%	16dBm	0.947	1.04	1.19

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Mode	Rate	CPU loading	TX power	Current (A)		
				Min.	Avg.	Max.
		50%		0.801	0.941	1.18
		25%		0.8	0.885	1.23
11a	6Mbps	100%	20dBm	1.28	1.4	1.56
		50%		1.13	1.29	1.57
		25%		1.13	1.23	1.55
	54Mbps	100%	18dBm	1.17	1.29	1.42
		50%		1.03	1.18	1.46
		25%		1.03	1.12	1.45
11an (HT20)	MCS0	100%	20dBm	1.35	1.42	1.55
		50%		1.16	1.3	1.58
		25%		1.16	1.25	1.55
	MCS7	100%	18dBm	1.2	1.3	1.45
		50%		1.04	1.19	1.46
		25%		1.04	1.13	1.44
	MCS8	100%	20dBm	1.32	1.43	1.59
		50%		1.16	1.31	1.6
		25%		1.16	1.26	1.58
	MCS15	100%	18dBm	1.2	1.31	1.45
		50%		0.948	1.08	1.38
		25%		1.04	1.14	1.45
11an (HT40)	MCS0	100%	18dBm	1.19	1.31	1.45
		50%		1.05	1.19	1.48
		25%		1.05	1.14	1.49
	MCS7	100%	16dBm	1.09	1.2	1.35
		50%		0.944	1.09	1.38
		25%		0.943	1.03	1.36
	MCS8	100%	18dBm	1.2	1.32	1.48
		50%		1.05	1.2	1.49
		25%		1.06	1.15	1.47
	MCS15	100%	16dBm	1.11	1.2	1.33
		50%		0.948	1.08	1.38
		25%		0.948	1.03	1.35
11ac (VHT20)	MCS0	100%	20dBm	1.31	1.43	1.56
		50%		1.16	1.31	1.59
		25%		1.16	1.26	1.58
	MCS8	100%	18dBm	1.19	1.3	1.47

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Mode	Rate	CPU loading	TX power	Current (A)		
				Min.	Avg.	Max.
		50%		1.04	1.19	1.47
		25%		1.04	1.13	1.48
11ac (VHT40)	MCS0	100%	18dBm	1.22	1.31	1.46
		50%		1.06	1.2	1.46
		25%		1.06	1.14	1.48
	MCS9	100%	14dBm	1.02	1.11	1.26
		50%		0.862	1	1.28
		25%		0.859	0.948	1.25
11ac (VHT80)	MCS0	100%	16dBm	1.15	1.23	1.36
		50%		0.978	1.11	1.41
		25%		0.978	1.06	1.39
	MCS9	100%	12dBm	0.971	1.06	1.17
		50%		0.819	0.957	1.24
		25%		0.819	0.907	1.24

Several power saving modes are available and are listed in the table below.

Mode	Description	Current (Avg)
Power Saving mode	CPU is on, Stay on Wi-Fi connection only.	431mA
RAM suspend mode	CPU is on, memory and wireless connection are off.	7.7mA
Linux graceful power down mode	All circuits are off. Only the NVCC_SNVS_1V8 PMU is alive and ONOFF pin is accessible to allow turn on of the SOM.	154uA

9 Module Pin Out and PIN-MUX Table

Table 7 lists the pin multiplexing (PIN-MUX) of the Summit SOM 8M Plus. Most of the pin names on the SOM are same as the pin names of the connected NXP processor. The "Pin Number " column shows the relationship of the SOM pin number to the NXP processor pin number.

PO = Power Output, PI = Power Input, DI = Digital Input, DO = Digital Output, DIO = Bi-directional Digital Port, GND = Ground

NXP process has configurable internal Pull-up (PU) and pull-down (PD) resistor whose values are listed below. During a reset condition, the PU and PD state are pre-defined and cannot be changed.

Table 7: Resistor characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Pull-up (PU) resistor	VDD=1.65 to 1.95V Temp=0 to 95℃	12	22	49	kΩ
Pull-down (PD) resistor		13	23	48	kΩ
Pull-up (PU) resistor	VDD=3.0 to 3.6V Temp=0 to 95℃	18	37	72	kΩ
Pull-down (PD) resistor		24	43	87	kΩ

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Pin configuration for the i.MX is achieved using a suite of evaluation and configuration tools that assists users from initial evaluation to production software development. Users can download the tool from the NXP website: https://www.nxp.com/design/designs/config-tools-for-i-mx-applications-processors:CONFIG-TOOLS-IMX?tab=Design_Tools_Tab

Table 4: Pin-Mux table for Summit SOM 8M Plus

Pin Number		SOM/Processor Pin name	PIN Multiplexing	I/O	Power group	Comments
SOM	CPU					
A1	AE12	SAI1_MCLK	**GPIO:** GPIO4_IO20 **SAI:** SAI1_MCLK/ SAI5_MCLK SAI1_TX_BCLK **ENET1:**ENET1_TX_CLK	DIO	VDD_1V8	**At reset Condition**: Input with PD
A2	-	GND	NA	-	NA	
A3	-	GND	NA	-	NA	
A4	AH8	SAI1_RXC	**GPIO:** GPIO4_IO1 **SAI:** SAI1_RX_BCLK/ SAI5_RX_BCLK **PDM:** PDM_CLK **ENET1:** ENET1_1588_EVENT0_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD
A5	AJ9	SAI1_RXFS	**GPIO:** GPIO4_IO0 **SAI:** SAI1_RX_SYNC/SAI5_RX_SYNC **ENET1:** ENET1_1588_EVENT0_IN	DIO	VDD_1V8	**At reset Condition:** Input with PD
A6	AH12	SAI1_RXD7	**GPIO:** GPIO4_IO9 **SAI:** SAI1_RX_DATA7/ SAI1_TX_DATA4 SAI1_TX_SYNC/ SAI6_MCLK **ENET1:** ENET1_RGMII_RD3	DIO	VDD_1V8	**At reset Condition:** Input with PD
A7	AH10	SAI1_RXD6	**GPIO:** GPIO4_IO8 **SAI:** SAI1_RX_DATA6/ SAI6_RX_SYNC SAI6_TX_SYNC **ENET1:** ENET1_RGMII_RD2	DIO	VDD_1V8	**At reset Condition:** Input with PD
A8	AE10	SAI1_RXD5	**GPIO:** GPIO4_IO7 **SAI:** SAI1_RX_DATA5/ SAI1_RX_SYNC SAI6_RX_DATA0/ SAI6_TX_DATA0 **ENET1:** ENET1_RGMII_RD1	DIO	VDD_1V8	**At reset Condition:** Input with PD
A9	AD10	SAI1_RXD4	**GPIO:** GPIO4_IO6 **SAI:** SAI1_RX_DATA4/ SAI6_RX_BCLK SAI6_TX_BCLK **ENET1:** ENET1_RGMII_RD0	DIO	VDD_1V8	**At reset Condition:** Input with PD
A10	AJ8	SAI1_RXD3	**GPIO:** GPIO4_IO5 **SAI:** SAI1_RX_DATA3/ SAI5_RX_DATA3 **PDM:** PDM_BIT_STREAM3 **ENET1:** ENET1_MDIO	DIO	VDD_1V8	**At reset Condition:** Input with PD
A11	AH9	SAI1_RXD2	**GPIO:** GPIO4_IO4 **SAI:** SAI1_RX_DATA2/ SAI5_RX_DATA2 **PDM:** PDM_BIT_STREAM2 **ENET1:** ENET1_MDC	DIO	VDD_1V8	**At reset Condition:** Input with PD
A12	AF10	SAI1_RXD1	**GPIO:** GPIO4_IO3 **SAI:**	DIO	VDD_1V8	**At reset Condition:** Input with PD

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Pin Number SOM	Pin Number CPU	SOM/Processor Pin name	PIN Multiplexing	I/O	Power group	Comments
			SAI1_RX_DATA1/ SAI5_RX_DATA1 **PDM:** PDM_BIT_STREAM1 **ENET1:** ENET1_1588_EVENT1_OUT			
A13	AC10	SAI1_RXD0	**GPIO:** GPIO4_IO2 **SAI:** SAI1_RX_DATA0/ SAI1_TX_DATA1 SAI5_RX_DATA0 **PDM:** PDM_BIT_STREAM0 **ENET1:** ENET1_1588_EVENT1_IN	DIO	VDD_1V8	**At reset Condition:** Input with PD
A14	**-**	**GND**	**NA**	**-**	**NA**	
A15	**-**	**SYS_nRST**	**NA**	DI	NVCC_SNVS_1V8	PMIC reset input pin. **Note:** **Internally 100KΩ pulled up to NVCC_SNVS_1V8. Once it is asserted low, PMIC performs reset.**
A16	**-**	**GND**	**NA**	**-**	**NA**	
A17	AH7	I2C1_SDA	**GPIO:** GPIO5_IO15 **I2C:** I2C1_SDA **ENET_QOS:** ENET_QOS_MDIO **ECSPI:** ECSPI1_MOSI	DIO	VDD_1V8	**At reset Condition:** Input with PD
A18	AJ7	I2C3_SCL	**GPIO:** GPIO5_IO18 **I2C:** I2C3_SCL **ECSPI:** ECSPI2_SCLK **PWM:** PWM4_OUT **GPT:** GPT2_CLK	DIO	VDD_1V8	**At reset Condition:** Input with PD
A19	AH6	I2C2_SCL	**GPIO:** GPIO5_IO16 **uSDHC:** uSDHC3_CD_B **I2C:** I2C2_SCL **ENET_QOS:** ENET_QOS_1588_EVENT1_AUX_IN ENET_QOS_1588_EVENT1_IN **ECSPI:** ECSPI1_MISO	DIO	VDD_1V8	**At reset Condition:** Input with PD
A20	AC8	I2C1_SCL	**GPIO:** GPIO5_IO14 **I2C:** I2C1_SCL **ENET_QOS:** ENET_QOS_MDC **ECSPI:** ECSPI1_SCLK	DIO	VDD_1V8	**At reset Condition:** Input with PD
A21	AJ6	I2C3_SDA	**GPIO:** GPIO5_IO19 **I2C:** I2C3_SDA **ECSPI:** ECSPI2_MOSI **PWM:** PWM3_OUT **GPT:** GPT3_CLK	DIO	VDD_1V8	**At reset Condition:** Input with PD
A22	AE8	I2C2_SDA	**GPIO:** GPIO5_IO17 **uSDHC:** uSDHC3_WP **I2C:** I2C2_SDA **ENET_QOS:** ENET_QOS_1588_EVENT1_OUT **ECSPI:** ECSPI1_SS0	DIO	VDD_1V8	**At reset Condition:** Input with PD
A23	**-**	**GND**	**NA**	**-**	**NA**	
A24	**-**	**GND**	**NA**	**-**	**NA**	

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Pin Number		SOM/Processor Pin name	PIN Multiplexing	I/O	Power group	Comments
SOM	CPU					
A25	-	GND	NA	-	NA	
A26	AH5	UART4_TXD	**GPIO:** GPIO5_IO29 **I2C:** I2C6_SDA **UART:** UART2_RTS_B/UART4_TX **GPT:** GPT1_CAPTURE1	DIO	VDD_1V8	**At reset Condition:** Input with PD
A27	AJ5	UART4_RXD	**GPIO:** GPIO5_IO28 **I2C:** I2C6_SCL **UART:** UART2_CTS_B/UART4_RX **GPT:** GPT1_COMPARE1 **PCIE:** PCIE1_CLKREQ_B	DIO	VDD_1V8	**At reset Condition:** Input with PD
A28	AJ4	UART3_TXD	**GPIO:** GPIO5_IO27 **uSDHC:** uSDHC3_VSELECT **UART:** UART1_RTS_B/UART3_TX **CAN:** CAN2_RX **GPT:** GPT1_CLK	DIO	VDD_1V8	**At reset Condition:** Input with PD
A29	AD6	UART1_RXD	**GPIO:** GPIO5_IO22 **UART:** UART1_RX **ECSPI:** ECSPI3_SCLK	DIO	VDD_1V8	**At reset Condition:** Input with PD
A30	AH4	UART2_TXD	**GPIO:** GPIO5_IO25 **UART:** UART2_TX **ECSPI:** ECSPI3_SS0 **GPT:** GPT1_COMPARE2	DIO	VDD_1V8	**At reset Condition:** Input with PD
A31	AE6	UART3_RXD	**GPIO:** GPIO5_IO26 **uSDHC:** uSDHC3_RESET_B **UART:** UART1_CTS_B/UART3_RX **CAN:** CAN2_TX **GPT:** GPT1_CAPTURE2	DIO	VDD_1V8	**At reset Condition:** Input with PD
A32	AJ3	UART1_TXD	**GPIO:** GPIO5_IO23 **UART:** UART1_TXD **ECSPI:** ECSPI3_MOSI	DIO	VDD_1V8	**At reset Condition:** Input with PD
A33	AF6	UART2_RXD	**GPIO:** GPIO5_IO24 **UART:** UART2_ _RX **ECSPI:** ECSPI3_MISO **GPT:** GPT1_COMPARE3	DIO	VDD_1V8	**At reset Condition:** Input with PD
A34-A51	-	GND	NA	-	NA	
A52	A4	GPIO1_IO14	**GPIO:** GPIO1_IO14 **uSDHC:** uSDHC3_CD_B **USB:** USB2_OTG_PWR **PWM:** PWM3_OUT **CCM:** CCM_CLKO1	DIO	VDD_1V8	**At reset Condition:** Input with PD
A53	B4	GPIO1_IO05	**GPIO:** GPIO1_IO05 **ISP:** ISP_FL_TRIG_1 **CCM:** CCM_PMIC_READY	DIO	VDD_1V8	Output high during reset; After reset: Input with PU
A54	A6	GPIO1_IO13	**GPIO:** GPIO1_IO13 **USB:** USB1_OTG_OC **PWM:** PWM2_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD
A55	B5	GPIO1_IO15	**GPIO:** GPIO1_IO15 **uSDHC:** uSDHC3_WP **USB:** USB2_OTG_OC **PWM:** PWM4_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD

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Pin Number SOM	Pin Number CPU	SOM/Processor Pin name	PIN Multiplexing	I/O	Power group	Comments
			CCM: CCM_CLKO**2**			
A56	-	**GND**	**NA**	-	**NA**	
A57	B7	GPIO1_IO10	**GPIO:** GPIO**1**_IO**14** **USB:** USB**1**_OTG_ID **PWM:** PWM**3**_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD
A58	A5	GPIO1_IO12	**GPIO:** GPIO**1**_IO**12** **USB:** USB**1**_OTG_PWR **SDMA:** SDMA**2**_EXT_EVENT**1**	DIO	VDD_1V8	**At reset Condition:** Input with PD
A59	A3	GPIO1_IO06	**GPIO:** GPIO**1**_IO**06** **uSDHC:** uSDHC**1**_CD_B **ENET_QOS:** ENET_QOS_MDC **ISP:** ISP_SHUTTER_TRIG_**1** **CCM:** CCM_EXT_CLK**3**	DIO	VDD_1V8	**At reset Condition:** Input with PD
A60	A7	GPIO1_IO00	**GPIO:** GPIO**1**_IO**00** **ISP:** ISP_FL_TRIG_**0** **CCM:** CCM_ENET_PHY_REF_CLK_ROOT CCM_EXT_CLK1 CCM_REF_CLK_32K	DIO	VDD_1V8	**At reset Condition:** Input with PD
A61	-	**GND**	**NA**	-	**NA**	
A62	-	**GND**	**NA**	-	**NA**	
A63	B8	GPIO1_IO09	**GPIO:** GPIO**1**_IO**09** **uSDHC:** uSDHC**3**_RESET_B **ENET_QOS:** ENET_QOS_1588_EVENT**0**_OUT **ISP:** ISP_SHUTTER_OPEN_**1** **PWM:** PWM**2**_OUT **SDMA:** SDMA**2**_EXT_EVENT**0**	DIO	VDD_1V8	**At reset Condition:** Input with PD
A64	-	**GND**	**NA**	-	**NA**	
A65	-	**GND**	**NA**	-	**NA**	
A66	A8	GPIO1_IO08	**GPIO:** GPIO**1**_IO**08** **uSDHC:** uSDHC**2**_RESET_B **ENET_QOS:** ENET_QOS_1588_EVENT**0**_AUX_IN ENET_QOS_1588_EVENT**0**_IN **ISP:** ISP_PRELIGHT_TRIG_**1** **PWM:** PWM**1**_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD
A67	E8	GPIO1_IO01	**GPIO:** GPIO**1**_IO**01** **ISP:** ISP_SHUTTER_TRIG_**0** **PWM:** PWM**1**_OUT **CCM:** CCM_REF_CLK_24M CCM_EXT_CLK2	DIO	VDD_1V8	Output low during reset; After reset: Input with PD
A68	F6	GPIO1_IO07	**GPIO:** GPIO**1**_IO**07** **uSDHC:** uSDHC**1**_WP **ENET_QOS:** ENET_QOS_MDIO **ISP:** ISP_FLASH_TRIG_**1** **CCM:** CCM_EXT_CLK**4**	DIO	VDD_1V8	**At reset Condition:** Input with PD
A69	D8	GPIO1_IO11	**GPIO:** GPIO**1**_IO**11**	DIO	VDD_1V8	**At reset Condition:** Input with

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Pin Number SOM	Pin Number CPU	SOM/Processor Pin name	PIN Multiplexing	I/O	Power group	Comments
			uSDHC: uSDHC3_VSELECT **USB:** USB2_OTG_ID **PWM:** PWM2_OUT **CCM:** CCM_PMIC_READY			PD
A70	G8	BOOT_MODE2	**NA**	DI	VDD_1V8	BOOT MODE CONFIGURATION: At reset Condition: Input with PD
A71	G12	BOOT_MODE3	**NA**	DI	VDD_1V8	BOOT MODE CONFIGURATION: At reset Condition: Input with PD
A72	F8	BOOT_MODE1	**NA**	DI	VDD_1V8	BOOT MODE CONFIGURATION: At reset Condition: Input with PD
A73	G10	BOOT_MODE0	**NA**	DI	VDD_1V8	BOOT MODE CONFIGURATION: At reset Condition: Input with PD
B1	AD18	SPDIF_RX	**GPIO:** GPIO5_IO4 **I2C:** I2C5_SDA **PWM:** PWM2_OUT **CAN:** CAN1_RX **GPT:** GPT1_COMPARE2 **SPDIF:** SPDIF1_IN	DIO	VDD_1V8	**At reset Condition:** Input with PD
B2	-	GND	NA	-	NA	
B3	AE18	SPDIF_TX	**GPIO:** GPIO5_IO3 **I2C:** I2C5_SCL **PWM:** PWM3_OUT **CAN:** CAN1_TX **GPT:** GPT1_COMPARE1 **SPDIF:** SPDIF1_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD
B4	-	GND	NA	-	NA	
B5	-	GND	NA	-	NA	
B6	AJ22	ECSPI2_SS0	**GPIO:** GPIO5_IO13 **I2C:** I2C4_SDA **UART:** UART4_RTS_B **CCM:** CCM_CLKO2 **ECSPI:** ECSPI2_SS0	DIO	VDD_1V8	**At reset Condition:** Input with PD
B7	-	GND	NA	-	NA	
B8	-	GND	NA	-	NA	
B9	AH21	ECSPI2_SCLK	**GPIO:** GPIO5_IO10 **SAI:** SAI7_TX_BCLK **I2C:** I2C3_SCL **UART:** UART4_RX **ECSPI:** ECSPI2_SCLK	DIO	VDD_1V8	**At reset Condition:** Input with PD
B10	-	GND	NA	-	NA	
B11	-	GND	NA	-	NA	
B12	AJ21	ECSPI2_MOSI	**GPIO:** GPIO5_IO11 **SAI:** SAI7_TX_DATA0	DIO	VDD_1V8	**At reset Condition:** Input with PD

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Pin Number SOM	Pin Number CPU	SOM/Processor Pin name	PIN Multiplexing	I/O	Power group	Comments
			I2C: I2C3_SDA **UART:** UART4_TX **ECSPI:** ECSPI2_MOSI			
B13	-	GND	NA	-	NA	
B14	-	GND	NA	-	NA	
B15	AH20	ECSPI2_MISO	**GPIO:** GPIO5_IO12 **SAI:** SAI7_MCLK **I2C:** I2C4_SCL **UART:** UART4_CTS_B **ESPI:** ECSPI2_MISO **CCM:** CCM_CLKO1	DIO	VDD_1V8	**At reset Condition:** Input with PD
B16-B20	-	GND	NA	-	NA	
B21	-	BT_PCM_CLK	**NA**	DIO	WI-FI_1V8	Bluetooth PCM clock: Output if Master Input if Slave
B22	-	BT_PCM_OUT	**NA**	DO	WI-FI_1V8	Bluetooth PCM Data Out
B23	-	GND	NA	-	NA	
B24	-	BT_PCM_IN	**NA**	DI	WI-FI_1V8	Bluetooth PCM Data In
B25	-	BT_PCM_SYNC	**NA**	DIO	WI-FI_1V8	Bluetooth PCM clock: Output if Master Input if Slave
B26-B29	-	GND	NA	-	NA	
B30	-	UART_LTE_SOUT	**NA**	DO	WI-FI_1V8	**Reserved for coexistence with LTE:** Serial data to external LTE device.
B31	-	UART_LTE_SIN	**NA**	DI	WI-FI_1V8	**Reserved for coexistence with LTE:** Serial data from external LTE device.
B32	-	GND	NA	-	NA	
B33	J29	POR_B	**NA**	DO	NVCC_SNVS_1V8	Power On reset output pin. Open drain output with 100K Ω pull up resistor. **At reset Condition:** Input with PU.
B34	-	GND	NA	-	NA	
B35	-	GND	NA	-	NA	
B36	F22	PMIC_ON_REQ	**NA**	DI	NVCC_SNVS_1V8	PMIC ON input from application processor. When it is asserted “High”, the PMIC starts the power on sequence. At reset Condition: Output with PU. **Note:**

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Pin Number SOM	Pin Number CPU	SOM/Processor Pin name	PIN Multiplexing	I/O	Power group	Comments
						This pin has internal connection between PMIC and NXP processor for managing the power. No external connection is required. **Suggest having test point on this pin for debug usage.**
B37	AH19	SAI3_TXC	**GPIO:** GPIO5_IO0 **SAI:** SAI3_TX_BCLK/SAI5_RX_DATA2 **UART:** UART2_TX **PDM:** PDM_BIT_STREAM2 **GPT:** GPT1_CAPTURE1	DIO	VDD_1V8	**At reset Condition:** Input with PD
B38	AJ20	SAI3_MCLK	**GPIO:** GPIO5_IO2 **SAI:** SAI3_MCLK/SAI5_MCLK **PWM:** PWM4_OUT **SPDIF:** SPDIF1_OUT/SPDIF1_IN	DIO	VDD_1V8	**At reset Condition:** Input with PD
B39	G22	ONOFF	**NA**	DI	NVCC_SNVS_1V8	Signal input to turn ON and turn OFF the Processor
B40	AJ19	SAI3_RXFS	**GPIO:** GPIO4_IO28 **SAI:** SAI3_RX_SYNC/SAI2_RX_DATA1 SAI5_RX_SYNC/SAI3_RX_DATA1 **PDM:** PDM_BIT_STREAM0 **SPDIF:** SPDIF1_IN	DIO	VDD_1V8	**At reset Condition:** Input with PD
B41	-	GND	NA	-	NA	
B42	-	GND	NA	-	NA	
B43	AH18	SAI3_TXD	**GPIO:**GPIO5_IO1 **SAI:** SAI3_TX_DATA0/SAI2_TX_DATA3 SAI5_RX_DATA3 **GPT:** GPT1_CAPTURE2 **SPDIF:** SPDIF1_ EXT_CLK **SRC:** SRC_BOOT_MODE5	DIO	VDD_1V8	**At reset Condition:** Input with PD
B44	AF18	SAI3_RXD	**GPIO:** GPIO4_IO30 **SAI:** SAI3_RX_DATA0/SAI2_RX_DATA3 SAI5_RX_DATA0 **UART:** UART2_RTS_B **PDM:** PDM_BIT_STREAM1	DIO	VDD_1V8	**At reset Condition:** Input with PD
B45	AJ18	SAI3_RXC	**GPIO:** GPIO4_IO29 **SAI:** SAI3_RX_BCLK/SAI2_RX_DATA2 SAI5_RX_BCLK **UART:** UART2_CTS_B **PDM:** PDM_CLK **GPT:** GPT1_CLK	DIO	VDD_1V8	**At reset Condition:** Input with PD
B46	AC16	SAI3_TXFS	**GPIO:** GPIO4_IO31 **SAI:** SAI3_TX_SYNC/SAI2_TX_DATA1 SAI5_RX_DATA1/SAI3_TX_DATA1 **UART:** UART2_RX	DIO	VDD_1V8	**At reset Condition:** Input with PD

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Pin Number SOM	Pin Number CPU	SOM/Processor Pin name	PIN Multiplexing	I/O	Power group	Comments
			PDM: PDM_BIT_STREAM3			
B47	-	GND	NA	-	NA	
B48	-	GND	NA	-	NA	
B49	AH17	SAI2_RXFS	**GPIO:** GPIO4_IO21 **SAI:** SAI2_RX_SYNC/SAI5_TX_SYNC SAI5_TX_DATA1/SAI2_RX_DATA1 **UART:** UART1_TX **PDM:** PDM_BIT_STREAM2	DIO	VDD_1V8	**At reset Condition:** Input with PD
B50	AJ17	SAI2_TXFS	**GPIO:** GPIO4_IO24 **SAI:** SAI2_TX_SYNC/SAI5_TX_DATA1 SAI2_TX_DATA1 **UART:** UART1_CTS_B **PDM:** PDM_BIT_STREAM2 **ENET_QOS:** ENET_QOS_1588_EVENT3_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD
B51	AJ16	SAI2_RXC	**GPIO:** GPIO4_IO22 **SAI:** SAI2_RX_BCLK/SAI5_TX_BCLK **UART:** UART1_RX **PDM:** PDM_BIT_STREAM1 **CAN:** CAN1_TX	DIO	VDD_1V8	**At reset Condition:** Input with PD
B52	AH16	SAI2_TXD0	**GPIO:** GPIO4_IO26 **SAI:** SAI2_TX_DATA0/SAI5_TX_DATA3 **ENET_QOS:** ENET_QOS_1588_EVENT2_IN ENET_QOS_1588_EVENT2_AUX_IN **CAN:** CAN2_TX **SRC:** SRC_BOOT_MODE4	DIO	VDD_1V8	**At reset Condition:** Input with PD
B53	AH15	SAI2_TXC	**GPIO:** GPIO4_IO25 **SAI:** SAI2_TX_BCLK/SAI5_TX_DATA2 **PDM:** PDM_BIT_STREAM1 **CAN:** CAN1_RX	DIO	VDD_1V8	**At reset Condition:** Input with PD
B54	AJ15	SAI2_MCLK	**GPIO:** GPIO4_IO27 **SAI:** SAI2_MCLK/SAI5_MCLK/SAI3_MCLK **ENET_QOS:** ENET_QOS_1588_EVENT3_IN ENET_QOS_1588_EVENT3_AUX_IN **CAN:** CAN2_RX	DIO	VDD_1V8	**At reset Condition:** Input with PD
B55	AJ14	SAI2_RXD0	**GPIO:** GPIO4_IO23 **SAI:** SAI2_RX_DATA0/SAI5_TX_DATA0 SAI2_TX_DATA1 **UART:** UART1_RTS **PDM:** PDM_BIT_STREAM3 **ENET_QOS:** ENET_QOS_1588_EVENT2_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD
B56		VDD_3V3	**NA**	PO	**NA**	3.3V power output from SOM. **Note:** **NOT to be power source for the**

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Pin Number SOM	Pin Number CPU	SOM/Processor Pin name	PIN Multiplexing	I/O	Power group	Comments
						other circuit; Reserved for control the add-on circuit when SOM is in power saving mode.
B57	-	**GND**	**NA**	-	**NA**	
B58	AD16	SAI5_RXD1	**GPIO:** GPIO3_IO22 **SAI:** SAI5_RX_DATA1/SAI1_TX_DATA3 SAI1_TX_SYNC/SAI5_TX_SYNC **PDM:** PDM_BIT_STREAM1 **CAN:** CAN1_TX	DIO	VDD_1V8	**At reset Condition:** Input with PD
B59	-	**GND**	**NA**	-	**NA**	
B60	AF16	SAI5_RXD2	**GPIO:** GPIO3_IO23 **SAI:** SAI5_RX_DATA2/SAI1_TX_DATA4 SAI1_TX_SYNC/SAI5_TX_BCLK **PDM:** PDM_BIT_STREAM2 **CAN:** CAN1_RX	DIO	VDD_1V8	**At reset Condition:** Input with PD
B61	-	**GND**	**NA**	-	**NA**	
B62		**VSD_3V3**	**NA**	PO	**VDD_3V3**	3.3V power output from SOM. **Note:** **A load switch built-in the PMIC that generate the VSD_3V3 from the VDD_3V3 rail by the SD2_RESET_B control signal from the NXP processor.** **The VSD_3V3 has 400mA current limit that can be used as the power source for uSDHC2 bus.**
B63	AE16	SAI5_RXD0	**GPIO:** GPIO3_IO21 **SAI:** SAI5_RX_DATA0/SAI1_TX_DATA2 **I2C:** I2C5_SCL **PDM:** PDM_BIT_STREAM0 **PWM:** PWM2_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD
B64	-	**GND**	**NA**	-	**NA**	
B65		**VSD_3V3**	**NA**	PO	VDD_3V3	3.3V power output from SOM. **Note:** **A load switch built-in the PMIC that generates the VSD_3V3 from the VDD_3V3 rail by the SD2_RESET_B control signal from the NXP processor.** **The VSD_3V3 has 400mA current limit that can be used as the power source for uSDHC2 bus.**
B66	AF14	SAI5_MCLK	**GPIO:** GPIO3_IO25 **SAI:** SAI5_MCLK/SAI1_TX_BCLK **I2C:** I2C5_SDA **PWM:** PWM1_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD

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			CAN: CAN2_RX			
B67	AD14	SAI5_RXC	**GPIO:** GPIO3_IO20 **SAI:** SAI5_RX_BCLK/SAI1_TX_DATA1 **I2C:** I2C6_SDA **PDM:** PDM_CLK **PWM:** PWM3_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD
B68	AE14	SAI5_RXD3	**GPIO:** GPIO3_IO24 **SAI:** SAI5_RX_DATA3/SAI1_TX_DATA5 SAI1_TX_SYNC/SAI5_TX_DATA0 **PDM:** PDM_BIT_STREAM3 **CAN:** CAN2_TX	DIO	VDD_1V8	**At reset Condition:** Input with PD
B69	AC14	SAI5_RXFS	**GPIO:** GPIO3_IO19 **SAI:** SAI5_RX_SYNC/SAI1_TX_DATA0 **I2C:** I2C6_SCL **PWM:** PWM4_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD
B70	-	**SCLL**	**NA**	DO	NVCC_SNVS_1V8	Level translator low voltage I/O pin 1.8V
B71	-	**GND**	**NA**	-	**NA**	
B72	-	**GND**	**NA**	-	**NA**	
B73	-	**SDAL**	**NA**	DIO	NVCC_SNVS_1V8	Level translator low voltage I/O pin 1.8V
B74	-	**SCLH**	**NA**	DO	VDD_3V3	Level translator low voltage I/O pin 3.3V
B75	-	**SDAH**	**NA**	DIO	VDD_3V3	Level translator low voltage I/O pin 3.3V
B76	-	**GND**	**NA**	-	**NA**	
B77	AJ12	SAI1_TXC	**GPIO:** GPIO4_IO11 **SAI:** SAI1_TX_BCLK/SAI5_TX_BCLK **ENET1:** ENET1_RGMII_RXC	DIO	VDD_1V8	**At reset Condition:** Input with PD
B78	AF12	SAI1_TXFS	**GPIO:** GPIO4_IO10 **SAI:** SAI1_TX_SYNC/SAI5_TX_SYNC **ENET1:** ENET1_RGMII_RX_CTL	DIO	VDD_1V8	**At reset Condition:** Input with PD
B79	AJ13	SAI1_TXD7	**GPIO:** GPIO4_IO19 **SAI:** SAI1_TX_DATA7/SAI6_MCLK **PDM:** PDM_CLK **ENET1:** ENET1_TX_ER	DIO	VDD_1V8	**At reset Condition:** Input with PD
B80		**VSYS_5V**	**NA**	PI	**NA**	SOM main power input: 2.7V to 5.5V **Note:** **Place 1uF bypass capacitor (or greater) as close as possible to this pin.**
B81	AC12	SAI1_TXD6	**GPIO:** GPIO4_IO18 **SAI:** SAI1_TX_DATA6/SAI6_RX_SYNC SAI6_TX_SYNC **ENET1:** ENET1_RX_ER	DIO	VDD_1V8	**At reset Condition:** Input with PD
B82	-	**GND**	**NA**	-	**NA**	
B83		**VSYS_5V**	**NA**	PI	**NA**	SOM main power input: 2.7V to 5.5V **Note:**

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						Place 1uF bypass capacitor (or greater) as close as possible to this pin.
B84	AH14	SAI1_TXD5	**GPIO:** GPIO4_IO17 **SAI:** SAI1_TX_DATA5/SAI6_RX_DATA0 SAI6_TX_DATA0 **ENET1:** ENET1_RGMII_TXC			**At reset Condition:** Input with PD
B85	-	**GND**	**NA**	-	**NA**	
B86		**VSYS_5V**	**NA**	PI	**NA**	SOM main power input: 2.7V to 5.5V **Note:** **Place 1uF bypass capacitor (or greater) as close as possible to this pin.**
B87	AH13	SAI1_TXD4	**GPIO:** GPIO4_IO16 **SAI:** SAI1_TX_DATA4/SAI6_RX_BCLK SAI6_TX_BCLK **ENET1:** ENET1_RGMII_TX_CTL			**At reset Condition:** Input with PD
B88	AD12	SAI1_TXD3	**GPIO:** GPIO4_IO15 **SAI:** SAI1_TX_DATA3/SAI5_TX_DATA3 **ENET1:** ENET1_RGMII_TD3	DIO	VDD_1V8	**At reset Condition:** Input with PD
B89	AH11	SAI1_TXD2	**GPIO:** GPIO4_IO14 **SAI:** SAI1_TX_DATA2/SAI5_TX_DATA2 **ENET1:** ENET1_RGMII_TD2	DIO	VDD_1V8	**At reset Condition:** Input with PD
B90	AJ10	SAI1_TXD1	**GPIO:** GPIO4_IO13 **SAI:** SAI1_TX_DATA1/SAI5_TX_DATA1 **ENET1:** ENET1_RGMII_TD1	DIO	VDD_1V8	**At reset Condition:** Input with PD
B91	AJ11	SAI1_TXD0	**GPIO:** GPIO4_IO12 **SAI:** SAI1_TX_DATA0/SAI5_TX_DATA0 **ENET1:** ENET1_RGMII_TD0	DIO	VDD_1V8	**At reset Condition:** Input with PD
C1	**E29**	**LVDS0_D1_P**	**NA**	DO	VDDA_1V8	
C2	**F28**	**LVDS0_D1_N**	**NA**	DO	VDDA_1V8	
C3	**F29**	**LVDS0_CLK_P**	**NA**	DO	VDDA_1V8	
C4	**G28**	**LVDS0_CLK_N**	**NA**	DO	VDDA_1V8	
C5	**K28**	**CLKIN1**	**NA**	DI	VDD_1V8	**At reset Condition:** Input with PD
C6	**G29**	**LVDS0_D2_P**	**NA**	DO	VDDA_1V8	
C7	**H28**	**LVDS0_D2_N**	**NA**	DO	VDDA_1V8	
C8	**K29**	**CLK_OUT1**	**NA**	DO	VDD_1V8	**At reset Condition:** Input with PD
C9	**H29**	**LVDS0_D3_P**	**NA**	DO	VDDA_1V8	
C10	**J28**	**LVDS0_D3_N**	**NA**	DO	VDDA_1V8	
C11	**L28**	**CLKIN2**	**NA**	DI	VDD_1V8	**At reset Condition:** Input with PD
C12	-	**GND**	**NA**	-	**NA**	

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C13	-	GND	NA	-	NA	
C14	L29	CLK_OUT2	NA	DO	VDD_1V8	**At reset Condition:** Output low
C15	L24	NAND_DATA02	**GPIO:** GPIO3_IO8 **uSDHC:** uSDHC3_CD_B **I2C:** I2C4_SDA **UART:** UART4_CTS_B **NAND:** NAND_DATA02 **QSPI:** QSPI_A_DATA2	DIO	VDD_1V8	**At reset Condition:** Input with PD
C16	L25	NAND_DATA01	**GPIO:** GPIO3_IO7 **SAI:** SAI3_TX_SYNC **UART:** UART4_TX **ISP:** ISP_PRELIGHT_TRIG_0 **NAND:** NAND_DATA01 **QSPI:** QSPI_A_DATA1	DIO	VDD_1V8	**At reset Condition:** Input with PD
C17	-	GND	NA	-	NA	
C18	N24	NAND_DATA03	**GPIO:** GPIO3_IO9 **uSDHC:** uSDHC3_WP **UART:** UART4_RTS_B **ISP:** ISP_FL_TRIG_1 **NAND:** NAND_DATA03 **QSPI:** QSPI_A_DATA3	DIO	VDD_1V8	**At reset Condition:** Input with PD
C19	N25	NAND_ALE	**GPIO:** GPIO3_IO0 **SAI:** SAI3_TX_BCLK **UART:** UART3_RX **ISP:** ISP_FL_TRIG_0 **NAND:** NAND_ALE **QSPI:** QSPI_A_SCLK	DIO	VDD_1V8	**At reset Condition:** Input with PD
C20	L26	NAND_CE0_B	**GPIO:** GPIO3_IO1 **SAI:** SAI3_TX_DATA0 **UART:** UART3_TX **ISP:** ISP_SHUTTER_TRIG_0 **NAND:** NAND_ CE0_B **QSPI:** QSPI_A_SS0_B	DIO	VDD_1V8	**At reset Condition:** Input with PD
C21	R25	NAND_DATA00	**GPIO:** GPIO3_IO6 **SAI:** SAI3_RX_DATA0 **UART:** UART4_RX **ISP:** ISP_FLASH_TRIG_0 **NAND:** NAND_DATA00 **QSPI:** QSPI_A_DATA0	DIO	VDD_1V8	**At reset Condition:** Input with PD
C22	-	GND	NA	-	NA	
C23	T28	NAND_READY_B	**GPIO:** GPIO3_IO16 **uSDHC:** uSDHC3_RESET_B **I2C:** I2C3_SCL **NAND:** NAND_READY_B	DIO	VDD_1V8	**At reset Condition:** Input with PD
C24	-	GND	NA	-	NA	
C25	-	GND	NA	-	NA	
C26	-	GND	NA	-	NA	
C27	AB29	SD2_CLK	**GPIO:** GPIO2_IO13 **uSDHC:** uSDHC2_CLK	DIO	NVCC_SD2	**At reset Condition:** Input with PD

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			ART:UART4_RX **ECSPI:** ECSPI2_SCLK			Note: When operating at uSDHC2, the I/O level are automatically detected and set either 1.8V or 3.3V accordingly.
C28	AA26	SD2_DATA2	**GPIO:** GPIO2_IO17 **uSDHC:** uSDHC2_DATA2 **PDM:** PDM_BIT_STREAM2 **ECSPI:** ECSPI2_SS0 **SPDIF:** SPDIF1_OUT	DIO	NVCC_SD2	**At reset Condition:** Input with PD Note: When operating at uSDHC2, the I/O level are automatically detected and set either 1.8V or 3.3V accordingly.
C29	**-**	**GND**	**NA**	**-**	**NA**	
C30	AB28	SD2_CMD	**GPIO:** GPIO2_IO14 **uSDHC:** uSDHC2_CMD **UART:** UART4_TX **PDM:** PDM_CLK **ECSPI:** ECSPI2_MOSI	DIO	NVCC_SD2	**At reset Condition**: Input with PD Note: When operating at uSDHC2, the I/O level are automatically detected and set either 1.8V or 3.3V accordingly.
C31	AA25	SD2_DATA3	**GPIO:** GPIO2_IO18 **uSDHC:** uSDHC2_DATA3 **PDM:** PDM_BIT_STREAM3 **ECSPI:** ECSPI2_MISO **SPDIF:** SPDIF1_IN **SRC:** SRC_EARLY_RESET	DIO	NVCC_SD2	**At reset Condition:** Input with PD Note: When operating at uSDHC2, the I/O level are automatically detected and set either 1.8V or 3.3V accordingly.
C32	AC26	SD2_WP	**GPIO:** GPIO2_IO20 **uSDHC:** uSDHC2_WP	DIO	NVCC_SD2	**At reset Condition:** Input with PD Note: When operating at uSDHC2, the I/O level are automatically detected and set either 1.8V or 3.3V accordingly.
C33	AC29	SD2_DATA1	**GPIO:** GPIO2_IO16 **uSDHC:** uSDHC2_DATA1 **I2C:** I2C4_SCL **UART:** UART2_TX **PDM:** PDM_BIT_STREAM1	DIO	NVCC_SD2	**At reset Condition:** Input with PD Note: When operating at uSDHC2, the I/O level are automatically detected and set either 1.8V or 3.3V accordingly.
C34	AC28	SD2_DATA0	**GPIO:** GPIO2_IO15 **uSDHC:** uSDHC2_DATA0 **I2C:** I2C4_SDA **UART:** UART2_RX **PDM:** PDM_BIT_STREAM0	DIO	NVCC_SD2	**At reset Condition:** Input with PD Note: When operating at uSDHC2, the I/O level are automatically detected and set either 1.8V or 3.3V accordingly.
C35	AD28	SD2_RESET_B	**GPIO:** GPIO2_IO19 **uSDHC:** uSDHC2_RESET_B **SRC:** SRC_SYSTEM_RESET	DIO	NVCC_SD2	**At reset Condition:** Input with PD Note: When operating at uSDHC2, the I/O level are automatically detected and set either 1.8V or

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						3.3V accordingly.
C36	AD29	SD2_CD_B	**GPIO:** GPIO2_IO12 **uSDHC:** uSDHC2_CD_B	DIO	NVCC_SD2	**At reset Condition:** Input with PD Note: When operating at uSDHC2, the I/O level are automatically detected and set either 1.8V or 3.3V accordingly.
C37-C39	-	GND	NA	-	NA	
C40	AG28	ENET_RD1	**GPIO:** GPIO1_IO27 **SAI:** SAI7_RX_SYNC **uSDHC:** uSDHC3_RESET_B **PDM:** PDM_BIT_STREAM0 **ENET_QOS:** ENET_QOS_RGMII_RD1	DIO	VDD_1V8	**At reset Condition:** Input with PD
C41	AH29	ENET_MDIO	**GPIO:** GPIO1_IO17 **SAI:** SAI6_TX_SYNC **uSDHC:** uSDHC3_DATA5 **PDM:** PDM_BIT_STREAM3 **ENET_QOS:** ENET_QOS_MDIO	DIO	VDD_1V8	**At reset Condition:** Input with PD
C42	AE29	ENET_RXC	**GPIO:** GPIO1_IO25 **SAI:** SAI7_TX_BCLK **uSDHC:** uSDHC3_DATA3 **PDM:** PDM_BIT_STREAM2 **ENET_QOS:** ENET_QOS_RGMII_RXC ENET_QOS_RX_ER	DIO	VDD_1V8	**At reset Condition:** Input with PD
C43	AF29	ENET_RD2	**GPIO:** GPIO1_IO28 **SAI:** SAI7_RX_BCLK **uSDHC:** uSDHC3_CLK **PDM:** PDM_CLK **ENET_QOS:** ENET_QOS_RGMII_RD2	DIO	VDD_1V8	**At reset Condition:** Input with PD
C44	AE28	ENET_RX_CTL	**GPIO:** GPIO1_IO24 **SAI:** SAI7_TX_SYNC **uSDHC:** uSDHC3_DATA2 **PDM:** PDM_BIT_STREAM3 **ENET_QOS:** ENET_QOS_RGMII_RX_CTL	DIO	VDD_1V8	**At reset Condition:** Input with PD
C45	AF28	ENET_RD3	**GPIO:** GPIO1_IO29 **SAI:** SAI7_MCLK **uSDHC:** uSDHC3_CMD **ENET_QOS:** ENET_QOS_RGMII_RD3 **SPDIF:** SPDIF1_IN	DIO	VDD_1V8	**At reset Condition:** Input with PD
C46	AH28	ENET_MDC	**GPIO:** GPIO1_IO16 **SAI:** SAI6_TX_DATA0 **uSDHC:** uSDHC3_STROBE **ENET_QOS:** ENET_QOS_MDC	DIO	VDD_1V8	**At reset Condition:** Input with PD
C47	AC25	ENET_TD0	**GPIO:** GPIO1_IO21 **SAI:** SAI6_RX_BCLK **uSDHC:** uSDHC3_WP **PDM:** PDM_CLK **ENET_QOS:** ENET_QOS_RGMII_TD0	DIO	VDD_1V8	**At reset Condition:** Input with PD
C48	AG29	ENET_RD0	**GPIO:** GPIO1_IO26 **SAI:** SAI7_RX_DATA0	DIO	VDD_1V8	**At reset Condition:** Input with PD

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			uSDHC: uSDHC3_DATA4 **PDM:** PDM_BIT_STREAM1 **ENET_QOS:** ENET_QOS_RGMII_RD0			
C49	AE26	ENET_TD1	**GPIO:** GPIO1_IO20 **SAI:** SAI6_RX_SYNC **uSDHC:** uSDHC3_CD_B **PDM:** PDM_BIT_STREAM0 **ENET_QOS:** ENET_QOS_RGMII_TD1	DIO	VDD_1V8	**At reset Condition:** Input with PD
C50	AD24	ENET_TD3	**GPIO:** GPIO1_IO18 **SAI:** SAI6_TX_BCLK **uSDHC:** uSDHC3_DATA6 **PDM:** PDM_BIT_STREAM2 **ENET_QOS:** ENET_QOS_RGMII_TD3	DIO	VDD_1V8	**At reset Condition:** Input with PD
C51	AF26	ENET_TD2	**GPIO:** GPIO1_IO19 **SAI:** SAI6_RX_DATA0 **uSDHC:** uSDHC3_DATA7 **PDM:** PDM_BIT_STREAM1 **ENET_QOS:** ENET_QOS_RGMII_TD2 ENET_QOS_TX_CLK	DIO	VDD_1V8	**At reset Condition:** Input with PD
C52	AE24	ENET_TXC	**GPIO:** GPIO1_IO23 **SAI:** SAI7_TX_DATA0 **uSDHC:** USDHC3_DATA1 **ENET_QOS:** ENET_QOS_RGMII_TXC ENET_QOS_TX_ER	DIO	VDD_1V8	**At reset Condition:** Input with PD
C53	AF24	ENET_TX_CTL	**GPIO:** GPIO1_IO22 **SAI:** SAI6_MCLK **uSDHC:** uSDHC3_DATA0 **ENET_QOS:** ENET_QOS_RGMII_TX_CTL **SPDIF:** SPDIF1_OUT	DIO	VDD_1V8	**At reset Condition:** Input with PD
C54	**-**	**GND**	**NA**	**-**	**NA**	
C55	**-**	**GND**	**NA**	**-**	**NA**	
C56	AC22	HDMI_DDC_SCL	**GPIO:** GPIO3_IO26 **I2C:** I2C5_SCL **CAN:** CAN1_TX **HDMI:** HDMI_SCL	DIO	VDD_1V8	**At reset Condition:** Input with PD
C57	**AH27**	**HDMI_TX2_P**	**NA**	DIO	VDDA_1V8	
C58	**AJ27**	**HDMI_TX2_N**	**NA**	DIO	VDDA_1V8	
C59	**AH23**	**EARC_AUX**	**NA**	DIO	VDDA_1V8	**At reset Condition:** Input with PD
C60	**AH26**	**HDMI_TX1_P**	**NA**	DIO	VDDA_1V8	
C61	**AJ26**	**HDMI_TX1_N**	**NA**	DIO	VDDA_1V8	
C62	AD22	HDMI_CEC	**GPIO:** GPIO3_IO28 **I2C:** I2C6_SCL **CAN:** CAN2_TX **HDMI:** HDMI_CEC	DIO	VDD_1V8	**At reset Condition:** Input with PD
C63	**AH25**	**HDMI_TX0_P**	**NA**	DIO	VDDA_1V8	

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SOM	CPU					
C64	AJ25	HDMI_TX0_N	**NA**	DIO	VDDA_1V8	
C65	AE22	HDMI_HPD	**GPIO:** GPIO3_IO29 **I2C:** I2C6_SDA **CAN:** CAN2_RX **HDMI:** HDMI_HPD/HDMI_HPD_O	DIO	VDD_1V8	**At reset Condition:** Input with PD
C66	AH24	HDMI_TXC_P	**NA**	DIO	VDDA_1V8	
C67	AJ24	HDMI_TXC_N	**NA**	DIO	VDDA_1V8	
C68	AF22	HDMI_DDC_SDA	**GPIO:** GPIO3_IO27 **I2C:** I2C5_SDA **CAN:** CAN1_RX **HDMI:** HDMI_SDA	DIO	VDD_1V8	**At reset Condition:** Input with PD
C69	AJ23	EARC_P_UTIL	**NA**	DIO	VDDA_1V8	**At reset Condition:** Output
C70	AH22	EARC_N_HPD	**NA**	DIO	VDDA_1V8	**At reset Condition:** Output
C71	-	GND	NA	-	NA	
C72	-	GND	NA	-	NA	
C73	AC18	SPDIF_EXT_CLK	**GPIO:** GPIO5_IO5 **PWM:** PWM1_OUT **GPT:** GPT1_COMPARE3 **SPDIF:** SPDIF1_EXT_CLK			
D1	A11	USB1_VBUS_3V3	**NA**	DI	VDD_3V3	**At reset Condition:** Input
D2	E10	USB1_DN	**NA**	DIO	VDD_3V3	**At reset Condition:** Input
D3	D10	USB1_DP	**NA**	DIO	VDD_3V3	**At reset Condition:** Input
D4	B9	USB1_RXN	**NA**	DIO	VDD_3V3	**At reset Condition:** Input
D5	B11	USB1_ID	**NA**	DI	VDD_3V3	NA
D6	A9	USB1_RXP	**NA**	DIO	VDD_3V3	**At reset Condition:** Input
D7	B10	USB1_TXN	**NA**	DIO	VDD_3V3	**At reset Condition:** Output
D8	-	GND	NA	-	NA	
D9	A10	USB1_TXP	**NA**	DIO	VDD_3V3	**At reset Condition:** Output
D10	-	GND	NA	-	NA	
D11	E12	USB2_ID	**NA**	DI	VDD_3V3	NA
D12	-	GND	NA	-	NA	
D13	B12	USB2_RXN	**NA**	DIO	VDD_3V3	**At reset Condition:** Input
D14	D12	USB2_VBUS_3V3	**NA**	DI	VDD_3V3	**At reset Condition:** Input
D15	A12	USB2_RXP	**NA**	DIO	VDD_3V3	**At reset Condition:** Input
D16	B13	USB2_TXN	**NA**	DIO	VDD_3V3	**At reset Condition:** Output
D17	-	GND	NA	-	NA	
D18	A13	USB2_TXP	**NA**	DIO	VDD_3V3	**At reset Condition:** Output
D19	D14	USB2_DP	**NA**	DIO	VDD_3V3	**At reset Condition:** Input

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Pin Number		SOM/Processor Pin name	PIN Multiplexing	I/O	Power group	Comments
SOM	CPU					
D20	-	GND	NA	-	NA	
D21	E14	USB2_DN	NA	DIO	VDD_3V3	**At reset Condition:** Input
D22-D24	-	GND	NA	-	NA	
D25	B16	MIPI_DSI1_D0_N	NA	DO	VDDA_1V8	**At reset Condition:** Output low
D26	-	GND	NA	-	NA	
D27	A16	MIPI_DSI1_D0_P	NA	DO	VDDA_1V8	**At reset Condition:** Output low
D28	B17	MIPI_DSI1_D1_N	NA	DO	VDDA_1V8	**At reset Condition:** Output low
D29	-	GND	NA	-	NA	
D30	A17	MIPI_DSI1_D1_P	NA	DO	VDDA_1V8	**At reset Condition:** Output low
D31	B18	MIPI_DSI1_CLK_N	NA	DO	VDDA_1V8	**At reset Condition:** Output low
D32	F14	JTAG_TDO	NA	DO	VDD_1V8	
D33	A18	MIPI_DSI1_CLK_P	NA	DO	VDDA_1V8	**At reset Condition:** Output low
D34	B19	MIPI_DSI1_D2_N	NA	DO	VDDA_1V8	**At reset Condition:** Output low
D35	G14	JTAG_TMS	NA	DI	VDD_1V8	**At reset Condition:** Input with PU
D36	A19	MIPI_DSI1_D2_P	NA	DO	VDDA_1V8	**At reset Condition:** Output low
D37	B20	MIPI_DSI1_D3_N	NA	DO	VDDA_1V8	**At reset Condition:** Output low
D38	G16	JTAG_TDI	NA	DI	VDD_1V8	**At reset Condition:** Input with PU
D39	A20	MIPI_DSI1_D3_P	NA	DO	VDDA_1V8	**At reset Condition:** Output low
D40	-	GND	NA	-	NA	
D41	G18	JTAG_TCK	NA	DI	VDD_1V8	**At reset Condition:** Input with PU
D42	-	GND	NA	-	NA	
D43	D20	MIPI_CSI1_D1_P	NA	DI	VDDA_1V8	**At reset Condition:** Input
D44	G20	JTAG_MOD	NA	DI	VDD_1V8	**At reset Condition:** Input with PD
D45	E20	MIPI_CSI1_D1_N	NA	DI	VDDA_1V8	**At reset Condition:** Input
D46	D22	MIPI_CSI1_CLK_P	NA	DO	VDDA_1V8	**At reset Condition:** Input
D47	-	GND	NA	-	NA	
D48	E22	MIPI_CSI1_CLK_N	NA	DO	VDDA_1V8	**At reset Condition:** Input
D49	D24	MIPI_CSI1_D2_P	NA	DI	VDDA_1V8	**At reset Condition:** Input
D50	D18	MIPI_CSI1_D0_P	NA	DI	VDDA_1V8	**At reset Condition:** Input
D51	E24	MIPI_CSI1_D2_N	NA	DI	VDDA_1V8	**At reset Condition:** Input
D52	D26	MIPI_CSI1_D3_P	NA	DI	VDDA_1V8	**At reset Condition:** Input
D53	E18	MIPI_CSI1_D0_N	NA	DI	VDDA_1V8	**At reset Condition:** Input
D54	E26	MIPI_CSI1_D3_N	NA	DI	VDDA_1V8	**At reset Condition:** Input
D55	-	GND	NA	-	NA	
D56	-	GND	NA	-	NA	

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Pin Number		SOM/Processor Pin name	PIN Multiplexing	I/O	Power group	Comments
SOM	CPU					
D57	B21	MIPI_CSI2_D3_N	NA	DI	VDDA_1V8	**At reset Condition:** Input
D58	A21	MIPI_CSI2_D3_P	NA	DI	VDDA_1V8	**At reset Condition:** Input
D59	-	GND	NA	-	NA	
D60	B22	MIPI_CSI2_D2_N	NA	DI	VDDA_1V8	**At reset Condition:** Input
D61	A22	MIPI_CSI2_D2_P	NA	DI	VDDA_1V8	**At reset Condition:** Input
D62	-	GND	NA	-	NA	
D63	B23	MIPI_CSI2_CLK_N	NA	DO	VDDA_1V8	**At reset Condition:** Input
D64	A23	MIPI_CSI2_CLK_P	NA	DO	VDDA_1V8	**At reset Condition:** Input
D65	-	GND	NA	-	NA	
D66	B24	MIPI_CSI2_D1_N	NA	DI	VDDA_1V8	**At reset Condition:** Input
D67	A24	MIPI_CSI2_D1_P	NA	DI	VDDA_1V8	**At reset Condition:** Input
D68	-	GND	NA	-	NA	
D69	B25	MIPI_CSI2_D0_N	NA	DI	VDDA_1V8	**At reset Condition:** Input
D70	A25	MIPI_CSI2_D0_P	NA	DI	VDDA_1V8	**At reset Condition:** Input
D71-D73	-	GND	NA	-	NA	
D74	-	GND	NA	-	NA	
D75	A26	LVDS1_D0_P	NA	DO	VDDA_1V8	
D76	B26	LVDS1_D0_N	NA	DO	VDDA_1V8	
D77	-	GND	NA	-	NA	
D78	A27	LVDS1_D1_P	NA	DO	VDDA_1V8	
D79	B27	LVDS1_D1_N	NA	DO	VDDA_1V8	
D80	-	GND	NA	-	NA	
D81	A28	LVDS1_CLK_P	NA	DO	VDDA_1V8	
D82	B28	LVDS1_CLK_N	NA	DO	VDDA_1V8	
D83	-	GND	NA	-	NA	
D84	B29	LVDS1_D2_P	NA	DO	VDDA_1V8	
D85	C28	LVDS1_D2_N	NA	DO	VDDA_1V8	
D86	-	GND	NA	-	NA	
D87	C29	LVDS1_D3_P	NA	DO	VDDA_1V8	
D88	D28	LVDS1_D3_N	NA	DO	VDDA_1V8	
D89	D29	LVDS0_D0_P	NA	DO	VDDA_1V8	
D90	E28	LVDS0_D0_N	NA	DO	VDDA_1V8	
D91	-	GND	NA	-	NA	
G1-G4		GND	NA	-	NA	

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10 MECHANICAL AND PCB FOOTPRINT SPECIFICATION

Module dimensions of Summit SOM 8M Plus are 47 x 40 x 4.6 mm. Detail drawings are shown in Figure 4.

Note: There are some components located at the center of the bottom of the module (see below picture). The host PCB requires routing out of that area. Please reference the PCB footprint for detail dimension from our website.

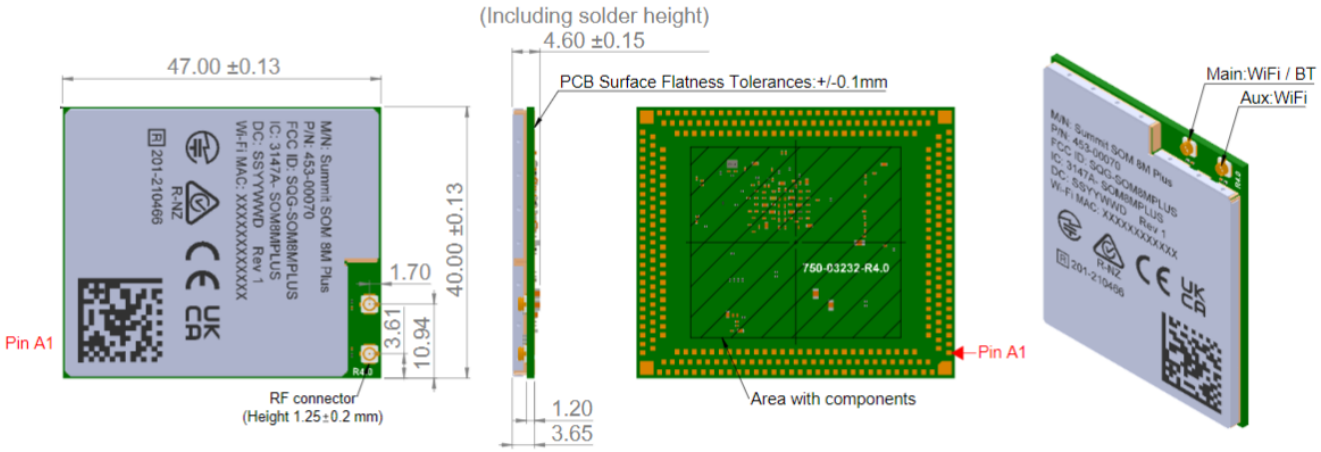

Figure 4: Mechanical drawing – Summit SOM 8M Plus module

The heat-sink kit for thermal management is detailed in Figure 5. It contains a thermal pad, heat sink and two push pins. The user can install it after the SOM is assembled on the host platform. When the system reaches an ambient temperature higher than 70°C, a heat sink like this is needed to maintain function and reliability.

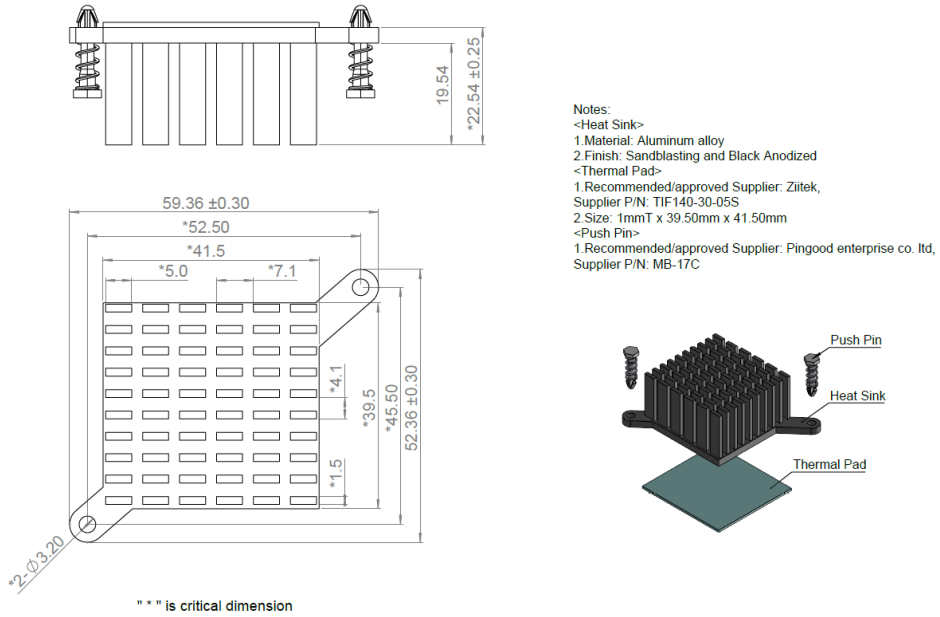

Figure 5: Mechanical drawing – Summit SOM 8M Plus module

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Figure 6 details the recommend PCB footprint implementation on the host PCB. Be aware of the keep out and routing area at the center of the SOM module. Also, always retain the two location holes (and connect to ground) for heat sink kit so that a heat sink can be applied if thermal management issues are encountered during development.

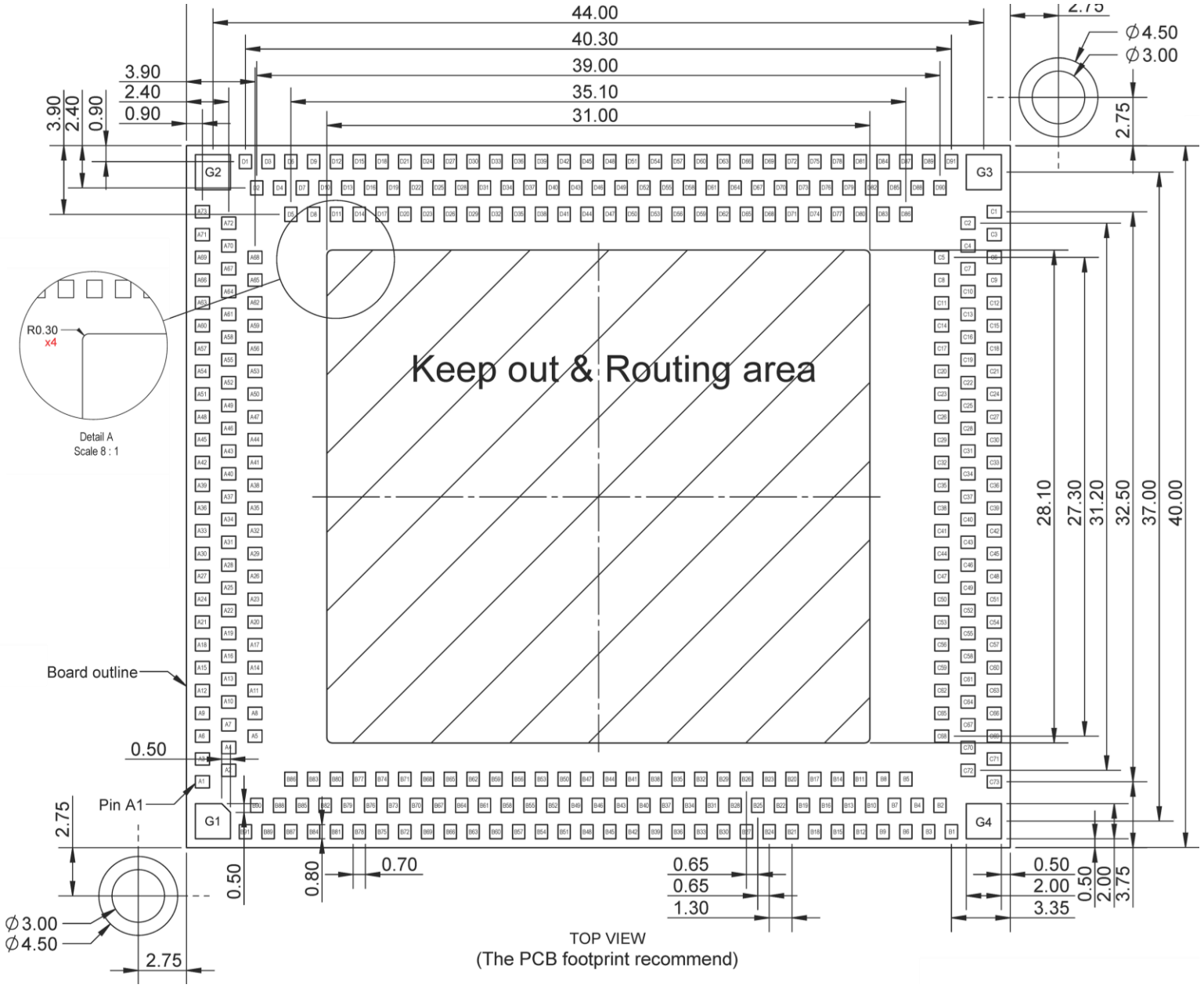

Figure 6: Recommend PCB footprint for Host PCB

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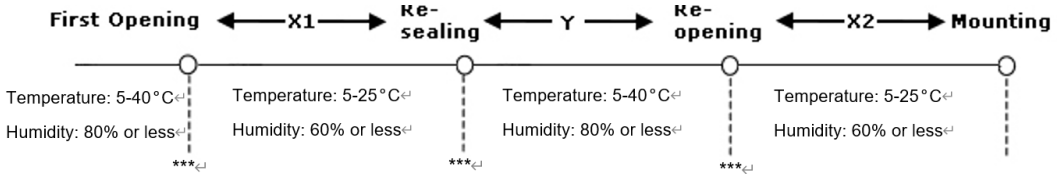
11 HANDLING AND ASSEMBLY INSTRUCTIONS

11.1 Recommended Storage, Handling, Baking, and Reflow Profile

1. **Required Storage Conditions:**
   - **Prior to Opening the Dry Packing**
     The following are required storage conditions prior to opening the dry packing:
     - · Normal temperature: 5~40℃
     - · Normal humidity: 80% (Relative humidity) or less
     - · Storage period: One year or less
   - **After Opening the Dry Packing**
     The following are required storage conditions after opening the dry packing (to prevent moisture absorption):
     - · Storage conditions for one-time soldering:
       - Temperature: 5-25°C
       - Humidity: 60% or less
       - Period: 72 hours or less after opening
     - · Storage conditions for two-time soldering
       - Storage conditions following opening and prior to performing the 1st reflow:
         - Temperature: 5-25°C
         - Humidity: 60% or less
         - Period: A hours or less after opening
       - Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow
         - Temperature: 5-25°C
         - Humidity: 60% or less
         - Period: B hours or less after completion of the 1st reflow

         Note: Should keep A+B within 72 hours.
   - **Temporary Storage Requirements after Opening**
     The following are temporary storage requirements after opening:
     - Only re-store the devices once prior to soldering.
     - Use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using vacuumed heat-sealing**.**

       The following indicates the required storage period, temperature, and humidity for this temporary storage:



Note: X1+X2 – Refer to After Opening the Dry Packing storage requirements. X1+X2 should not exceed 72 hours.

Note: Y – Keep within two weeks or less.

2. **Baking Conditions**:
   Baking conditions and processes for the module follow the J-STD-033 standard which includes the following:
   - The calculated shelf life in a sealed bag is 12 months at <40℃ and <80% relative humidity.
   - Once the packaging is opened, the SOM must be mounted (per MSL4/Moisture Sensitivity Level 4) within 72 hours at <30℃ and <60% relative humidity.
   - If the SOM is not mounted within 72 hours or if, when the Dry pack is opened, the humidity indicator card displays >10% humidity, then the product must be baked for 48 hours at 125℃ (±5℃).

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3. **Reflow** profile**:**
   Convection reflow or IR/Convection reflow (one-time soldering or two-time soldering in air or nitrogen environment)
   - Measuring point – IC package surface

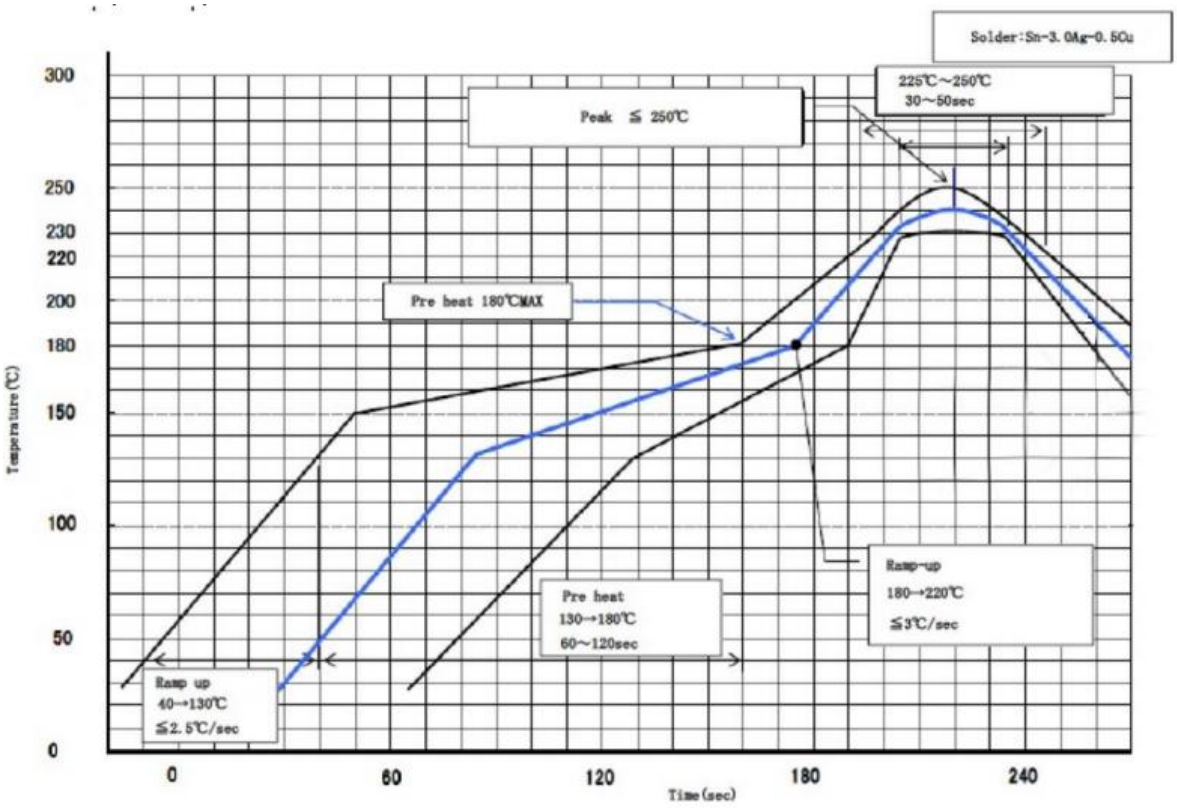

Figure 9: Recommend reflow profile

   - Temperature profile:
     - Ramp-up: 40-130°C less than 2.5°C /sec.
     - Pre-heat: 130-180°C 60-120 seconds, 180°C MAX.
     - Ramp-up: 189-220°C, less than 3°C /sec.
     - Peak temperature: 225~250°C, 30-50seconds, 250°C Max.
     - Ramp-down: Maximum 6°C /sec.

11.2 Others

- Stencil thickness: ≥ 0.125mm with one to one of pad dimension opening. (Reference the PCB footprint design)
- The coplanarity of the Summit SOM 8M Plus is <0.1mm on the PCB button. It is recommended to have supported carrier fixtures during reflow process to minimize the potential bow on the host PCB which causing poor or insufficient solder.
- The Summit SOM 8M Plus only allows one-time reflow process.

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12 REGULATORY

For regulatory information on the Summit SOM 8M Plus, see the Regulatory Information Guide, available on the Summit SOM 8M Plus product page at www.lairdconnect.com/summit-som-8m-plus

12.1 Regulatory IDs Summary

Model	US/FCC	Canada/IC	Japan
Summit SOM 8M Plus	SQG-SOM8MPLUS	3147A-SOM8MPLUS	201-210466

12.2 Certified Antennas

Model	Type	Connector	Peak Gain
Laird/NanoBlade-IP04 (Part# CAF94505)	PCB Dipole	IPEX U.FL	2 dBi (2.4-2.5 GHz), 3.9 dBi (5.15-5.35 GHz), 4 dBi (5.6 GHz)
Laird/Mini NanoBlade Flex (Part# MAF95310)	PCB Dipole	IPEX U.FL	2.8 dBi (2.4-2.5 GHz), 3.4 dBi (4.9-5.875 GHz)
Laird/Flex MIMO (Part# EFD2455A3S-10MHF1)	PCB Dipole	IPEX U.FL	1.7dBi (2.4-2.48GHz), 2.5dBi (4.9-5.9GHz)
Laird/FlexPIFA (Part# 001-0016)	PIFA	IPEX U.FL	2.5dBi (2.4-2.48GHz), 3dBi (4.9-5.9GHz)
Laird/2.4GHz/5GHz Dipole Antenna (Part# 001-0009)	Dipole	RP-SMA Male	2dBi (2.4-2.5GHz), 2dBi (5.15-5.85GHz)

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13 Ordering Information

Order Model	Description
453-00070R	Module, Summit SOM 8M Plus, Quad Core CPU, 512MB LPDDR4, 8GB eMMC, Tape and Reel
453-00070C	Module, Summit SOM 8M Plus, Quad Core CPU, 512MB LPDDR4, 8GB eMMC, Cut Tape
453-00071R	Module, Summit SOM 8M Plus, Quad Core CPU, 1GB LPDDR4, 8GB eMMC, Tape and Reel
453-00071C	Module, Summit SOM 8M Plus, Quad Core CPU, 1GB LPDDR4, 8GB eMMC, Cut Tape
453-00072R	Module, Summit SOM 8M Plus, Quad Core CPU, 2GB LPDDR4, 16GB eMMC, Tape and Reel
453-00072C	Module, Summit SOM 8M Plus, Quad Core CPU, 2GB LPDDR4, 16GB eMMC, Cut Tape
453-00070-K1	Development Kit, Summit SOM 8M Plus, Quad Core CPU, 512MB LPDDR4, 8GB eMMC
453-00071-K1	Development Kit, Summit SOM 8M Plus, Quad Core CPU, 1GB LPDDR4, 8GB eMMC
453-00072-K1	Development Kit, Summit SOM 8M Plus, Quad Core CPU, 2GB LPDDR4, 16GB eMMC
110-00770	Heat Sink, 41.5mm x 39.5mm x 22.54mm, Summit SOM 8M Plus

13.1 General Comments

This is a preliminary datasheet. Please check with Laird Connectivity for the latest information before commencing a design. If in doubt, ask.

cs **Česky [Czech]**	*[Jméno výrobce]* tímto prohlašuje, že tento *[typ zařízení]* je ve shodě se základními požadavky a dalšími příslušnými ustanoveními směrnice 1999/5/ES.
da **Dansk [Danish]**	Undertegnede *[fabrikantens navn]* erklærer herved, at følgende udstyr *[udstyrets typebetegnelse]* overholder de væsentlige krav og øvrige relevante krav i direktiv 1999/5/EF.
de **Deutsch [German]**	Hiermit erklärt *[Name des Herstellers]*, dass sich das Gerät *[Gerätetyp]* in Übereinstimmung mit den grundlegenden Anforderungen und den übrigen einschlägigen Bestimmungen der Richtlinie 1999/5/EG befindet.
et **Eesti [Estonian]**	Käesolevaga kinnitab *[tootja nimi = name of manufacturer]* seadme *[seadme tüüp = type of equipment]* vastavust direktiivi 1999/5/EÜ põhinõuetele ja nimetatud direktiivist tulenevatele teistele asjakohastele sätetele.
en **English**	Hereby, *[name of manufacturer]*, declares that this *[type of equipment]* is in compliance with the essential requirements and other relevant provisions of Directive 1999/5/EC.
es **Español [Spanish]**	Por medio de la presente *[nombre del fabricante]* declara que el *[clase de equipo]* cumple con los requisitos esenciales y cualesquiera otras disposiciones aplicables o exigibles de la Directiva 1999/5/CE.
el **Ελληνική [Greek]**	ΜΕ ΤΗΝ ΠΑΡΟΥΣΑ *[name of manufacturer]* ΔΗΛΩΝΕΙ ΟΤΙ *[type of equipment]* ΣΥΜΜΟΡΦΩΝΕΤΑΙ ΠΡΟΣ ΤΙΣ ΟΥΣΙΩΔΕΙΣ ΑΠΑΙΤΗΣΕΙΣ ΚΑΙ ΤΙΣ ΛΟΙΠΕΣ ΣΧΕΤΙΚΕΣ ΔΙΑΤΑΞΕΙΣ ΤΗΣ ΟΔΗΓΙΑΣ 1999/5/ΕΚ.
fr **Français [French]**	Par la présente *[nom du fabricant]* déclare que l'appareil *[type d'appareil]* est conforme aux exigences essentielles et aux autres dispositions pertinentes de la directive 1999/5/CE.
it **Italiano [Italian]**	Con la presente *[nome del costruttore]* dichiara che questo *[tipo di apparecchio]* è conforme ai requisiti essenziali ed alle altre disposizioni pertinenti stabilite dalla direttiva 1999/5/CE.
Latviski [Latvian]	Aršo*[name of manufacturer /izgatavotājanosaukums]* deklarē, ka*[type of equipment / iekārtas tips]*atbilstDirektīvas 1999/5/EK būtiskajāmprasībām un citiemar to saistītajiemnoteikumiem.
Lietuvių [Lithuanian]	Šiuo *[manufacturer name]* deklaruoja, kad šis *[equipment type]* atitinka esminius reikalavimus ir kitas 1999/5/EB Direktyvos nuostatas.
nl **Nederlands [Dutch]**	Hierbij verklaart *[naam van de fabrikant]* dat het toestel *[type van toestel]* in overeenstemming is met de essentiële eisen en de andere relevante bepalingen van richtlijn 1999/5/EG.

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Malti [Maltese]	Hawnhekk, *[isem tal-manifattur]*, jiddikjara li dan *[il-mudel tal-prodott]* jikkonforma mal-ħtiġijiet essenzjali u ma provvedimenti oħrajn relevanti li hemm fid-Dirrettiva 1999/5/EC.
Magyar [Hungarian]	Alulírott, *[gyártó neve]* nyilatkozom, hogy a *[... típus]*megfelel a vonatkozó alapvetõ követelményeknek és az 1999/5/EC irányelv egyéb elõírásainak.
Polski [Polish]	Niniejszym *[nazwa producenta]* oświadcza, że *[nazwa wyrobu]* jest zgodny z zasadniczymi wymogami oraz pozostałymi stosownymi postanowieniami Dyrektywy 1999/5/EC.
Português [Portuguese]	*[Nome do fabricante]* declara que este *[tipo de equipamento]* está conforme com os requisitos essenciais e outras disposições da Directiva 1999/5/CE.
Slovensko [Slovenian]	*[Ime proizvajalca]* izjavlja, da je ta *[tip opreme]* v skladu z bistvenimi zahtevami in ostalimi relevantnimi določili direktive 1999/5/ES.
Slovensky [Slovak]	*[Menovýrobcu]*týmtovyhlasuje, že*[typzariadenia]*spĺňazákladnépožiadavky a všetkyprís lušnéustanoveniaSmernice 1999/5/ES.
Suomi [Finnish]	*[Valmistaja = manufacturer]* vakuuttaa täten että *[type of equipment = laitteen tyyppimerkintä]* tyyppinen laite on direktiivin 1999/5/EY oleellisten vaatimusten ja sitä koskevien direktiivin muiden ehtojen mukainen.
Svenska [Swedish]	Härmed intygar *[företag]* att denna *[utrustningstyp]* står I överensstämmelse med de väsentliga egenskapskrav och övriga relevanta bestämmelser som framgår av direktiv 1999/5/EG.

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14 BLUETOOTH SIG QUALIFICATION

14.1 Overview

The Summit SOM 8M Plus module is listed on the Bluetooth SIG website as a qualified Controller Subsystem.

Design Name	Owner	Declaration ID	Model Number	Link to listing on the SIG website
Summit SOM 8M Plus	Laird	D057225	453-00070	https://launchstudio.bluetooth.com/ListingDetails/143874
Summit SOM 8M Plus	Laird	D057225	453-00070-K1	https://launchstudio.bluetooth.com/ListingDetails/143874
Summit SOM 8M Plus	Laird	D057225	453-00071	https://launchstudio.bluetooth.com/ListingDetails/143874
Summit SOM 8M Plus	Laird	D057225	453-00071-K1	https://launchstudio.bluetooth.com/ListingDetails/143874
Summit SOM 8M Plus	Laird	D057225	453-00072	https://launchstudio.bluetooth.com/ListingDetails/143874
Summit SOM 8M Plus	Laird	D057225	453-00072-K1	https://launchstudio.bluetooth.com/ListingDetails/143874

It is a mandatory requirement of the Bluetooth Special Interest Group (SIG) that every product implementing Bluetooth technology has a Declaration ID. Every Bluetooth design is required to go through the qualification process, even when referencing a Bluetooth Design that already has its own Declaration ID. The Qualification Process requires each company to register as a member of the Bluetooth SIG – www.bluetooth.org

The following is a link to the Bluetooth Registration page: https://www.bluetooth.org/login/register/

For each Bluetooth Design, it is necessary to purchase a Declaration ID. This can be done before starting the new qualification, either through invoicing or credit card payment. The fees for the Declaration ID will depend on your membership status, please refer to the following webpage:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/fees

For a detailed procedure of how to obtain a new Declaration ID for your design, please refer to the following SIG document, (login is required to views this document):

https://www.bluetooth.org/DocMan/handlers/DownloadDoc.ashx?doc_id=283698&vId=317486

14.2 Qualification Steps When Referencing a Laird Connectivity Controller Subsystem Design

To qualify your product when referencing a Laird Connectivity Controller Subsystem design, follow these steps:

1. To start a listing, go to: https://www.bluetooth.org/tpg/QLI_SDoc.cfm

   Note: A user name and password are required to access this site.

2. In step 1, select the option, New Listing and Reference a Qualified Design.
3. Enter *99404* in the Controller Subsystem table entry.
4. Enter your complimentary Host Subsystem and optional Profile Subsystem QDID in the table entry.
5. Select your pre-paid Declaration ID from the drop-down menu or go to the Purchase Declaration ID page.

   Note: Unless the Declaration ID is pre-paid or purchased with a credit card, you cannot proceed until the SIG invoice is paid.

6. Once all the relevant sections of step 1 are finished, complete steps 2, 3, and 4 as described in the help document accessible from the site.

Your new design will be listed on the SIG website and you can print your Certificate and DoC.

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For further information please refer to the following training material:

https://www.bluetooth.org/en-us/test-qualification/qualification-overview/listing-process-updates

If you require assistance with the qualification process please contact our recommended Bluetooth Qualification Expert (BQE), Steve Flooks, steve.flooks@eurexuk.com.

15 Additional Assistance

Please contact your local sales representative or our support team for further assistance:

Laird Connectivity Support Center: https://www.lairdconnect.com/resources/support

Email: wireless.support@lairdconnectivity.com
Phone: Americas: +1-800-492-2320
Europe: +44-1628-858-940
Hong Kong: +852-2762-4823

Web: https://www.lairdconnect.com/products

Note: Information contained in this document is subject to change.