User's Manual

RZ/G2UL, RZ/A3UL, RZ/Five
SMARC Module Board

User's Manual: Hardware

Renesas Microprocessor
RZ Family / RZ/G, RZ/A Series

RTK9743U11C01000BE
RTK9743F01C01000BE
RTK9763U02C01000BE
RTK9763U02C01001BE

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Rev.1.01 Jul, 2022

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(Rev.5.0-1 October 2020)

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The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

1.1 Overview

This document describes a specification of the RZ/G2UL, RZ/A3UL and RZ/Five SMARC Module Board to evaluate the functions and performance of the Renesas Electronics microprocessor RZ/G2UL “R9A07G043U11GBG”, RZ/A3UL “R9A07G063U02GBG” and RZ/Five “R9A07G043F01GBG” and evaluate application software programs.

This document introduces 4 types of the SMARC Module Boards.

However, the RZ/G2UL SMARC Module Board (RTK9743U11C01000BE) will be mainly explained here. Please refer to the **section 5.1 “Type Name and Features of Each Board”** for the main features of each SMARC Module Board.

The RTK9743U11C01000BE complies with the SMARC v2.1 and has following features.

- It is mounted with the following external memories.

  DDR4 SDRAM: 1GB × 1pc

  QSPI flash memory: 128Mb × 1pc (*1)

  eMMC memory: 64GB × 1pc

  OctaRAM memory: 512Mb *1pc (*2)

  OctaFLASH memory: 1Gb * 1pc (*2)
- The microSD card slot is implemented and used as an eSD for boot.
- It is implemented a 5-output clock generator “5P35023”.
- It is implemented a PMIC “DA9062” as power supply circuit.
- The Ethernet PHY is implemented as standard and can send/receive data at 10/100/1000Mbps.
- Terminals not used on this board such as a USB connector, a LAN connector and a camera connector and so on are connected to the 314-pin 0.5-mm pitch connector, which can be used in conjunction with a Carrier Board.
- The 10-pin connector for ARM Cortex Debug is implemented for connection to debug interface.
- The 6-pin connector is implemented for connection to ADC interface.
- The 45-pin FFC/FPC connector is mounted as standard for connection to parallel output interface. (*3)

Note 1. The QSPI flash memoy is not supported on the RTK9763U02C01001BE.
Note 2. The OctaFlash and Octa RAM memories are supportted on the RTK9763U02C01001BE.
Note 3. The parallel output interface is not supported on the RTK9743F01C01000BE.

1.2 Configuration

Figure 1.1 shows an example of system configuration using the RTK9743U11C01000BE.

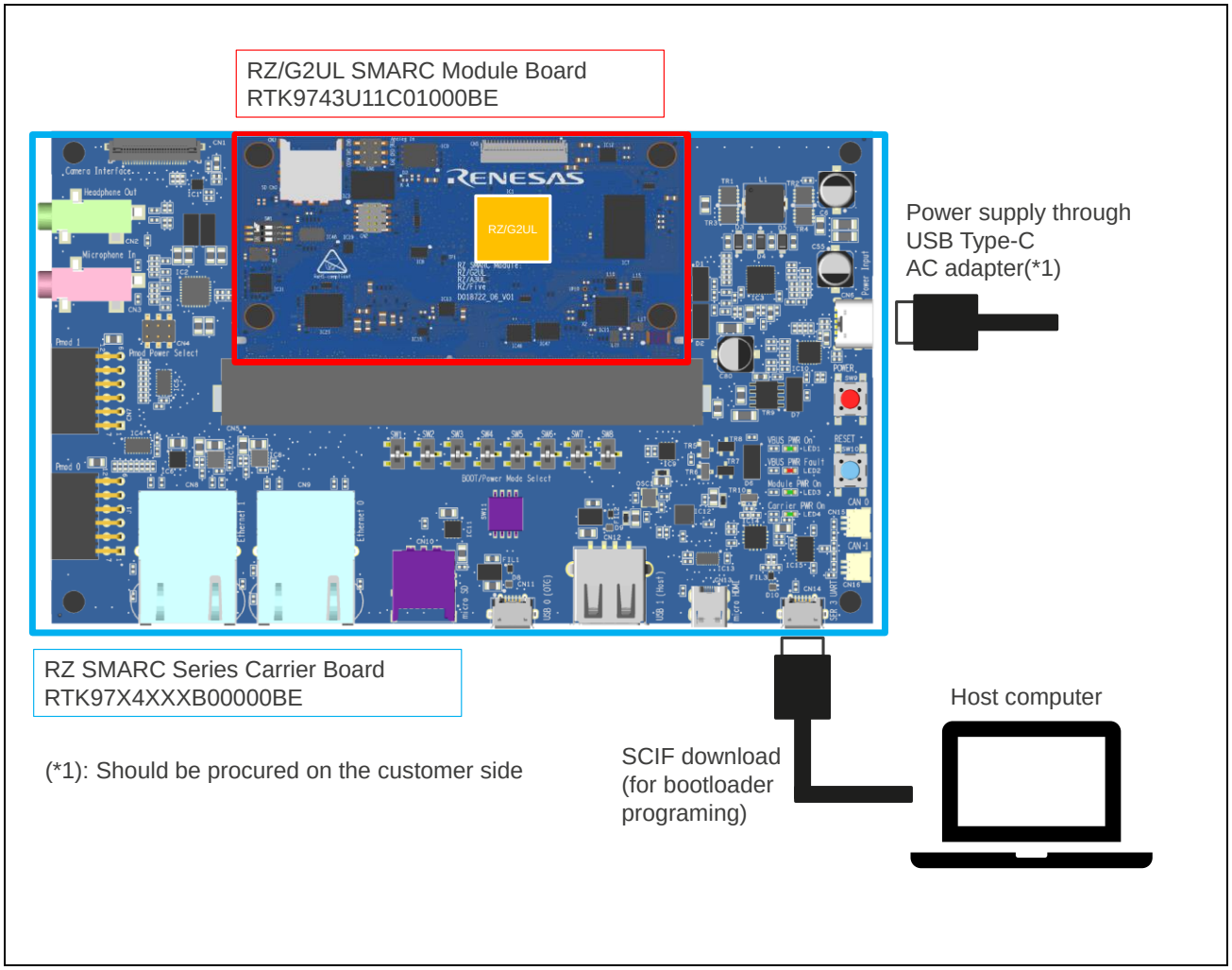


Figure 1.1 Example of System Configuration Using the RTK9743U11C01000BE

NOTE

The above example uses RTK9743U11C01000BE.

1.3 Features

1.3.1 RTK9743U11C01000BE (RZ/G2UL SMARC Module Board)

Table 1.1 shows the features of the RTK9743U11C01000BE.

Table 1.1 Features of the RTK9743U11C01000BE

Item	Details
CPU	RZ/G2UL Input (Xin) clock: 24MHz Arm Cortex-A55 clock: 1.0GHz Arm Cortex-M33 clock: 200MHz AXI-bus clock: 200MHz APB-bus clock: 100MHz Internal memory Instruction cache: 32KB Data cache: 32KB Power voltage: 1.1V, I/O: 3.3V 361-Pin PBGA 0.5-mm pitch
Memory	QSPI flash memory: 128Mb * 1pc DDR4 SDRAM: 1GB * 1pc eMMC memory: 64GB * 1pc
Clock IC	Clock generator: 1pc
Ethernet IC	Ethernet PHY: 2pcs
Connector	microSD card slot (4 bits): 1pc 10-pin connector for JTAG: 1pc 6-pin connector for ADC: 1pc SMARC edge connector (314 pins): 1pc FFC/FPC connector (45pin): 1pc
Switch	System setting DIP switch: 3 bits
Circuit board specifications	Dimensions: 82 mm * 50 mm Mount: Double-sided mounting (6 layers)

1.3.2 RTK9763U02C01000BE (RZ/A3UL SMARC Module Board QSPI Edition)

Table 1.2 shows the features of the RTK9763U02C01000BE.

Table 1.2 Features of the RTK9763U02C01000BE

Item	Details
CPU	RZ/A3UL Input (Xin) clock: 24MHz Arm Cortex-A55 clock: 1.0GHz AXI-bus clock: 200MHz APB-bus clock: 100MHz Internal memory Instruction cache: 32KB Data cache: 32KB Power voltage: 1.1V, I/O: 3.3V 361-Pin PBGA 0.5-mm pitch
Memory	QSPI flash memory: 128Mb * 1pc DDR4 SDRAM: 1GB * 1pc eMMC memory: 64GB * 1pc
Clock IC	Clock generator: 1pc
Ethernet IC	Ethernet PHY: 2pcs
Connector	microSD card slot (4 bits): 1pc 10-pin connector for JTAG: 1pc 6-pin connector for ADC: 1pc SMARC edge connector (314 pins): 1pc FFC/FPC connector (45pin): 1pc
Switch	System setting DIP switch: 3 bits
Circuit board specifications	Dimensions: 82 mm * 50 mm Mount: Double-sided mounting (6 layers)

1.3.3 RTK9763U02C01001BE (RZ/A3UL SMARC Module Board OCTAL Edition)

Table 1.3 shows the features of the RTK9763U02C01001BE.

Table 1.3 Features of the RTK9763U02C01001BE

Item	Details
CPU	RZ/A3UL Input (Xin) clock: 24MHz Arm Cortex-A55 clock: 1.0GHz AXI-bus clock: 200MHz APB-bus clock: 100MHz Internal memory Instruction cache: 32KB Data cache: 32KB Power voltage: 1.1V, I/O: 3.3V 361-Pin PBGA 0.5-mm pitch
Memory	DDR4 SDRAM: 1GB * 1pc eMMC memory: 64GB * 1pc OctaRAM memory: 512Mb *1pc OctaFLASH memory: 1Gb * 1pc
Clock IC	Clock generator: 1pc
Ethernet IC	Ethernet PHY: 2pcs
Connector	microSD card slot (4 bits): 1pc 10-pin connector for JTAG: 1pc 6-pin connector for ADC: 1pc SMARC edge connector (314 pins): 1pc FFC/FPC connector (45pin): 1pc
Switch	System setting DIP switch: 3 bits
Circuit board specifications	Dimensions: 82 mm * 50 mm Mount: Double-sided mounting (6 layers)

1.3.4 RTK9743F01C01000BE (RZ/Five SMARC Module Board)

Table 1.4 shows the features of the RTK9743F01C01000BE.

Table 1.4 Features of the RTK9743F01C01000BE

Item	Details
CPU	RZ/Five Input (Xin) clock: 24MHz AndesCore™ AX45MP clock: 1.0GHz AXI-bus clock: 200MHz APB-bus clock: 100MHz Internal memory Instruction cache: 32KB Data cache: 32KB Power voltage: 1.1V, I/O: 3.3V 361-Pin PBGA 0.5-mm pitch
Memory	QSPI flash memory: 128Mb * 1pc DDR4 SDRAM: 1GB * 1pc eMMC memory: 64GB * 1pc
Clock IC	Clock generator: 1pc
Ethernet IC	Ethernet PHY: 2pcs
Connector	microSD card slot (4 bits): 1pc 10-pin connector for JTAG: 1pc 6-pin connector for ADC: 1pc SMARC edge connector (314 pins): 1pc FFC/FPC connector (45pin): 1pc (*1)
Switch	System setting DIP switch: 3 bits
Circuit board specifications	Dimensions: 82 mm * 50 mm Mount: Double-sided mounting (6 layers)

Note 1. The parallel output interface is not supported on the RTK9743F01C01000BE.

1.4 Physical View

Figure 1.2 and **Figure 1.3** show the top and bottom views of the RTK9743U11C01000BE.

Figure 1.2 Top View of the RTK9743U11C01000BE

NOTE

This picture is of the RTK9743U11C01000BE.

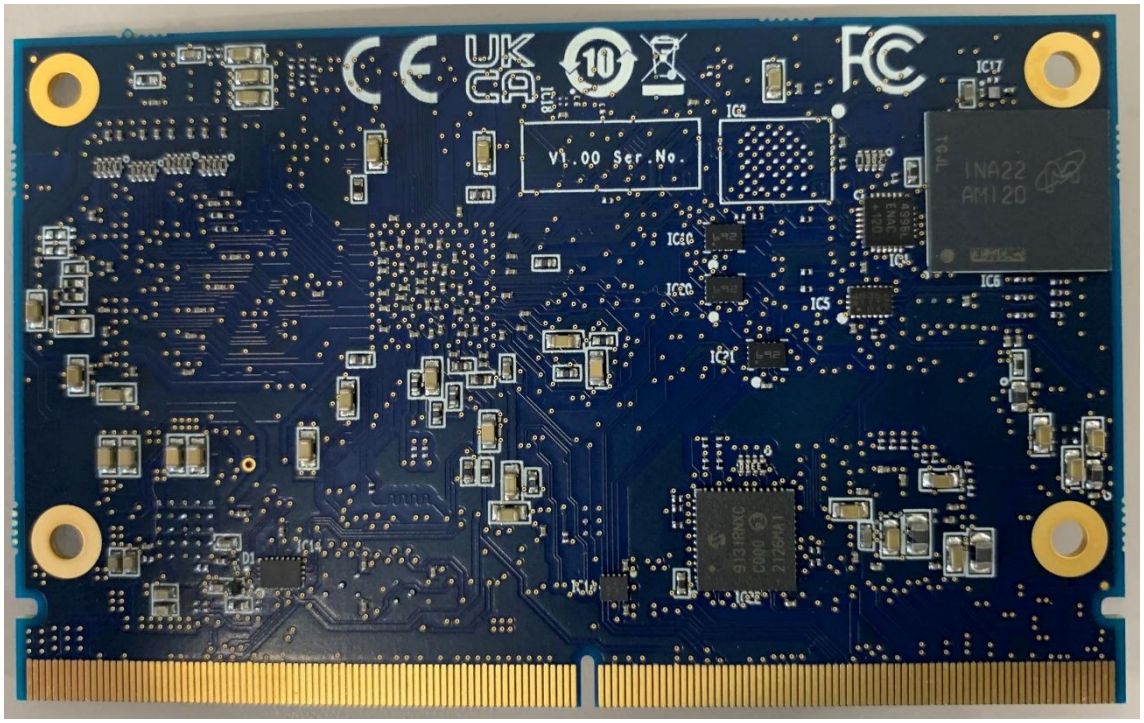


Figure 1.3 Bottom View of the RTK9743U11C01000BE

NOTE

This picture is of the RTK9743U11C01000BE.

1.5 Block Diagram

1.5.1 RTK9743U11C01000BE (RZ/G2UL SMARC Module Board)

Figure 1.4 shows the block diagram of the RTK9743U11C01000BE.

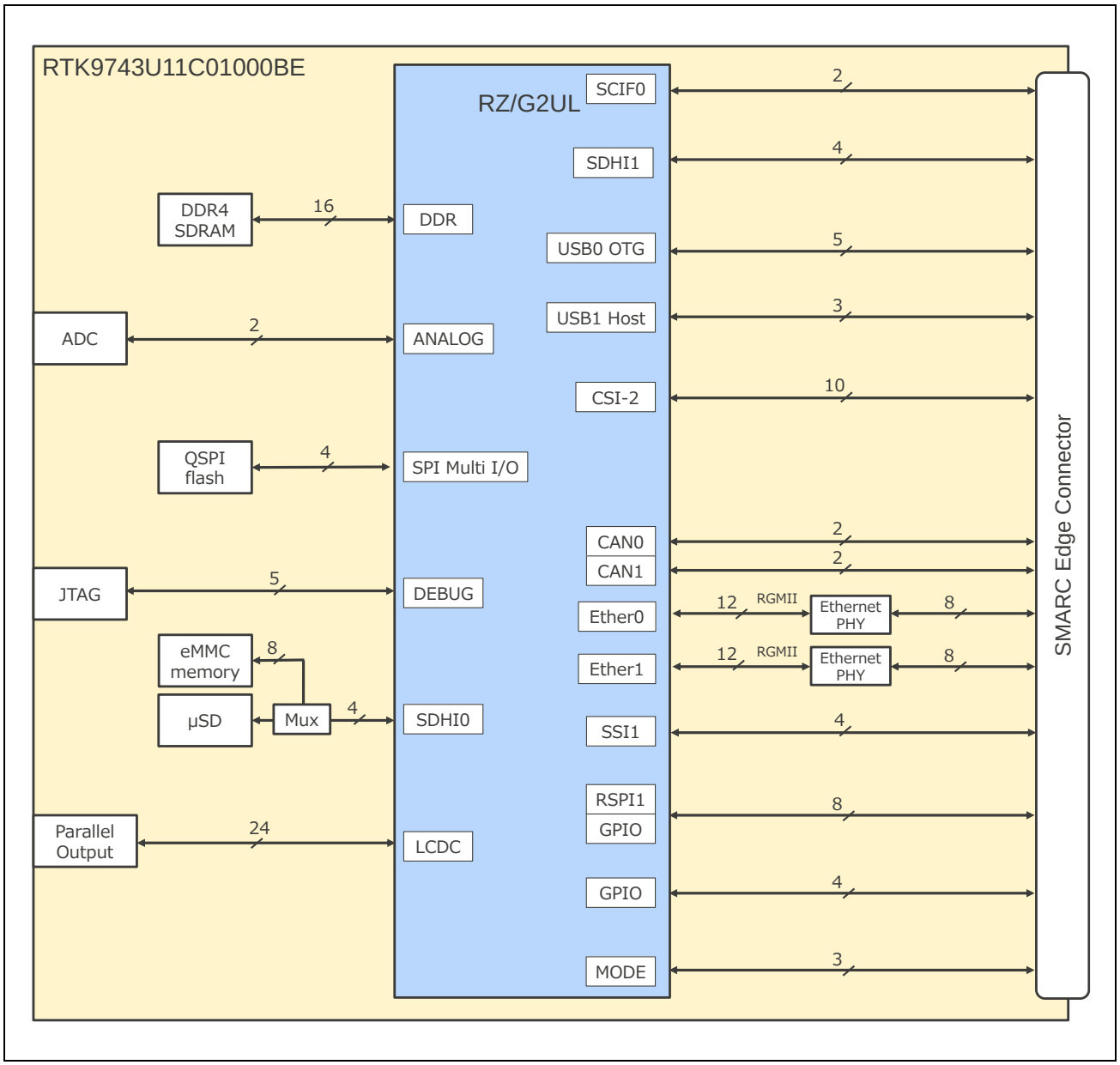


Figure 1.4 Block Diagram of the RTK9743U11C01000BE

1.5.2 RTK9763U02C01000BE (RZ/A3UL SMARC Module Board QSPI Edition)

Figure 1.5 shows the block diagram of the RTK9763U02C01000BE.

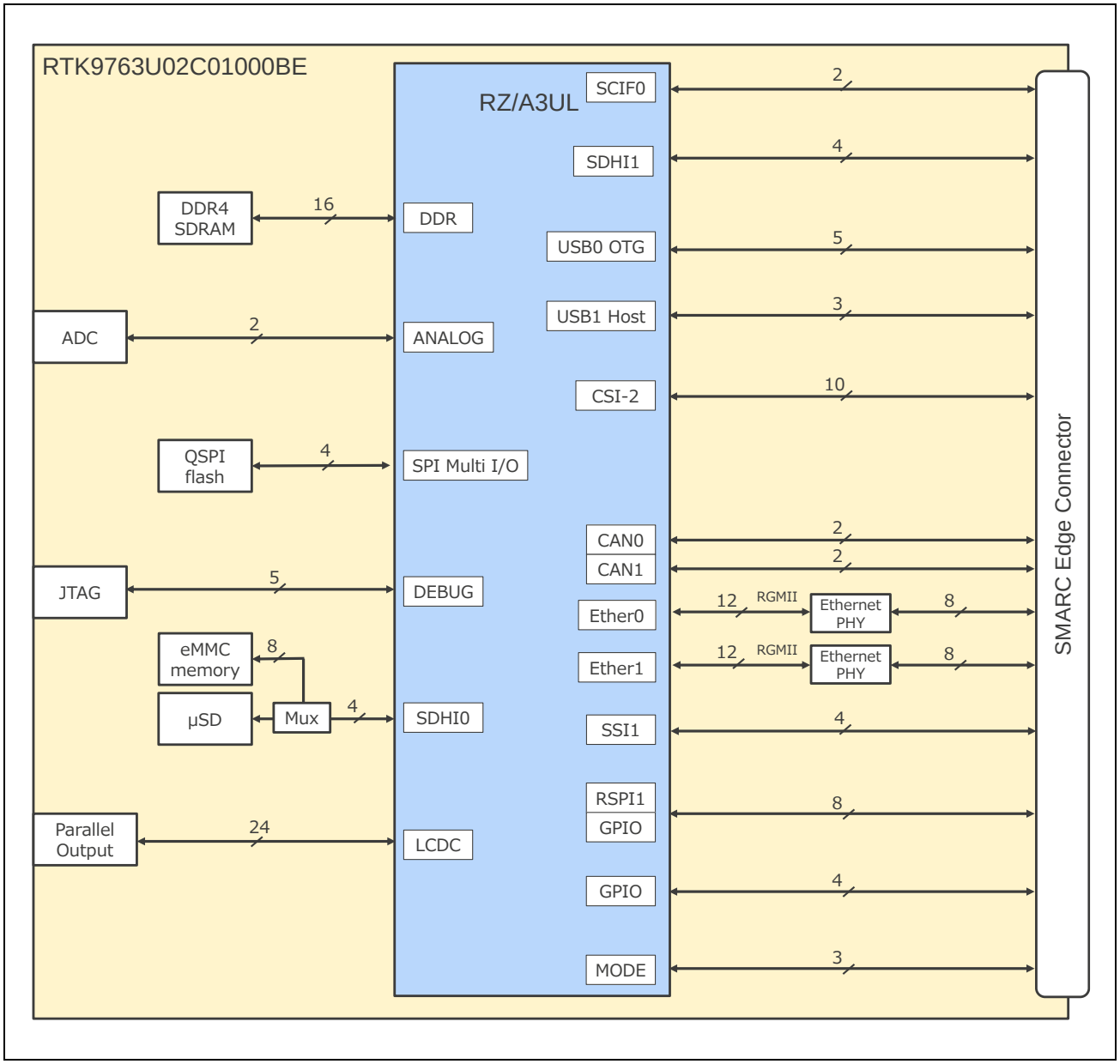


Figure 1.5 Block Diagram of the RTK9763U02C01000BE

1.5.3 RTK9763U02C01001BE (RZ/A3UL SMARC Module Board OCTAL Edition)

Figure 1.6 shows the block diagram of the RTK9763U02C01001BE.

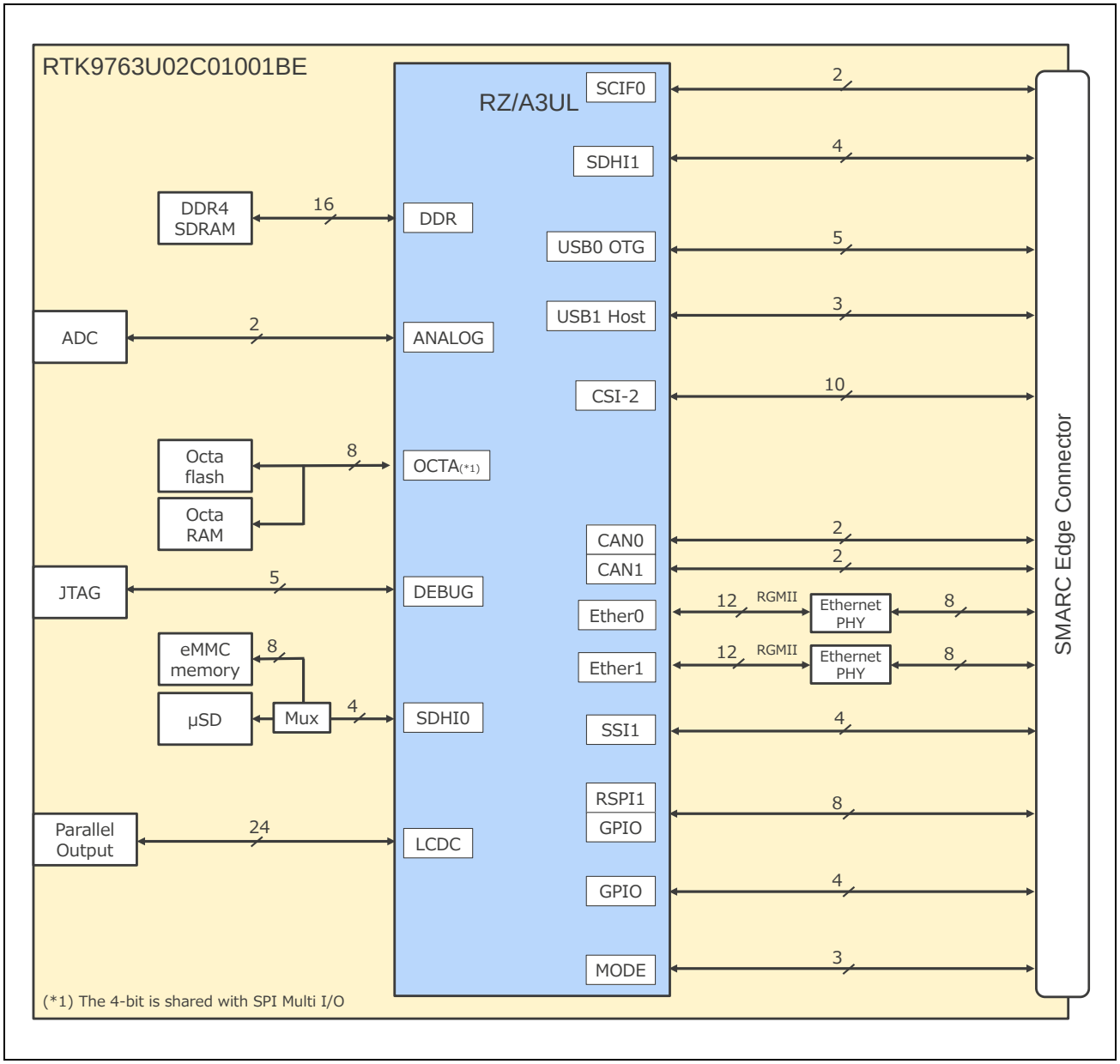


Figure 1.6 Block Diagram of the RTK9763U02C01001BE

1.5.4 RTK9743F01C01000BE (RZ/Five SMARC Module Board)

Figure 1.7 shows the block diagram of the RTK9743F01C01000BE.

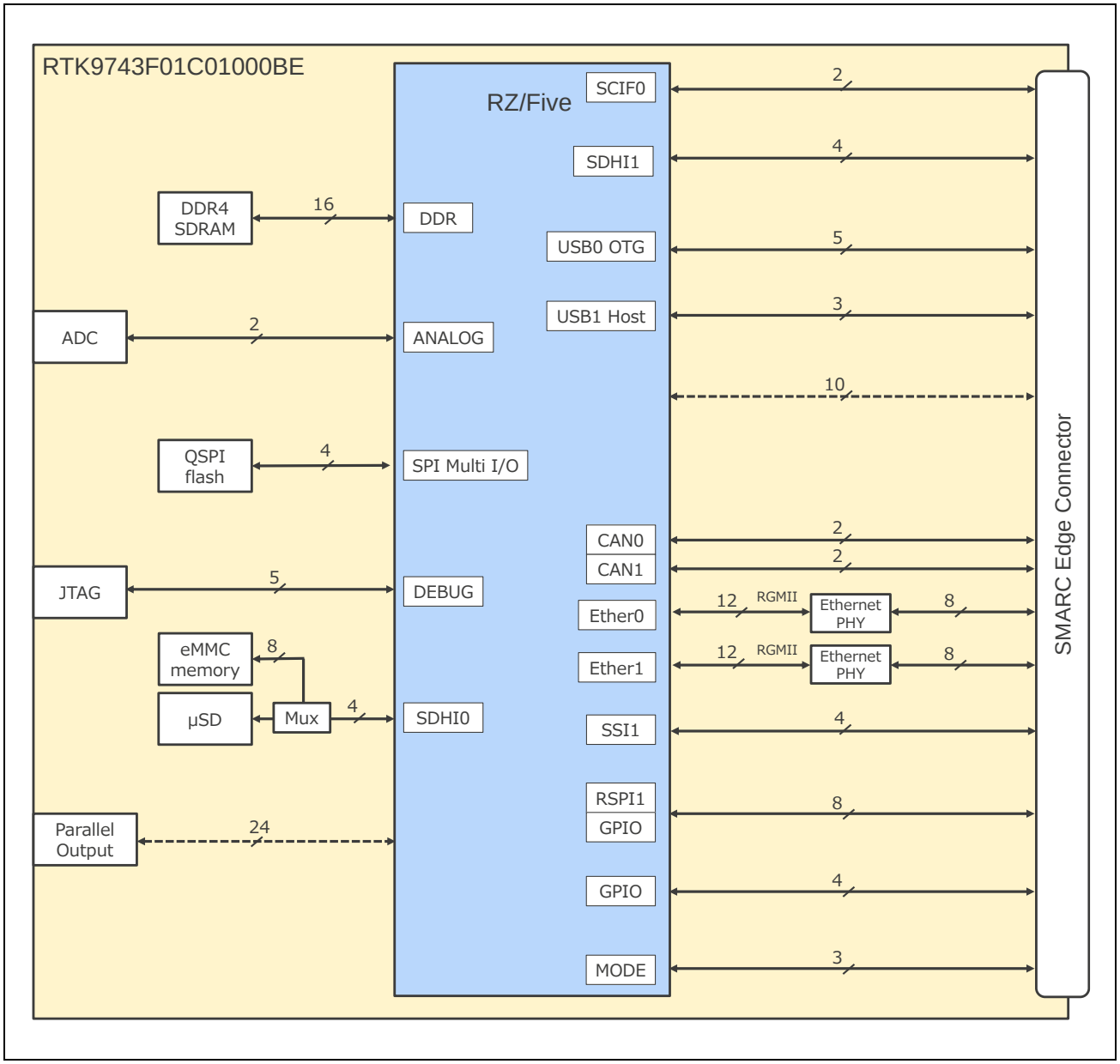


Figure 1.7 Block Diagram of the RTK9743F01C01000BE

1.6 Component Layout

Figure 1.8 and **Figure 1.9** show the layout of main components of the RTK9743U11C01000BE.

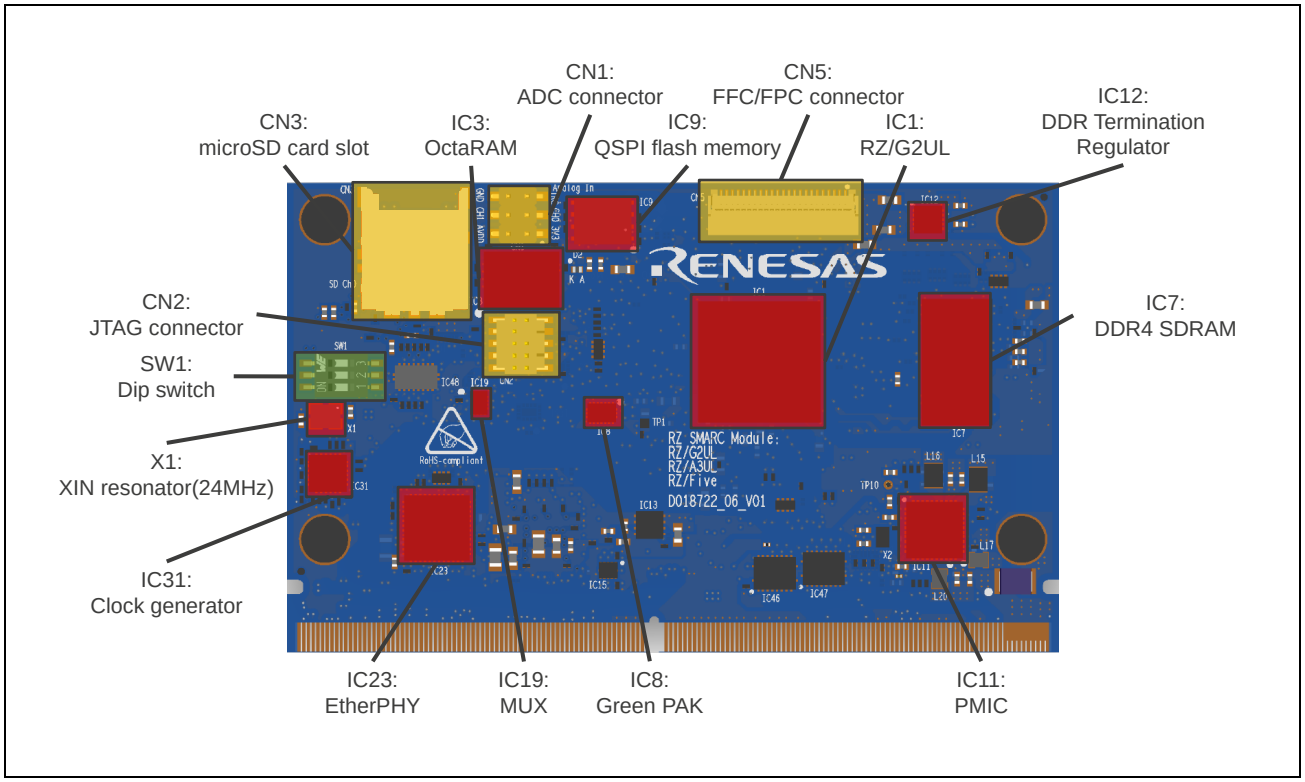


Figure 1.8 Layout of Components of the RTK9743U11C01000BE (Top View)

NOTE

The layout of this top view is of the RTK9743U11C01000BE.

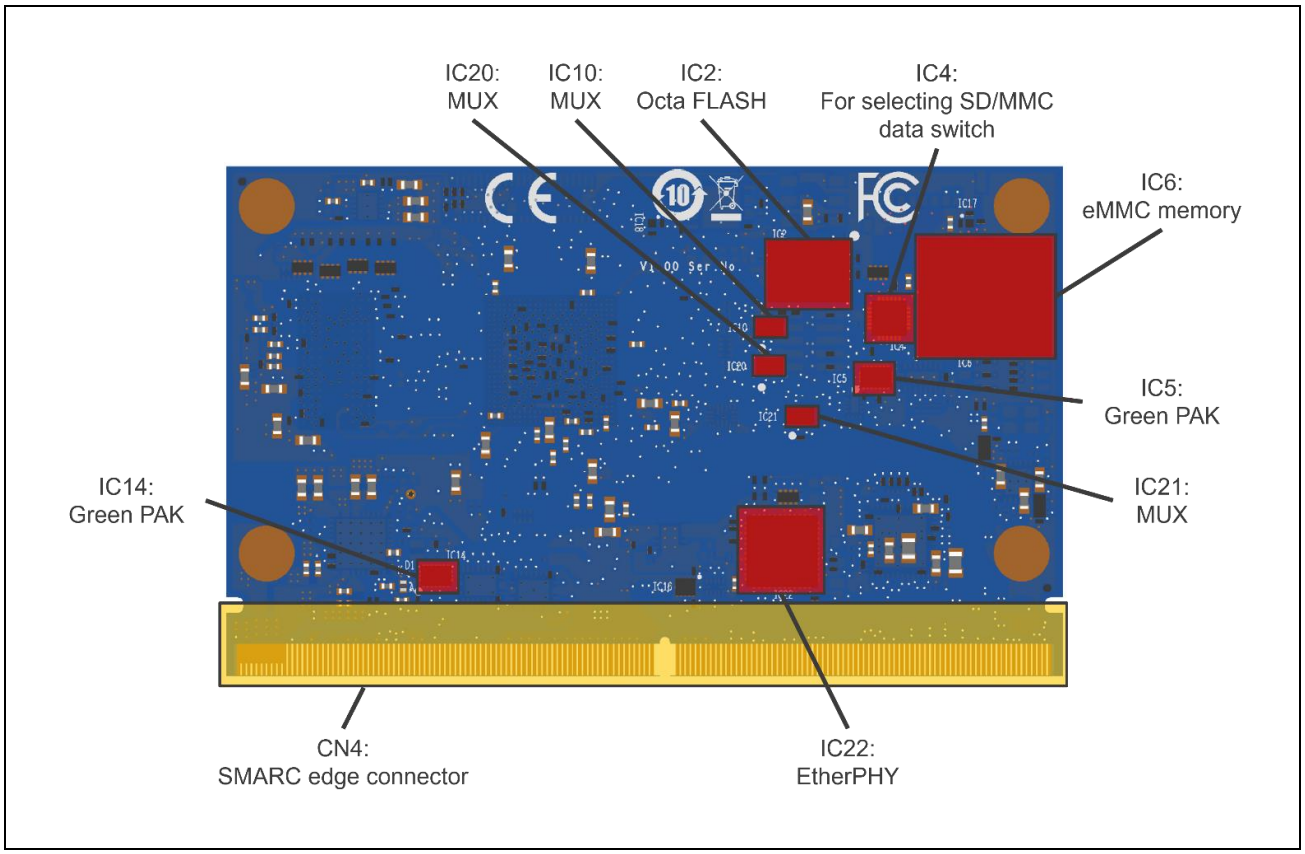


Figure 1.9 Layout of Components of the RTK9743U11C01000BE (Bottom View)

NOTE

The layout of this bottom view is of the RTK9743U11C01000BE.

Table 1.5 and **Table 1.6** list main components mounted on the RTK9743U11C01000BE.

Table 1.5 Main Components on the RTK9743U11C01000BE (1) IC

Component Number	Component Name	Type (Manufacturer)
IC1	MPU	R9A07G043U11GBG (Renesas Electronics)
IC2(*1)	OctaFLASH Memory	MX66UW1G45GXDQ00 (Macronix)
IC3(*1)	OctaRAM Memory	APS51208N-OCHx-BD (AP Memory)
IC4	Data switch IC	MAX4996LETG+ (MAXIM)
IC5	GreenPAK for Power/Reset	SLG7RN45356 (Renesas Electronics)
IC6	eMMC memory	MTFC64GASAQHD-IT (Micron)
IC7	DDR4 SDRAM	MT40A512M16LY-062E:E (Micron)
IC8	GreenPAK for USB/Ethernet Logic	SLG7RN45315 (Renesas Electronics)
IC9	QSPI flash memory	AT25QL128A_MHE (Renesas Electronics)
IC10, IC19 IC20, IC21	Quad SPDT Switch IC	STG3692QTR (STMicroelectronics)
IC11	PMIC	DA9062 (Renesas Electronics)
IC12	DDR Termination Regulator	NCP51200MNTXG (On Semiconductor)
IC14	GreenPAK for Boot Mode	SLG7RN45314 (Renesas Electronics)
IC22	Ethernet PHY	KSZ9131RNXC (Microchip)
IC23	Ethernet PHY	KSZ9131RNXC (Microchip)
IC31	Clock generator	5P35023B-629NLGI (Renesas Electronics)
X1	Crystal resonator for XIN	FL2400022 (Diodes Inc)

Note 1. The RTK9743U11C01000BE is not implemented.

Table 1.6 Main Components on the RTK9743U11C01000BE (2) Connector

Components Number	Component Name	Type (Manufacturer)
CN1	ADC connector (6pin)	M22-5320305 (HARWIN)
CN2	JTAG connector (10pin)	FTSH-105-01-F-DV-007-K (Samtec)
CN3	microSD card slot	504077-1891 (Molex)
CN4	SMARC edge connector (314pin)	
CN5	FFC/FPC connector (45pin)	FH23-45S-0.3SHAW(05) (HIROSE)

1.7 Absolute Maximum Ratings

Table 1.7 lists absolute maximum ratings of the RTK9743U11C01000BE.

Table 1.7 Absolute Maximum Ratings of the RTK9743U11C01000BE

Symbol	Item	Rated Value	Note
VDD_IN	power voltage	5.25V	Reference: Vss
—	Maximum power consumption	3A	Includes continuous RZ SMARC Series Carrier Board current consumption
Topr	Operating ambient temperature*1	0°C to 50°C	Do not expose to condensation or corrosive gases
Tstg	Storage temperature*1	-10°C to 60°C	Do not expose to condensation or corrosive gases

Note 1. Ambient temperature is the air temperature at a position as close to the board as possible.

1.8 Operating Condition

Table 1.8 lists operating conditions of the RTK9743U11C01000BE.

Table 1.8 Operating Conditions of the RTK9743U11C01000BE

Symbol	Item	Rated Value	Note
VDD_IN	Power volotage	3.0V to 5.25V	Reference: SMARC v2.1 specification
Topr	Operating ambient temperature*1	0°C to 40°C	Do not expose to condensation or corrosive gases

Note 1. Ambient temperature is the air temperature at a position as close to the board as possible.

2. Functional Specifications

2.1 Overview of Functions

Table 2.1 lists function modules of the RTK9743U11C01000BE.

Table 2.1 Function Modules of the RTK9743U11C01000BE

Section	Function	Description
2.2	**MPU**	RZ/G2UL Input (Xin) clock: 24MHz Arm Cortex-A55 clock: 1.0GHz Arm Cortex-M33 clock: 200MHz AXI-bus clock: 200MHz APB-bus clock: 100MHz
2.3	**Memory**	QSPI flash memory: 128Mb * 1pc (*1) DDR4 SDRAM: 1GB * 1pc eMMC memory: 64GB * 1pc (See **section 2.11** for details.) OctaRAM memory: 512Mb *1pc (*2) OctaFLASH memory: 1Gb * 1pc (*2)
2.4	**Gigabit Ethernet Interface**	Connection between the Ethernet controller (E-MAC) and LAN connector via Ethernet PHY
2.5	**ADC Interface**	Connection between ADC module and connector
2.6	**Clock Configuration**	System clock configuration
2.7	**Reset Control**	Reset control for RZ/G2UL mounted on the RTK9743U11C01000BE.
2.8	**Power Supply Configuration**	System power supply configuration of the RTK9743U11C01000BE and the RTK97X4XXXB00000BE
2.9	**PMIC**	Connection between RZ/G2UL and PMIC
2.10	**Debug Interface**	Connection between Debug Interface and connector
2.11	**SD/MMC Host Interface**	Connection between SD/MMC Host Interface (SDHI) channel 0 and microSD card slot
2.12	**GreenPAK**	SLG7RN45314(Boot Mode): 1pc SLG7RN45315(USB/Etehrnet Logic): 1pc SLG7RN45356(Power/Reset): 1pc
2.13 (*3)	**Parallel Output Interface**	Connection between Parallel Output Interface and connector
—	Operating specification	Connectors and switches Details are described in **Section 3**

Note 1. The QSPI flash memoy is not supported on the RTK9763U02C01001BE.

Note 2. The OctaFlash and Octa RAM memories are supported on the RTK9763U02C01001BE.

Note 3. The parallel output interface is not supported on the RTK9743F01C01000BE.

2.2 MPU

2.2.1 Overview of RZ/G2UL

The RTK9743U11C01000BE contains a 64-bit microprocessor RZ/G2UL that runs in synchronization with the CPU clock (max.1.0 GHz).

2.2.2 Overview of RZ/A3UL

The RTK9763U02C01000BE and RTK9763U02C01001BE contain a 64-bit microprocessor RZ/A3UL that runs in synchronization with the CPU clock (max.1.0 GHz).

2.2.3 Overview of RZ/Five

The RTK9743F01C01000BE contains a 64-bit microprocessor RZ/Five that runs in synchronization with the CPU clock (max.1.0 GHz).

2.2.4 List of Pin Functions

As described in the section1.1, RZ/G2UL is available in pin-compatible with RZ/A3UL and RZ/Five.

Table 2.2 lists pin functions of each product used in each Module Board.

Table 2.2 List of Pin Function Selection Used on Each Module Board (1/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
F17	ADC_AVDD18	ADC_AVDD18	ADC_AVDD18	NC	1.8V *Note*: Unused in case of RZ/Five	—	—
B18	ADC_CH0	ADC_CH0	ADC_CH0	NC	Pin connector (CN1) for ADC input *Note*: Unused in case of RZ/Five	—	—
A18	ADC_CH1	ADC_CH1	ADC_CH1	NC	Pin connector (CN1) for ADC input *Note*: Unused in case of RZ/Five	—	—
A9	AUDIO_CLK1	AUDIO_CLK1	AUDIO_CLK1	AUDIO_CLK1	Connected to clock generator (IC31), used as CD sampling rate 44.1KHz refclock 11.2896 MHz	—	—
B8	AUDIO_CLK2	AUDIO_CLK2	AUDIO_CLK2	AUDIO_CLK2	Connected to clock generator (IC31), used as DVD sampling rate 48.0KHz refclock 12.2880MHz	—	—
AE22	BSCANP	BSCANP	BSCANP	BSCANP	Initial setting: 0 (Pull down), should be controllable by resistor.	—	—
AD21	VSS	VSS	VSS	VSS	GND	—	—
AE11	CSI_CLKN	CSI_CLKN	CSI_CLKN	NC	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1) *Note*: Unused in case of RZ/Five	P4	CSI1_CK-
AD11	CSI_CLKP	CSI_CLKP	CSI_CLKP	NC	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1) *Note*: Unused in case of RZ/Five	P3	CSI1_CK+
AE12	CSI_DATA0_N	CSI_DATA0_N	CSI_DATA0_N	NC	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1) *Note*: Unused in case of RZ/Five	P8	CSI1_RX0-

Table 2.2 List of Pin Function Selection Used on Each Module Board (2/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AD12	CSI_DATA0_P	CSI_DATA0_P	CSI_DATA0_P	NC	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1) *Note*: Unused in case of RZ/Five	P7	CSI1_RX0+
AE10	CSI_DATA1_N	CSI_DATA1_N	CSI_DATA1_N	NC	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1) *Note*: Unused in case of RZ/Five	P11	CSI1_RX1-
AD10	CSI_DATA1_P	CSI_DATA1_P	CSI_DATA1_P	NC	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1) *Note*: Unused in case of RZ/Five	P10	CSI1_RX1+
AE13	CSI_DATA2_N	CSI_DATA2_N	CSI_DATA2_N	ADC_CH0	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1) *Note*: In case of RZ/Five, this pin is used as ADC_CH0. Removed a resiter (R8) and mounted a resistor (R10) for CSI/ADC options.	P14	CSI1_RX2-
AD13	CSI_DATA2_P	CSI_DATA2_P	CSI_DATA2_P	ADC_CH1	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1) *Note*: In case of RZ/Five, this pin is used as ADC_CH1. Removed a resiter (R9) and mounted a resistor (R11) for CSI/ADC options.	P13	CSI1_RX2+
AE9	CSI_DATA3_N	CSI_DATA3_N	CSI_DATA3_N	NC	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1) *Note*: Unused in case of RZ/Five	P17	CSI1_RX3-
AD9	CSI_DATA3_P	CSI_DATA3_P	CSI_DATA3_P	NC	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1) *Note*: Unused in case of RZ/Five	P16	CSI1_RX3+
F17	ADC_AVDD18	ADC_AVDD18	ADC_AVDD18	NC	1.8V *Note*: Unused in case of RZ/Five	—	—
Y11	CSI_VDD18	CSI_VDD18	CSI_VDD18	NC	1.8V *Note*: Unused in case of RZ/Five	—	—

Table 2.2 List of Pin Function Selection Used on Each Module Board (3/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
Y12	CSI_VDD18	CSI_VDD18	CSI_VDD18	NC	1.8V *Note*: Unused in case of RZ/Five	—	—
E25	DDR_ADDR0	DDR_ADDR0	DDR_ADDR0	SD1_CD	DDR4 SDRAM (IC7)	—	—
K25	DDR_ADDR1	DDR_ADDR1	DDR_ADDR1	DDR_ADDR1	DDR4 SDRAM (IC7)	—	—
P23	DDR_ADDR10	DDR_ADDR10	DDR_ADDR10	DDR_ADDR10	DDR4 SDRAM (IC7)	—	—
H25	DDR_ADDR11	DDR_ADDR11	DDR_ADDR11	DDR_ADDR11	DDR4 SDRAM (IC7)	—	—
N23	DDR_ADDR12	DDR_ADDR12	DDR_ADDR12	DDR_ADDR12	DDR4 SDRAM (IC7)	—	—
D23	DDR_ADDR13	DDR_ADDR13	DDR_ADDR13	DDR_ADDR13	DDR4 SDRAM (IC7)	—	—
H23	DDR_ADDR14	DDR_ADDR14	DDR_ADDR14	DDR_ADDR14	DDR4 SDRAM (IC7)	—	—
D25	DDR_ADDR15	DDR_ADDR15	DDR_ADDR15	DDR_ADDR15	DDR4 SDRAM (IC7)	—	—
C25	DDR_ADDR2	DDR_ADDR2	DDR_ADDR2	DDR_ADDR2	DDR4 SDRAM (IC7)	—	—
J25	DDR_ADDR6	DDR_ADDR6	DDR_ADDR6	DDR_ADDR6	DDR4 SDRAM (IC7)	—	—
A24	DDR_ADDR7	DDR_ADDR7	DDR_ADDR7	DDR_ADDR7	DDR4 SDRAM (IC7)	—	—
F25	DDR_ADDR8	DDR_ADDR8	DDR_ADDR8	DDR_ADDR8	DDR4 SDRAM (IC7)	—	—
B24	DDR_ADDR9	DDR_ADDR9	DDR_ADDR9	DDR_ADDR9	DDR4 SDRAM (IC7)	—	—
E24	DDR_BA0	DDR_BA0	DDR_BA0	DDR_BA0	DDR4 SDRAM (IC7)	—	—
L24	DDR_BA1	DDR_BA1	DDR_BA1	DDR_BA1	DDR4 SDRAM (IC7)	—	—
F23	DDR_BA2	DDR_BA2	DDR_BA2	DDR_BA2	DDR4 SDRAM (IC7)	—	—
A23	DDR_ CALIBRATION	DDR_ CALIBRATION	DDR_ CALIBRATION	DDR_ CALIBRATION	DDR4 SDRAM (IC7)	—	—
J24	DDR_CAS#	DDR_CAS#	DDR_CAS#	DDR_CAS#	DDR4 SDRAM (IC7)	—	—
M25	DDR_CKE	DDR_CKE	DDR_CKE	DDR_CKE	DDR4 SDRAM (IC7)	—	—
P24	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR_CLK_N	DDR4 SDRAM (IC7)	—	—
P25	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR_CLK_P	DDR4 SDRAM (IC7)	—	—
N24	DDR_CS0#	DDR_CS0#	DDR_CS0#	DDR_CS0#	DDR4 SDRAM (IC7)	—	—
L23	DDR_CS1#	DDR_CS1#	DDR_CS1#	DDR_CS1#	DDR4 SDRAM (IC7)	—	—
U23	DDR_DM0	DDR_DM0	DDR_DM0	DDR_DM0	DDR4 SDRAM (IC7)	—	—
Y24	DDR_DM1	DDR_DM1	DDR_DM1	DDR_DM1	DDR4 SDRAM (IC7)	—	—
T25	DDR_DQ0	DDR_DQ0	DDR_DQ0	DDR_DQ0	DDR4 SDRAM (IC7)	—	—
W24	DDR_DQ1	DDR_DQ1	DDR_DQ1	DDR_DQ1	DDR4 SDRAM (IC7)	—	—
W23	DDR_DQ10	DDR_DQ10	DDR_DQ10	DDR_DQ10	DDR4 SDRAM (IC7)	—	—
AD25	DDR_DQ11	DDR_DQ11	DDR_DQ11	DDR_DQ11	DDR4 SDRAM (IC7)	—	—
AD23	DDR_DQ12	DDR_DQ12	DDR_DQ12	DDR_DQ12	DDR4 SDRAM (IC7)	—	—
AA23	DDR_DQ13	DDR_DQ13	DDR_DQ13	DDR_DQ13	DDR4 SDRAM (IC7)	—	—
AC24	DDR_DQ14	DDR_DQ14	DDR_DQ14	DDR_DQ14	DDR4 SDRAM (IC7)	—	—
AE24	DDR_DQ15	DDR_DQ15	DDR_DQ15	DDR_DQ15	DDR4 SDRAM (IC7)	—	—
R24	DDR_DQ2	DDR_DQ2	DDR_DQ2	DDR_DQ2	DDR4 SDRAM (IC7)	—	—
Y25	DDR_DQ3	DDR_DQ3	DDR_DQ3	DDR_DQ3	DDR4 SDRAM (IC7)	—	—
T24	DDR_DQ4	DDR_DQ4	DDR_DQ4	DDR_DQ4	DDR4 SDRAM (IC7)	—	—
U25	DDR_DQ5	DDR_DQ5	DDR_DQ5	DDR_DQ5	DDR4 SDRAM (IC7)	—	—
R25	DDR_DQ6	DDR_DQ6	DDR_DQ6	DDR_DQ6	DDR4 SDRAM (IC7)	—	—
T23	DDR_DQ7	DDR_DQ7	DDR_DQ7	DDR_DQ7	DDR4 SDRAM (IC7)	—	—
AD24	DDR_DQ8	DDR_DQ8	DDR_DQ8	DDR_DQ8	DDR4 SDRAM (IC7)	—	—
AA24	DDR_DQ9	DDR_DQ9	DDR_DQ9	DDR_DQ9	DDR4 SDRAM (IC7)	—	—

Table 2.2 List of Pin Function Selection Used on Each Module Board (4/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
V24	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR_DQS0_N	DDR4 SDRAM (IC7)	—	—
V25	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR_DQS0_P	DDR4 SDRAM (IC7)	—	—
AB25	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR_DQS1_N	DDR4 SDRAM (IC7)	—	—
AB24	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR_DQS1_P	DDR4 SDRAM (IC7)	—	—
M24	DDR_ODT0	DDR_ODT0	DDR_ODT0	DDR_ODT0	DDR4 SDRAM (IC7)	—	—
L25	DDR_ODT1	DDR_ODT1	DDR_ODT1	DDR_ODT1	DDR4 SDRAM (IC7)	—	—
H24	DDR_RAS#	DDR_RAS#	DDR_RAS#	DDR_RAS#	DDR4 SDRAM (IC7)	—	—
B23	DDR_RESET#	DDR_RESET#	DDR_RESET#	DDR_RESET#	DDR4 SDRAM (IC7)	—	—
H20	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (IC7)	—	—
K20	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (IC7)	—	—
M20	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (IC7)	—	—
R20	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (IC7)	—	—
U20	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (IC7)	—	—
W20	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (IC7)	—	—
G25	DDR_WE#	DDR_WE#	DDR_WE#	DDR_WE#	DDR4 SDRAM (IC7)	—	—
Y19	DEBUGEN	DEBUGEN	DEBUGEN	DEBUGEN	DIP_SW (SW1)	—	—
P3	PVDD182533_0	PVDD182533_0	PVDD182533_0	PVDD182533_0	Input controlling PVDD182533_0 power level with SW1-3 High: 3.3V, Low: 1.8V	—	—
Y17	PVDD182533_1	PVDD182533_1	PVDD182533_1	PVDD182533_1	1.8V	—	—
Y3	EXCLK	EXCLK	EXCLK	EXCLK	24MHz input, connected to clock generator (IC31) for system clock	—	—
P6	VDD18	VDD18	VDD18	VDD18	1.8V	—	—
G6	MD_BOOT0	MD_BOOT0	MD_BOOT0	MD_BOOT0	Input BOOT_SEL0#, BOOT_SEL1# and BOOT_SEL2# logic states	—	—
C5	MD_BOOT1	MD_BOOT1	MD_BOOT1	MD_BOOT1	Input BOOT_SEL0#, BOOT_SEL1# and BOOT_SEL2# logic states	—	—
C4	MD_BOOT2	MD_BOOT2	MD_BOOT2	MD_BOOT2	Input BOOT_SEL0#, BOOT_SEL1# and BOOT_SEL2# logic states	—	—
F20	MD_CLKS	MD_CLKS	MD_CLKS	MD_CLKS	Initial setting: 1 (Pull Up), should be controllable by resistor.	—	—
A22	MD_OSCDRV0	MD_OSCDRV0	MD_OSCDRV0	MD_OSCDRV0	Initial setting: 0 (Pull Down), should be controllable by resistor.	—	—
C21	MD_OSCDRV1	MD_OSCDRV1	MD_OSCDRV1	MD_OSCDRV1	Initial setting: 0 (Pull Down), should be controllable by resistor.	—	—
AA2	NMI	NMI	NMI	NMI	Unused	—	—
B2	OM_CS1#	NC	OM_CS1#	P24_0	OctaRAM (IC3) *Note*: Unused in case of RZ/G2UL	—	—
A4	OM_DQS	NC	OM_DQS	P24_1	OctaFlash (IC2) and OctaRAM (IC3) *Note*: Unused in case of RZ/G2UL	—	—
B4	OM_SIO4	NC	OM_SIO4	P24_2	OctaFlash (IC2) and OctaRAM (IC3) *Note*: Unused in case of RZ/G2UL	—	—

Table 2.2 List of Pin Function Selection Used on Each Module Board (5/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
A3	OM_SIO5	NC	OM_SIO5	P24_3	OctaFlash (IC2) and OctaRAM (IC3) *Note*: Unused in case of RZ/G2UL	—	—
B3	OM_SIO6	NC	OM_SIO6	P24_4	OctaFlash (IC2) and OctaRAM (IC3) *Note*: Unused in case of RZ/G2UL	—	—
A2	OM_SIO7	NC	OM_SIO7	P24_5	OctaFlash (IC2) and OctaRAM (IC3) *Note*: Unused in case of RZ/G2UL	—	—
F14	OTP_VDD18	OTP_VDD18	OTP_VDD18	NC	1.8V *Note*: Unused in case of RZ/Five	—	—
B1	P0_0/SD0_CD/ RIIC3_SDA/ MTIOC2A/ SCI0_TXD	P0_0/SD0_CD	P0_0/SD0_CD	P0_0/SD0_CD	Card Detection High: No card, Low: Card insertd Connected to microSD card slot (CN3) for SD0 *Note*: Only available when SW_SD0_DEV _SEL(SW1-2) is disabled else this is used for GPIO0	P108	GPIO0
C2	P0_1/SD0_WP/ RIIC3_SCL/ MTIOC2B/ SCI0_RXD	P0_1	P0_1	P0_1	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1), used as CAM1_RST#	P111	GPIO3
D3	P0_2/SD1_CD/ MTIOC1A/ RIIC2_SDA/IRQ0	SD1_CD	SD1_CD	SD1_CD	Card Detection High: No card, Low: Card inserted Carrier Board Connector, connected to microSD card slot (CN10) for SD1	P35	SDIO_ CD#
C3	P0_3/SD1_WP/ MTIOC1B/ RIIC2_SCL/IRQ1	P0_3	P0_3	P0_3	Enables power to the uSD Card Carrier Board Connector, connected to microSD card slot (CN10) for SD1 Driven from the Reset signal due to limited SoC IO	P37	SDIO_ PWR_EN
P1	P4_5/ ET0_LINKSTA/ MTIOC3D	P4_5/ ET0_LINKSTA	P4_5/ ET0_LINKSTA	P4_5/ ET0_LINKSTA	Ethernet PHY_0 (IC22) Carrier Board Connector, connected to PMOD1 connector (J2)	P119	GPIO11
T3	P4_3/ET0_MDC/ RSPI1_SSL/ MTIOC8D/ MTIOC3B	RSPI1_SSL/ ET0_MDC	RSPI1_SSL/ ET0_MDC	RSPI1_SSL/ ET0_MDC	Ethernet PHY_0 (IC22) Carrier Board Connector, connected to PMOD0 connector (J1)	P54	SPI_CS0#
T2	P4_4/ET0_MDIO/ MTIOC3C	P4_4/ET0_MDIO	P4_4/ET0_MDIO	P4_4/ET0_MDIO	Ethernet PHY_0 (IC22) Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1), used as CAM1_PWR#	P109	GPIO1
N1	P3_1/ ET0_RX_CTL/ RX_DV/ SSI1_RCK/ POE4#/MTIOC0B	SSI1_RCK/ ET0_RX_CTL/ RX_DV	SSI1_RCK/ ET0_RX_CTL/ RX_DV	SSI1_RCK/ ET0_RX_CTL/ RX_DV	Ethernet PHY_0 (IC22) Carrier Board Connector, connected to PMOD0 connector (J1)	S39	I2S0_LRCK

Table 2.2 List of Pin Function Selection Used on Each Module Board (6/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
N2	P4_2/ ET0_RX_ERR/ RSPI1_MISO/ MTIOC8C/ MTIOC3A	RSPI1_MISO	RSPI1_MISO	RSPI1_MISO	Carrier Board Connector, connected to PMOD0 connector (J1)	P57	SPI1_DIN
AD20	P10_0/ ET1_RXD3/ SSI0_BCK/IRQ4/ MTIOC6A/IRQ2	ET1_RXD3	ET1_RXD3	ET1_RXD3	Ethernet PHY_1 (IC23)	—	—
AD18	P10_1/ ET1_RX_ERR/ SSI0_RCK/ SSI3_BCK/ MTIOC6B	ET1_ERR	ET1_ERR	ET1_ERR	Unused	—	—
AC20	P10_2/ ET1_MDC/ SSI0_TXD/ SSI3_RCK/ MTIOC6C	ET1_MDC	ET1_MDC	ET1_MDC	Ethernet PHY_1 (IC23)	—	—
AE21	P10_3/ ET1_MDIO/ SSI0_RXD/ SSI3_TXD/ USB1_VBUSEN/ MTIOC6D	ET1_MDIO	ET1_MDIO	ET1_MDIO	Ethernet PHY_1 (IC23)	—	—
AC19	P10_4/ ET1_LINKSTA/ ADC_TRG/ SSI3_RXD/ USB1_OVRCUR	ET1_LINKSTA	ET1_LINKSTA	ET1_LINKSTA	Ethernet PHY_1 (IC23)	—	—
A10	P11_3/SSI0_RXD /POE10#/ SCI1_CTS#/ RTS#/ RSPI2_SSL/ DISP_CLK	DISP_CLK	DISP_CLK	P11_3	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	A10
B10	P11_2/SSI0_TXD /POE8#/ SCI1_SCK/ RSPI2_MISO/ DISP_DATA0/ SCIF1_TXD	DISP_DATA0	DISP_DATA0	P11_2	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	B10
A11	P13_1/ SCIF0_RXD/ CAN0_TX/ MTIOC4B/ USB1_OVRCUR/ DISP_DATA1/ SCIF1_RXD	DISP_DATA1	DISP_DATA1	P13_1	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	A11
A14	P16_0/ SCIF1_CTS#/ CAN1_RX_DATA RATE_EN/ SCI0_CTS#/ RTS#/ DISP_DATA10	DISP_DATA10	DISP_DATA10	P16_0	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	A14

Table 2.2 List of Pin Function Selection Used on Each Module Board (7/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
C14	P15_0/RSPI0_CK /IRQ4/MTIOC8A/ DISP_DATA11	DISP_DATA11	DISP_DATA11	P15_0	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	C14
B14	P16_1/ SCIF1_RTS#/ DISP_DATA12	DISP_DATA12	DISP_DATA12	P16_1	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
C15	P15_1/ RSPI0_MOSI/ IRQ5/MTIOC8B/ DISP_DATA13	DISP_DATA13	DISP_DATA13	P15_1	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
A15	P15_3/ RSPI0_SSL/ IRQ7/MTIOC8D/ DISP_DATA14	DISP_DATA14	DISP_DATA14	P15_3	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
F16	P18_0/IRQ2/ ADC_TRG/ SCI0_SCK/ DISP_DATA15/ SCIF3_SCK	DISP_DATA15	DISP_DATA15	P18_0	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
B15	P15_2/ RSPI0_MISO/ IRQ6/MTIOC8C/ DISP_DATA16/ SCI1_TXD	DISP_DATA16	DISP_DATA16	P15_2	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
C16	P17_0/ RRRSPI2_CK/ SSI1_BCK/ CAN1_TX/ MTIOC3A/ DISP_DATA17/ SCI1_RXD	DISP_DATA17	DISP_DATA17	P17_0	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
A16	P17_2/ RSPI1_MISO/ SSI1_TXD/ CAN1_TX_ DATARATE_EN/ MTIOC3C/ DISP_DATA18	DISP_DATA18	DISP_DATA18	P17_2	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
B16	P17_1/ RSPI1_MOSI/ SSI1_RCK/ CAN1_RX/ MTIOC3B/ DISP_DATA19	DISP_DATA19	DISP_DATA19	P17_1	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
B11	P13_0/ SCIF0_TXD/ CAN_CLK/ MTIOC4A/ USB1_VBUSEN/ DISP_DATA2	DISP_DATA2	DISP_DATA2	P13_0	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
A17	P18_1/IRQ3/ SCIF3_SCK/ SCI0_TXD/ DISP_DATA20/ SCIF3_RXD	DISP_DATA20	DISP_DATA20	P18_1	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—

Table 2.2 List of Pin Function Selection Used on Each Module Board (8/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
B17	P18_2/IRQ4/ RSPI0_CK/ SCI0_SCK/ SCIF3_RXD/ SCI0_RXD/ DISP_DATA21/ SCIF3_TXD	DISP_DATA21	DISP_DATA21	P18_2	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
C17	P17_3/ RSPI1_SSL/ SSI1_RXD/ CAN1_RX_ DATARATE_EN/ MTIOC3D/ DISP_DATA22	DISP_DATA22	DISP_DATA22	P17_3	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
C20	P18_3/IRQ5/ RSPI0_MOSI/ SCI0_TXD/ SCIF3_TXD/ SCI0_CTS#/ RTS#/ DISP_DATA23/ SCIF4_SCK	DISP_DATA23	DISP_DATA23	P18_3	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
A12	P13_4/ SCIF0_RTS#/ CAN0_RX_ DATARATE_EN/ DISP_DATA3	DISP_DATA3	DISP_DATA3	P13_4	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
B12	P13_3/ SCIF0_CTS#/ CAN0_TX_ DATARATE_EN/ MTIOC4D/ DISP_DATA4	DISP_DATA4	DISP_DATA4	P13_3	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
C17	P17_3/ RSPI1_SSL/ SSI1_RXD/ CAN1_RX_ DATARATE_EN/ MTIOC3D/ DISP_DATA22	DISP_DATA22	DISP_DATA22	P17_3	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
C20	P18_3/IRQ5/ RSPI0_MOSI/ SCI0_TXD/ SCIF3_TXD/ SCI0_CTS#/ RTS#/ DISP_DATA23/ SCIF4_SCK	DISP_DATA23	DISP_DATA23	P18_3	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
A12	P13_4/ SCIF0_RTS#/ CAN0_RX_ DATARATE_EN/ DISP_DATA3	DISP_DATA3	DISP_DATA3	P13_4	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
B12	P13_3/ SCIF0_CTS#/ CAN0_TX_ DATARATE_EN/ MTIOC4D/ DISP_DATA4	DISP_DATA4	DISP_DATA4	P13_3	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—

Table 2.2 List of Pin Function Selection Used on Each Module Board (9/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
C11	P12_1/IRQ1/ SCI0_TXD/ MTIOC0B/ SCIF3_RXD/ DISP_DATA5	DISP_DATA5	DISP_DATA5	P12_1	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
C12	P13_2/ SCIF0_SCK/ CAN0_RX/ MTIOC4C/ DISP_DATA6	DISP_DATA6	DISP_DATA6	P13_2	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
C13	P14_0/ SCIF1_TXD/ CAN1_TX/ MTIC5U/ SCI0_RXD/ DISP_DATA7	DISP_DATA7	DISP_DATA7	P14_0	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
A13	P14_2/ SCIF1_SCK/ ADC_TRG/ CAN1_TX_ DATARATE_EN/ MTIC5W/ SCI0_SCK/ DISP_DATA8/ IRQ3	DISP_DATA8	DISP_DATA8	P14_2	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
B13	P14_1/ SCIF1_RXD/ CAN1_RX/ MTIC5V/ SCI0_TXD/ DISP_DATA9/ IRQ2	DISP_DATA9	DISP_DATA9	P14_1	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
C9	P11_1/ SSI0_RCK/ POE4#/ SCI1_TXD/ RSPI2_MOSI/ DISP_DE	DISP_DE	DISP_DE	P11_1	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
B9	P11_0/SSI0_BCK /POE0#/ SCI1_RXD/ RSPI2_CK/ DISP_HSYNC	DISP_HSYNC	DISP_HSYNC	P11_0	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
C10	P12_0/IRQ0/ SCI0_RXD/ MTIOC0A/ SCIF3_TXD/ DISP_VSYNC	DISP_VSYNC	DISP_VSYNC	P12_0	Connected to 45pin FFC/FPC connector (CN5) *Note*: Unused in case of RZ/Five	—	—
B22	P18_4/IRQ6/ RSPI0_MISO/ SCI0_RXD/ USB1_VBUSEN/ ADC_TRG/ SCI1_TXD/ SCIF4_RXD	IRQ6	IRQ6	IRQ6	Carrier Board Connector, connected to PMOD0 connector (J1)	P114	GPIO4

Table 2.2 List of Pin Function Selection Used on Each Module Board (10/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
A21	P18_5/IRQ7/ RSPI0_SSL/ SCI0_CTS#/ RTS#/ USB1_OVRCUR/ SCI1_RXD/ SCIF4_TXD	IRQ7	IRQ7	IRQ7	Ethernet PHY_1 (KSZ9131RNXC), used as an intrupt signal	—	—
N3	P3_0/ET0_RXC/ RX_CLK/ SSI1_BCK/ POE0#/MTIOC0A	ET0_RXC/ RX_CLK/ SSI1_BCK	ET0_RXC/ RX_CLK/ SSI1_BCK	ET0_RXC/ RX_CLK/ SSI1_BCK	Ethernet PHY_0 (KSZ9131RNXC) Carrier Board Connector, connected to Audio Codec (IC2)	S42	I2S0_CK
P2	P3_2/ET0_RXD0/ SSI1_TXD/ POE8#/MTIOC0C	ET0_RXD0/ SSI1_TXD	ET0_RXD0/ SSI1_TXD	ET0_RXD0/ SSI1_TXD	Ethernet PHY_0 (KSZ9131RNXC) Carrier Board Connector, connected to Audio Codec (IC2)	S40	I2S0_ SDOUT
R3	P3_3/ET0_RXD1/ SSI1_RXD/ POE10#/ MTIOC0D	ET0_RXD1/ SSI1_RXD	ET0_RXD1/ SSI1_RXD	ET0_RXD1/ SSI1_RXD	Ethernet PHY_0 (KSZ9131RNXC) Carrier Board Connector, connected to Audio Codec (IC2)	S41	I2S0_SDIN
R2	P4_0/ET0_RXD2/ RRRSPI2_CK/ MTIOC8A/ MTIOC2A/ USB1_VBUSEN	ET0_RXD2/ RSPI1_CK	ET0_RXD2/ RSPI1_CK	ET0_RXD2/ RSPI1_CK	Ethernet PHY_0 (KSZ9131RNXC) Carrier Board Connector, connected to PMOD0 connector (J1)	P56	SPI1_CK
R1	P4_1/ET0_RXD3/ RSPI1_MOSI/ MTIOC8B/ MTIOC2B/ USB1_OVRCUR	ET0_RXD3/ RSPI1_MOSI	ET0_RXD3/ RSPI1_MOSI	ET0_RXD3/ RSPI1_MOSI	Ethernet PHY_0 (KSZ9131RNXC) Carrier Board Connector, connected to PMOD0 connector (J1)	P58	SPI1_DO
M3	P2_2/ET0_TX_ COL/SSI0_TXD/ CAN1_TX_ DATARATE_EN/ MTCLKC/ SCI0_TXD/ RSPI0_MOSI	ET0_TX_COL	ET0_TX_COL	ET0_TX_COL	Unused	—	—
M6	P2_3/ET0_TX_ CRS/SSI0_RXD/ CAN1_RX_ DATARATE_EN/ MTCLKD/ SCI0_RXD/ RSPI0_MISO	ET0_TX_CRS	ET0_TX_CRS	ET0_TX_CRS	Unused	—	—
M1	P1_1/ ET0_TX_CTL/ TX_EN/ RSPI0_MOSI/ CAN0_TX/ MTIOC1B	ET0_TX_CTL/ TX_EN/CAN0_ TX	ET0_TX_CTL/ TX_EN/CAN0_ TX	ET0_TX_CTL/ TX_EN/CAN0_ TX	Ethernet PHY_0 (KSZ9131RNXC) Carrier Board Connector, connected to CAN0 connector (CN15)	P143	CAN0_TX
K6	P2_1/ ET0_TX_ERR/ SSI0_RCK/ CAN1_RX/ MTCLKB/ SCI0_CLK/ RSPI0_CK	CAN1_RX	CAN1_RX	CAN1_RX	Carrier Board Connector, connected to CAN1 connector (CN16)	P146	CAN1_RX
M2	P1_0/ET0_TXC/ TX_CLK/ RSPI0_CK/ CAN_CLK/ MTIOC1A	ET0_TXC_TX_ CLK/P1_0	ET0_TXC_TX_ CLK/P1_0	ET0_TXC_TX_ CLK/P1_0	Ethernet PHY_0 (KSZ9131RNXC)	P113	GPIO5

Table 2.2 List of Pin Function Selection Used on Each Module Board (11/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
L1	P1_2/ET0_TXD0/ RSPI0_MISO/ CAN0_RX/ MTIC5U	ET0_TXD0/ CAN0_RX	ET0_TXD0/ CAN0_RX	ET0_TXD0/ CAN0_RX	Ethernet PHY_0 (KSZ9131RNXC) Carrier Board Connector, connected to CAN0 connector (CN15)	P144	CAN0_RX
L2	P1_3/ET0_TXD1/ RSPI0_SSL/ CAN0_TX_ DATARATE_EN/ MTIC5V	ET0_TXD1/P1_3	ET0_TXD1/P1_3	ET0_TXD1/P1_3	Ethernet PHY_0 (KSZ9131RNXC) Carrier Board Connector, connected to PMOD0 connector (J1)	P114	GPIO6
K1	P1_4/ET0_TXD2/ CAN0_RX_ DATARATE_EN/ MTIC5W	ET0_TXD2/P1_4	ET0_TXD2/P1_4	ET0_TXD2/P1_4	Ethernet PHY_0 (KSZ9131RNXC) Carrier Board Connector,connected to PMOD0 connector (J1)	P115	GPIO7
K2	P2_0/ET0_TXD3/ SSI0_BCK/ CAN1_TX/ MTCLKA	ET0_TXD3/ CAN1_TX	ET0_TXD3/ CAN1_TX	ET0_TXD3/ CAN1_TX	Ethernet PHY_0 (KSZ9131RNXC) Carrier Board Connector, connected to CAN1 connector (CN16)	P145	CAN1_TX
AD3	P5_0/ USB0_VBUSEN/ SCIF2_TXD/ MTIOC7A	USB0_VBUSEN	USB0_VBUSEN	USB0_VBUSEN	Enables power to the USB0 port Carrier Board Connector, include gate USB0_VBUSEN state	P62	USB0_EN_ OC#
AC3	P5_1/ SCIF2_RXD/ MTIOC7B/ ADC_TRG/ SCI0_CTS#/ RTS#/ RSPI0_SSL/IRQ2	IRQ2	IRQ2	IRQ2	Ethernet PHY_0 (KSZ9131RNXC), used as an intrupt signal Carrier Board Connector, connected to PMOD1 connector (J2)	P118	GPIO10
AE3	P5_2/ USB0_OVRCUR/ SCIF2_SCK/ MTIOC7C/ SSI2_BCK	USB0_OVRCUR	USB0_OVRCUR	USB0_OVRCUR	Active low input when USB0 is over-current Carrier Board Connector, include gate USB0_OVRCUR state	P62	USB0_EN_ OC#
AD2	P5_3/ USB0_OTG_ID/ SCIF2_CTS#/ MTIOC7D/ SSI2_RCK/ USB1_VBUSEN	USB0_OTG_ID	USB0_OTG_ID	USB0_OTG_ID	OTG identification input Carrier Board Connector, connected to microUSB Type-AB connector (CN11)	P64	USB0_OTG_ ID
AB3	P5_4/ USB0_OTG_ EXICEN/ SCIF2_RTS#/ SSI2_DATA/ USB1_OVRCUR	USB1_OVRCUR	USB1_OVRCUR	USB1_OVRCUR	Active low input when USB1 is over-current Carrier Board Connector, include gate USB1_OVRCUR state	P67	USB1_EN_ OC#
AD1	P6_0/ USB1_VBUSEN/ RSPI2_CK/ CAN_CLK/ SCIF2_TXD/ MTIOC7A	USB1_VBUSEN	USB1_VBUSEN	USB1_VBUSEN	Enables power to the USB1 port Carrier Board Connector, include gate USB1_VBUSEN state	P67	USB1_EN_ OC#
AE2	P6_1/ USB1_OVRCUR/ RSPI2_MOSI/ CAN0_TX/ SCIF2_RXD/ MTIOC7B	SD1_PWR_SEL	SD1_PWR_SEL	SD1_PWR_SEL	Input controlling SD1_PVDD power level High: 3.3V, Low: 1.8V	—	—

Table 2.2 List of Pin Function Selection Used on Each Module Board (12/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AB2	P6_2/ADC_TRG/ RSPI2_MISO/ CAN0_RX/ SCIF2_SCK/ MTIOC7C/IRQ2	SD0_PWR_SEL/ ADC_TRG	SD0_PWR_SEL/ ADC_TRG	SD0_PWR_SEL/ ADC_TRG	Pin connector (CN1) for ADC input or Input controlling SD0_PVDD power level High: 3.3V, Low: 1.8V *Note*: Only available when uSD is being used else this is ADC_TRG input	—	—
AC1	P6_3/RIIC2_SDA/ RSPI2_SSL/ CAN0_TX_ DATARATE_EN/ SCIF2_CTS#/ MTIOC7D/ SCIF0_RXD/ IRQ3	SCIF0_RXD	SCIF0_RXD	SCIF0_RXD	Carrier Board Connector, connected to microUSB Type-AB connector (CN14), used as Serial Download Mode	P141	SER3_RX
AC2	P6_4/RIIC2_SCL/ CAN0_RX_ DATARATE_EN/ SCIF2_RTS#/ ADC_TRG/ SCIF0_TXD/IRQ4	SCIF0_TXD	SCIF0_TXD	SCIF0_TXD	Carrier Board Connector, connected to microUSB Type-AB connector (CN14), used as Serial Download Mode	P140	SER3_TX
AE18	P7_0/ET1_TXC/ TX_CLK/ ADC_TRG/ RSPI2_CK/ CAN_CLK/ MTIOC0A/ SCIF2_TXD/IRQ5	ET1_TXC/ TX_CLK	ET1_TXC/ TX_CLK	ET1_TXC/ TX_CLK	Ethernet PHY_1 (IC23)	—	—
AD17	P7_1/ ET1_TX_CTL/ TX_EN/ SCI1_SCK/ RSPI2_MOSI/ CAN0_TX/ MTIOC0B/ SCIF2_RXD	ET1_TX_CTL/ TX_EN	ET1_TX_CTL/ TX_EN	ET1_TX_CTL/ TX_EN	Ethernet PHY_1 (IC23)	—	—
AD16	P7_2/ET1_TXD0/ SCI1_TXD/ RSPI2_MISO/ CAN0_RX/ MTIOC0C/ SCIF2_SCK	ET1_TXD0	ET1_TXD0	ET1_TXD0	Ethernet PHY_1 (IC23)	—	—
AE16	P7_3/ET1_TXD1/ SCI1_RXD/ RSPI2_SSL/ CAN0_TX_ DATARATE_EN/ MTIOC0D/ SCIF2_CTS#	ET1_TXD1	ET1_TXD1	ET1_TXD1	Ethernet PHY_1 (IC23)	—	—
AD15	P7_4/ET1_TXD2/ SCI1_CTS#/ RTS#/IRQ2/ CAN0_RX_ DATARATE_EN/ SCIF2_RTS#	ET1_TXD2	ET1_TXD2	ET1_TXD2	Ethernet PHY_1 (IC23)	—	—

Table 2.2 List of Pin Function Selection Used on Each Module Board (13/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AE15	P8_0/ET1_TXD3/ SCIF0_SCK/ SCIF1_RXD/ SSI1_BCK/ SCI0_SCK/ MTIOC7A/IRQ1	ET1_TXD3	ET1_TXD3	ET1_TXD3	Ethernet PHY_1 (IC23)	—	—
AE17	P8_1/ ET1_TX_ERR/ SCIF0_RXD/ SCIF1_TXD/ SSI1_RCK/ SCI0_TXD/ MTIOC7B	ET1_TX_ERR	ET1_TX_ERR	ET1_TX_ERR	Unused	—	—
AC16	P8_2/ ET1_TX_COL/ SCIF0_TXD/ SCIF1_CTS#/ SSI1_TXD/ SCI0_RXD/ MTIOC7C	ET1_TX_COL	ET1_TX_COL	ET1_TX_COL	Unused	—	—
AC15	P8_3/ ET1_TX_CRS/ SCIF0_CTS#/ SCIF1_RTS#/ SSI1_RXD/ SCI0_CTS#/ RTS#/MTIOC7D	ET1_TX_CRS	ET1_TX_CRS	ET1_TX_CRS	Unused	—	—
AC17	P8_4/ET1_RXC/ RX_CLK/ SCIF0_RTS#	ET1_RXC/ RX_CLK	ET1_RXC/ RX_CLK	ET1_RXC/ RX_CLK	Ethernet PHY_1 (IC23)	—	—
AC18	P9_0/ ET1_RX_CTL/ RX_DV/ RSPI0_CK/ SSI2_BCK/ MTIOC4A/ SCIF4_SCK	ET1_RX_CTL_ RX_DV	ET1_RX_CTL_ RX_DV	ET1_RX_CTL_ RX_DV	Ethernet PHY_1 (IC23)	—	—
AE19	P9_1/ET1_RXD0/ RSPI0_MOSI/ SSI2_RCK/ MTIOC4B/ SCIF4_RXD	ET1_RXD0	ET1_RXD0	ET1_RXD0	Ethernet PHY_1 (IC23)	—	—
AD19	P9_2/ET1_RXD1/ RSPI0_MISO/ SSI2_DATA/ MTIOC4C/ SCIF4_TXD	ET1_RXD1	ET1_RXD1	ET1_RXD1	Ethernet PHY_1 (IC23)	—	—
AE20	P9_3/ET1_RXD2/ RSPI0_SSL/ IRQ3/MTIOC4D/ IRQ1	ET1_RXD2	ET1_RXD2	ET1_RXD2	Ethernet PHY_1 (IC23)	—	—
L3	PLL1_AVDD18	PLL1_AVDD18	PLL1_AVDD18	PLL1_AVDD18	1.8V	—	—
U3	PLL23_AVDD18	PLL23_AVDD18	PLL23_AVDD18	PLL23_AVDD18	1.8V	—	—
T6	PLL23_DVDD11	PLL23_DVDD11	PLL23_DVDD11	PLL23_DVDD11	1.1V	—	—
N17	PLL4_AVDD18	PLL4_AVDD18	PLL4_AVDD18	PLL4_AVDD18	1.8V	—	—
Y14	PLL5_AVDD18	PLL5_AVDD18	PLL5_AVDD18	PLL5_AVDD18	1.8V	—	—

Table 2.2 List of Pin Function Selection Used on Each Module Board (14/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
Y15	PLL5_DVDD11	PLL5_DVDD11	PLL5_DVDD11	NC	1.1V *Note*: Unused in case of RZ/Five	—	—
F11	PLL6_AVDD18	PLL6_AVDD18	PLL6_AVDD18	PLL6_AVDD18	1.8V	—	—
W2	PRST#	PRST#	PRST#	PRST#	Connected to PMIC, used as NRESET function	—	—
C19	PVDD	PVDD	PVDD	PVDD	3.3V	—	—
F13	PVDD	PVDD	PVDD	PVDD	3.3V	—	—
F19	PVDD	PVDD	PVDD	PVDD	3.3V	—	—
F9	PVDD	PVDD	PVDD	PVDD	3.3V	—	—
W6	PVDD	PVDD	PVDD	PVDD	3.3V	—	—
Y10	PVDD	PVDD	PVDD	PVDD	3.3V	—	—
Y18	PVDD	PVDD	PVDD	PVDD	3.3V	—	—
A7	QSPI_RESET#	QSPI_RESET#	QSPI_RESET#	QSPI_RESET#	Octa Flash (IC2)	—	—
A6	QSPI_WP#	QSPI_WP#	QSPI_WP#	QSPI_WP#	Unused *Note*: In case of RZ/Five, this pin is used as WDTOVF_PERROUT#. Mounted a resistor (R79) for WDTOVF option and connected to a logic IC for using NRESET function of PMIC, but the WDT function is not available at this time.	—	—
C7	QSPI0_IO0	QSPI0_IO0	QSPI0_IO0	QSPI0_IO0	QSPI Flash (IC9) or OctaFlash (IC2) and OctaRAM (IC3)	—	—
A5	QSPI0_IO1	QSPI0_IO1	QSPI0_IO1	QSPI0_IO1	QSPI Flash (IC9) or OctaFlash (IC2) and OctaRAM (IC3)	—	—
B7	QSPI0_IO2	QSPI0_IO2	QSPI0_IO2	QSPI0_IO2	QSPI Flash (IC9) or OctaFlash (IC2) and OctaRAM (IC3)	—	—
C6	QSPI0_IO3	QSPI0_IO3	QSPI0_IO3	QSPI0_IO3	QSPI Flash (IC9) or OctaFlash (IC2) and OctaRAM (IC3)	—	—
B6	QSPI0_SPCLK	QSPI0_SPCLK	QSPI0_SPCLK	QSPI0_SPCLK	QSPI Flash (IC9) or OctaFlash (IC2) and OctaRAM (IC3)	—	—
B5	QSPI0_SSL	QSPI0_SSL	QSPI0_SSL	QSPI0_SSL	QSPI Flash (IC9) or OctaFlash (IC2) and OctaRAM (IC3)	—	—
B19	RIIC0_SCL	RIIC0_SCL	RIIC0_SCL	RIIC0_SCL	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1)	S1	I2C_CAM_CK
B20	RIIC0_SDA	RIIC0_SDA	RIIC0_SDA	RIIC0_SDA	Carrier Board Connector, connected to 24pin FFC/FPC connector for MIPI-CSI (CN1)	S2	I2C_CAM_DAT
A19	RIIC1_SCL	RIIC1_SCL	RIIC1_SCL	RIIC1_SCL	Connected to 45pin FFC/FPC connector Carrier Board Connector, connected to PMOD1 connector (J2) and Audio Codec (IC2)	S48	I2C_GP_CK

Table 2.2 List of Pin Function Selection Used on Each Module Board (15/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
A20	RIIC1_SDA	RIIC1_SDA	RIIC1_SDA	RIIC1_SDA	Connected to 45pin FFC/FPC connector Carrier Board Connector, connected to PMOD1 connector (J2) and Audio Codec (IC2)	S39	I2C_GP_DAT
G1	SD0_CLK	SD0_CLK	SD0_CLK	SD0_CLK	eMMC Memory (IC6) or microSD card slot (CN3)	—	—
E2	SD0_CMD	SD0_CMD	SD0_CMD	SD0_CMD	eMMC Memory (IC6) or microSD card slot (CN3)	—	—
F1	SD0_DATA0	SD0_DATA0	SD0_DATA0	SD0_DATA0	eMMC Memory (IC6) or microSD card slot (CN3)	—	—
H3	SD0_DATA1	SD0_DATA1	SD0_DATA1	SD0_DATA1	eMMC Memory (IC6) or microSD card slot (CN3)	—	—
F2	SD0_DATA2	SD0_DATA2	SD0_DATA2	SD0_DATA2	eMMC Memory (IC6) or microSD card slot (CN3)	—	—
D2	SD0_DATA3	SD0_DATA3	SD0_DATA3	SD0_DATA3	eMMC Memory (IC6) or microSD card slot (CN3)	—	—
E1	SD0_DATA4	SD0_DATA4	SD0_DATA4	SD0_DATA4	eMMC Memory (IC6)	—	—
D1	SD0_DATA5	SD0_DATA5	SD0_DATA5	SD0_DATA5	eMMC Memory (IC6)	—	—
E3	SD0_DATA6	SD0_DATA6	SD0_DATA6	SD0_DATA6	eMMC Memory (IC6)	—	—
F3	SD0_DATA7	SD0_DATA7	SD0_DATA7	SD0_DATA7	eMMC Memory (IC6)	—	—
G3	SD0_PVDD	SD0_PVDD	SD0_PVDD	SD0_PVDD	1.8/3.3V	—	—
C1	SD0_RST#	SD0_RST#	SD0_RST#	SD0_RST#	eMMC Memory (IC6)	—	—
G2	SD1_CLK	SD1_CLK	SD1_CLK	SD1_CLK	Carrier Board Connector, connected to microSD card slot (CN10) for SD1	P36	SD1_CLK
H6	SD1_CMD	SD1_CMD	SD1_CMD	SD1_CMD	Carrier Board Connector, connected to microSD card slot (CN10) for SD1	P34	SD1_CMD
H2	SD1_DATA0	SD1_DATA0	SD1_DATA0	SD1_DATA0	Carrier Board Connector, connected to microSD card slot (CN10) for SD1	P39	SDIO_D0
J3	SD1_DATA1	SD1_DATA1	SD1_DATA1	SD1_DATA1	Carrier Board Connector, connected to microSD card slot (CN10) for SD1	P40	SDIO_D1
J1	SD1_DATA2	SD1_DATA2	SD1_DATA2	SD1_DATA2	Carrier Board Connector, connected to microSD card slot (CN10) for SD1	P41	SDIO_D2
J2	SD1_DATA3	SD1_DATA3	SD1_DATA3	SD1_DATA3	Carrier Board Connector, connected to microSD card slot (CN10) for SD1	P42	SDIO_D3
K3	SD1_PVDD	SD1_PVDD	SD1_PVDD	SD1_PVDD	1.8/3.3V	—	—
C8	SPI_PVDD	SPI_PVDD	SPI_PVDD	SPI_PVDD	1.8V	—	—
U2	TCK/SWDCLK	TCK/SWDCLK	TCK/SWDCLK	TCK/SWDCLK	JTAG Connector (CN2)	—	—
W1	TDI	TDI	TDI	TDI	JTAG Connector (CN2)	—	—
V2	TDO	TDO	TDO	TDO	JTAG Connector (CN2)	—	—
AD22	VSS	VSS	VSS	VSS	GND	—	—
U1	TMS/SWDIO	TMS/SWDIO	TMS/SWDIO	TMS/SWDIO	JTAG Connector (CN2)	—	—
V1	TRST#	TRST#	TRST#	TRST#	JTAG Connector (CN2)	—	—
AC9	USB_VDD18	USB_VDD18	USB_VDD18	USB_VDD18	1.8V	—	—
AC8	USB_RREF	USB_RREF	USB_RREF	USB_RREF	Connected to 1.8kΩ to GND	—	—
AC4	USB_VDD18	USB_VDD18	USB_VDD18	USB_VDD18	1.8V	—	—
AC5	USB_VDD18	USB_VDD18	USB_VDD18	USB_VDD18	1.8V	—	—
Y7	USB_VDD33	USB_VDD33	USB_VDD33	USB_VDD33	3.3V	—	—
Y8	USB_VDD33	USB_VDD33	USB_VDD33	USB_VDD33	3.3V	—	—

Table 2.2 List of Pin Function Selection Used on Each Module Board (16/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AC6	VSS	VSS	VSS	VSS	GND	—	—
AC7	VSS	VSS	VSS	VSS	GND	—	—
AD4	VSS	VSS	VSS	VSS	GND	—	—
AD7	VSS	VSS	VSS	VSS	GND	—	—
AE4	VSS	VSS	VSS	VSS	GND	—	—
AE7	VSS	VSS	VSS	VSS	GND	—	—
Y9	VSS	VSS	VSS	VSS	GND	—	—
AE6	USB0_DM	USB0_DM	USB0_DM	USB0_DM	Carrier Board Connector, connected to microUSB Type-AB connector (CN11)	P61	USB0_DM
AD6	USB0_DP	USB0_DP	USB0_DP	USB0_DP	Carrier Board Connector, connected to microUSB Type-AB connector (CN11)	P60	USB0_DP
AD8	USB0_VBUSIN	USB0_VBUSIN	USB0_VBUSIN	USB0_VBUSIN	Carrier Board Connector, connected to microUSB Type-AB connector (CN11)	P63	USB0_VBUS_DET
AE5	USB1_DM	USB1_DM	USB1_DM	USB1_DM	Carrier Board Connector, connected to USB Type-A connector (CN12)	P66	USB1_DM
AD5	USB1_DP	USB1_DP	USB1_DP	USB1_DP	Carrier Board Connector, connected to USB Type-A connector (CN12)	P65	USB1_DP
K10	VDD	VDD	VDD	VDD	1.1V	—	—
K12	VDD	VDD	VDD	VDD	1.1V	—	—
K14	VDD	VDD	VDD	VDD	1.1V	—	—
K16	VDD	VDD	VDD	VDD	1.1V	—	—
L11	VDD	VDD	VDD	VDD	1.1V	—	—
L13	VDD	VDD	VDD	VDD	1.1V	—	—
L15	VDD	VDD	VDD	VDD	1.1V	—	—
M10	VDD	VDD	VDD	VDD	1.1V	—	—
M12	VDD	VDD	VDD	VDD	1.1V	—	—
M14	VDD	VDD	VDD	VDD	1.1V	—	—
M16	VDD	VDD	VDD	VDD	1.1V	—	—
N11	VDD	VDD	VDD	VDD	1.1V	—	—
N13	VDD	VDD	VDD	VDD	1.1V	—	—
N15	VDD	VDD	VDD	VDD	1.1V	—	—
P10	VDD	VDD	VDD	VDD	1.1V	—	—
P12	VDD	VDD	VDD	VDD	1.1V	—	—
P14	VDD	VDD	VDD	VDD	1.1V	—	—
P16	VDD	VDD	VDD	VDD	1.1V	—	—
R11	VDD	VDD	VDD	VDD	1.1V	—	—
R13	VDD	VDD	VDD	VDD	1.1V	—	—
R15	VDD	VDD	VDD	VDD	1.1V	—	—
T10	VDD	VDD	VDD	VDD	1.1V	—	—
T12	VDD	VDD	VDD	VDD	1.1V	—	—
T14	VDD	VDD	VDD	VDD	1.1V	—	—
T16	VDD	VDD	VDD	VDD	1.1V	—	—
A1	VSS	VSS	VSS	VSS	GND	—	—
A25	VSS	VSS	VSS	VSS	GND	—	—

Table 2.2 List of Pin Function Selection Used on Each Module Board (17/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
A8	VSS	VSS	VSS	VSS	GND	—	—
AA25	VSS	VSS	VSS	VSS	GND	—	—
AA3	VSS	VSS	VSS	VSS	GND	—	—
AB1	VSS	VSS	VSS	VSS	GND	—	—
AB23	VSS	VSS	VSS	VSS	GND	—	—
AC10	VSS	VSS	VSS	VSS	GND	—	—
AC11	VSS	VSS	VSS	VSS	GND	—	—
AC12	VSS	VSS	VSS	VSS	GND	—	—
AC13	VSS	VSS	VSS	VSS	GND	—	—
AC14	VSS	VSS	VSS	VSS	GND	—	—
AC21	VSS	VSS	VSS	VSS	GND	—	—
AC22	VSS	VSS	VSS	VSS	GND	—	—
AC23	VSS	VSS	VSS	VSS	GND	—	—
AC25	VSS	VSS	VSS	VSS	GND	—	—
AD14	VSS	VSS	VSS	VSS	GND	—	—
AE1	VSS	VSS	VSS	VSS	GND	—	—
AE14	VSS	VSS	VSS	VSS	GND	—	—
AE23	VSS	VSS	VSS	VSS	GND	—	—
AE25	VSS	VSS	VSS	VSS	GND	—	—
AE8	VSS	VSS	VSS	VSS	GND	—	—
C18	VSS	VSS	VSS	VSS	GND	—	—
C22	VSS	VSS	VSS	VSS	GND	—	—
C23	VSS	VSS	VSS	VSS	GND	—	—
D24	VSS	VSS	VSS	VSS	GND	—	—
E23	VSS	VSS	VSS	VSS	GND	—	—
F10	VSS	VSS	VSS	VSS	GND	—	—
F12	VSS	VSS	VSS	VSS	GND	—	—
F15	VSS	VSS	VSS	VSS	GND	—	—
F18	VSS	VSS	VSS	VSS	GND	—	—
F24	VSS	VSS	VSS	VSS	GND	—	—
F6	VSS	VSS	VSS	VSS	GND	—	—
F7	VSS	VSS	VSS	VSS	GND	—	—
F8	VSS	VSS	VSS	VSS	GND	—	—
G20	VSS	VSS	VSS	VSS	GND	—	—
G23	VSS	VSS	VSS	VSS	GND	—	—
G24	VSS	VSS	VSS	VSS	GND	—	—
H1	VSS	VSS	VSS	VSS	GND	—	—
J11	VSS	VSS	VSS	VSS	GND	—	—
J13	VSS	VSS	VSS	VSS	GND	—	—
J15	VSS	VSS	VSS	VSS	GND	—	—
J17	VSS	VSS	VSS	VSS	GND	—	—
J20	VSS	VSS	VSS	VSS	GND	—	—
J23	VSS	VSS	VSS	VSS	GND	—	—
J6	VSS	VSS	VSS	VSS	GND	—	—
J9	VSS	VSS	VSS	VSS	GND	—	—

Table 2.2 List of Pin Function Selection Used on Each Module Board (18/18)

Pin Location	Pin Name	RZ/G2UL Pin Function	RZ/A3UL Pin Function	RZ/Five Pin Function	Description	SMARC Pin No.	SMARC Pin Name
K24	VSS	VSS	VSS	VSS	GND	—	—
L17	VSS	VSS	VSS	VSS	GND	—	—
L20	VSS	VSS	VSS	VSS	GND	—	—
L6	VSS	VSS	VSS	VSS	GND	—	—
L9	VSS	VSS	VSS	VSS	GND	—	—
M23	VSS	VSS	VSS	VSS	GND	—	—
N20	VSS	VSS	VSS	VSS	GND	—	—
N25	VSS	VSS	VSS	VSS	GND	—	—
N6	VSS	VSS	VSS	VSS	GND	—	—
N9	VSS	VSS	VSS	VSS	GND	—	—
P20	VSS	VSS	VSS	VSS	GND	—	—
R17	VSS	VSS	VSS	VSS	GND	—	—
R23	VSS	VSS	VSS	VSS	GND	—	—
R6	VSS	VSS	VSS	VSS	GND	—	—
R9	VSS	VSS	VSS	VSS	GND	—	—
T1	VSS	VSS	VSS	VSS	GND	—	—
T20	VSS	VSS	VSS	VSS	GND	—	—
U11	VSS	VSS	VSS	VSS	GND	—	—
U13	VSS	VSS	VSS	VSS	GND	—	—
U15	VSS	VSS	VSS	VSS	GND	—	—
U17	VSS	VSS	VSS	VSS	GND	—	—
U24	VSS	VSS	VSS	VSS	GND	—	—
U6	VSS	VSS	VSS	VSS	GND	—	—
U9	VSS	VSS	VSS	VSS	GND	—	—
V20	VSS	VSS	VSS	VSS	GND	—	—
V23	VSS	VSS	VSS	VSS	GND	—	—
V3	VSS	VSS	VSS	VSS	GND	—	—
V6	VSS	VSS	VSS	VSS	GND	—	—
W25	VSS	VSS	VSS	VSS	GND	—	—
W3	VSS	VSS	VSS	VSS	GND	—	—
Y1	VSS	VSS	VSS	VSS	GND	—	—
Y13	VSS	VSS	VSS	VSS	GND	—	—
Y16	VSS	VSS	VSS	VSS	GND	—	—
Y20	VSS	VSS	VSS	VSS	GND	—	—
Y23	VSS	VSS	VSS	VSS	GND	—	—
Y6	VSS	VSS	VSS	VSS	GND	—	—
B21	WDTOVF_ PERROUT#	WDTOVF_ PERROUT#	WDTOVF_ PERROUT#	NC	Connected to a logic IC for using NRESET function of PMIC *Note*: Unused in case of RZ/Five	—	—
Y2	XIN	XIN	XIN	XIN	GND (or 24MHz X'tal oscillator)	—	—
AA1	XOUT	XOUT	XOUT	XOUT	OPEN (or 24MHz X'tal oscillator)	—	—

2.3 Memory

QSPI flash memory and DDR4 SDRAM are mounted on the RTK9743U11C01000BE as external memories.

Please refer to the following for details.

2.3.1 QSPI Flash Memory

RZ/G2UL SMARC Module Board

RZ/A3UL SMARC Module Board
QSPI Edition

RZ/Five SMARC Module Board

Figure 2.1 shows a block diagram of the Serial Flash Memory Interface.

The QSPI flash memory is controlled by the SPI Multi I/O Bus Controller (SPIBSC) that is with built-in to the RZ/G2UL. This memory supports both single data rate (SDR) and double data rate (DDR) transfers at 66 MHz and 50 MHz clock frequency.

NOTE

The pull-up resistor on the clock line “RZ_QSPI0_SPCLK” is optional.

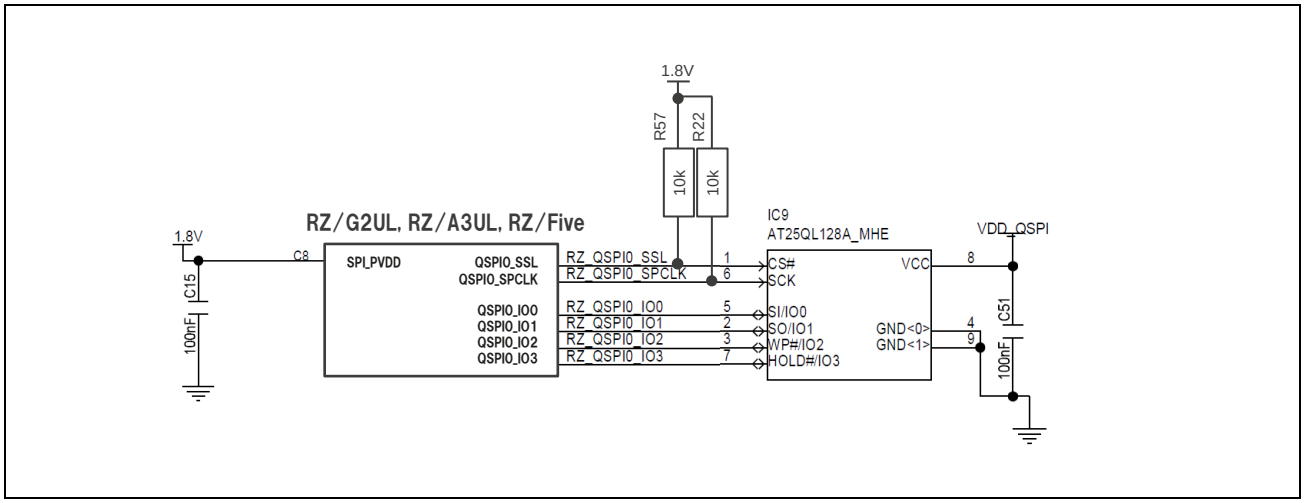


Figure 2.1 Block Diagram of Serial Flash Memory I/F

2.3.2 DDR4 SDRAM

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Edition | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board OCTAL Edition

Figure 2.2 shows a block diagram of the DDR4 SDRAM interface.

The DDR4 SDRAM is controlled by the DDR3L/DDR4 SDRAM Memory Controller (MEMC) that is with built-in to the RZ/G2UL. This interface supports up to DDR4-1600 SDRAM, a data bus width of 16-bit and inline ECC.

This interface complies with JEDEC STANDARD JESD79-4C.

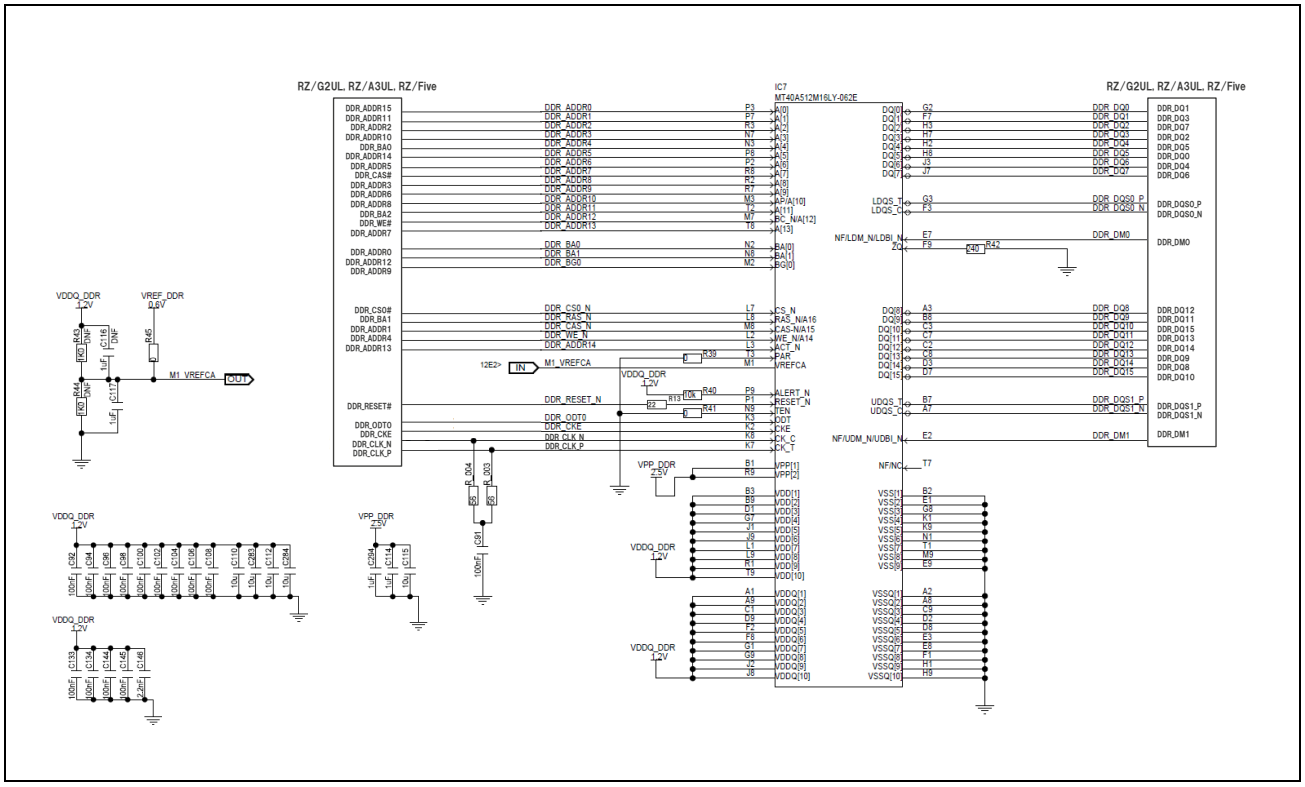


Figure 2.2 Block Diagram of DDR4 SDRAM

2.3.3 Octa Peripheral Interface

RZ/A3UL SMARC Module Board
OCTAL Edition

Figure 2.3 shows a block diagram of the Octa Periphral interface.

The OctaRAM and OctaFlash memory are controlled by the Octa Memory Controller that is with built-in to the RZ/A3UL. These memories support both single data rate (SOPI: Single Octa I/O) and double data rate (DOPI: Double Octa I/O) transfers at 100 MHz clock frequency.

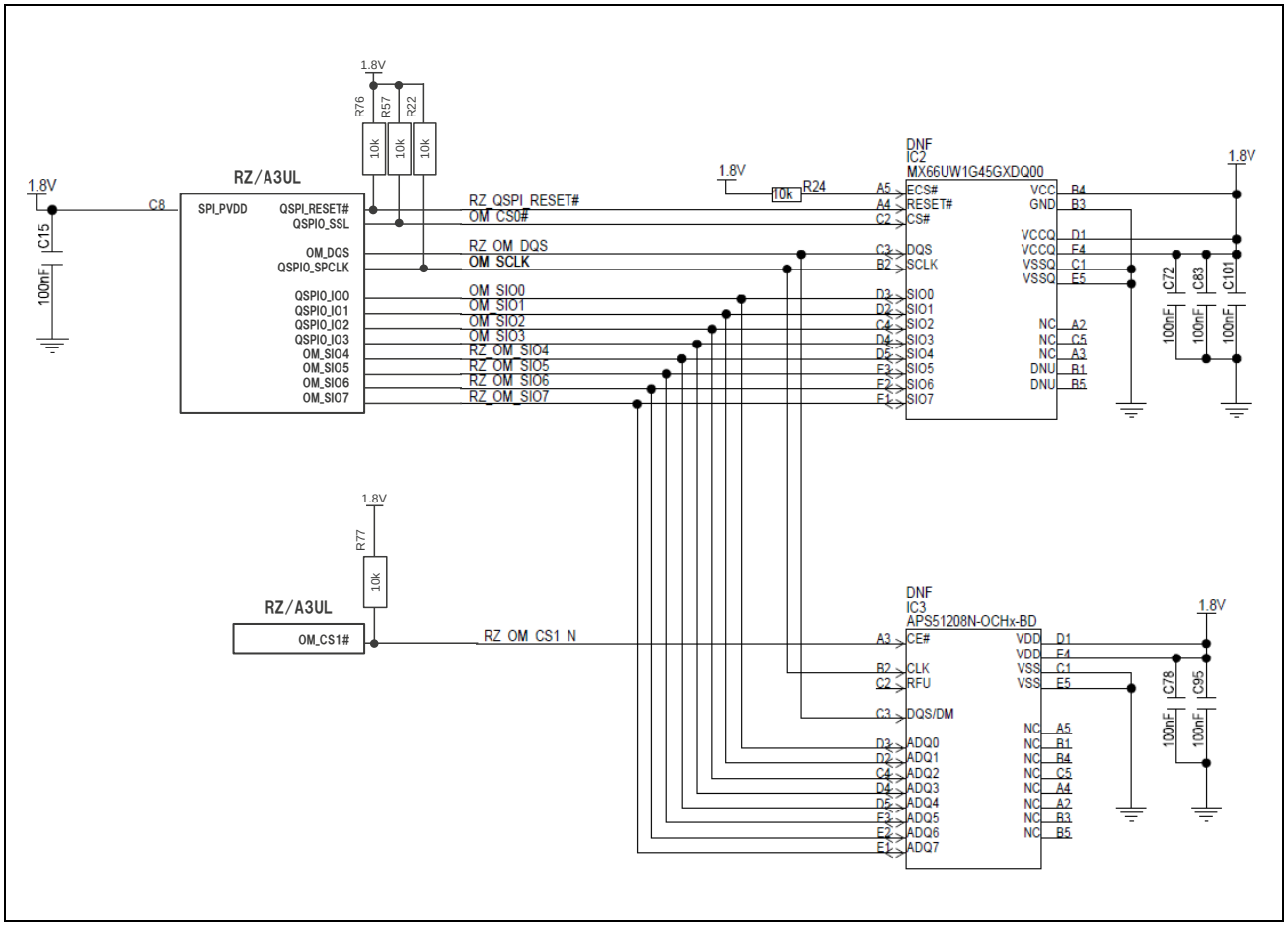


Figure 2.3 Block Diagram of Octa Peripheral I/F

2.4 Gigabit Ethernet Interface

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Edition | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board OCTAL Edition

Figure 2.4 and **Figure 2.5** show a block diagram of Gigabit Ethernet0 and Ethernet1 interface.

The Gigabit Ethernet Interface is controlled by the Ethernet controller (E-MAC) hat conforms to the definition of the MAC (Media Access Control) layer that is with built-in to the RZ/G2UL. The Ethernet clock is sourced from a clock generator connected to the Ethernet PHY.

This interface complies with IEEE802.3 PHY RGMII.

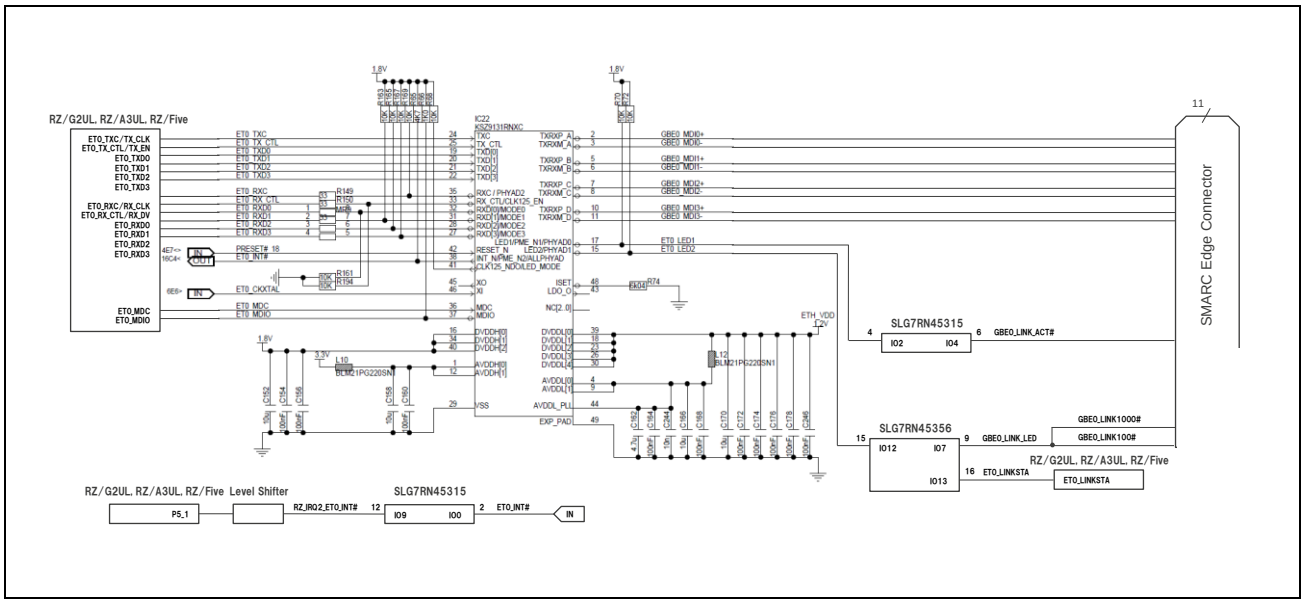


Figure 2.4 Block Diagram of Gigabit Ethernet0 I/F

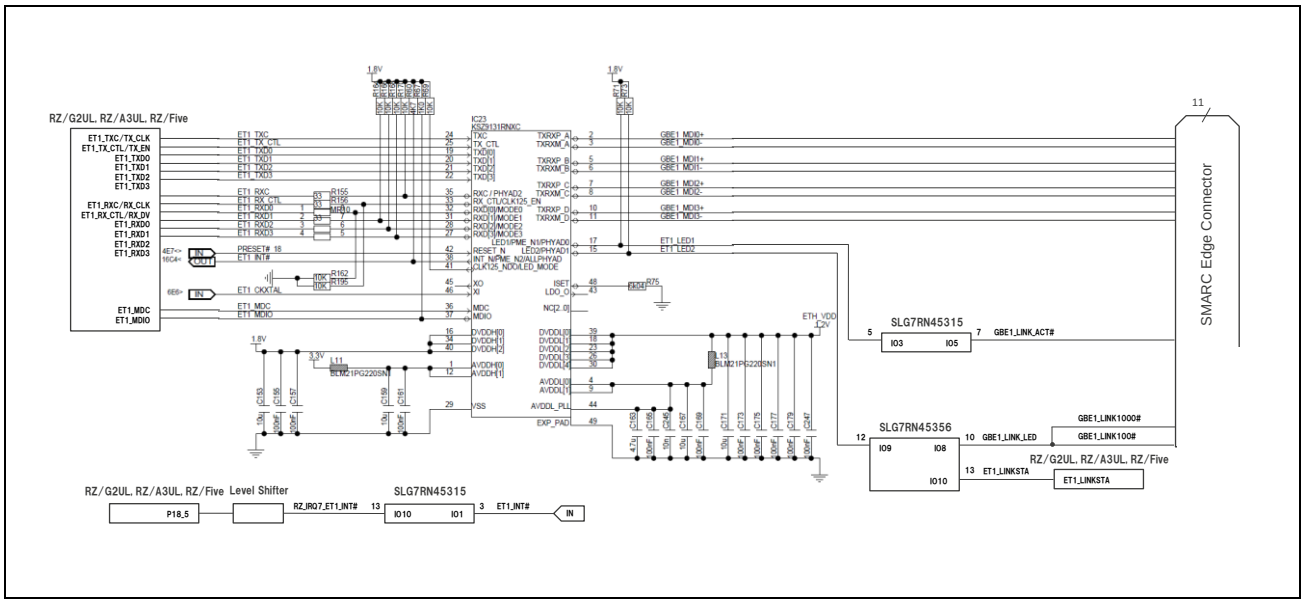


Figure 2.5 Block Diagram of Gigabit Ethernet1 I/F

2.5 ADC Interface

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Edition | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board OCTAL Edition

Figure 2.6 shows a block diagram of the ADC interface.

When the RZ/Five is used, the pin location is different from the RZ/G2UL, so option resistors are required.

The 6-pin connector is implemented on this board and 2ch input channels can be used as the analog signal.

NOTE

ADC_TRG is only available when SD0 is used for eMMC memory (not when microSD card is used).

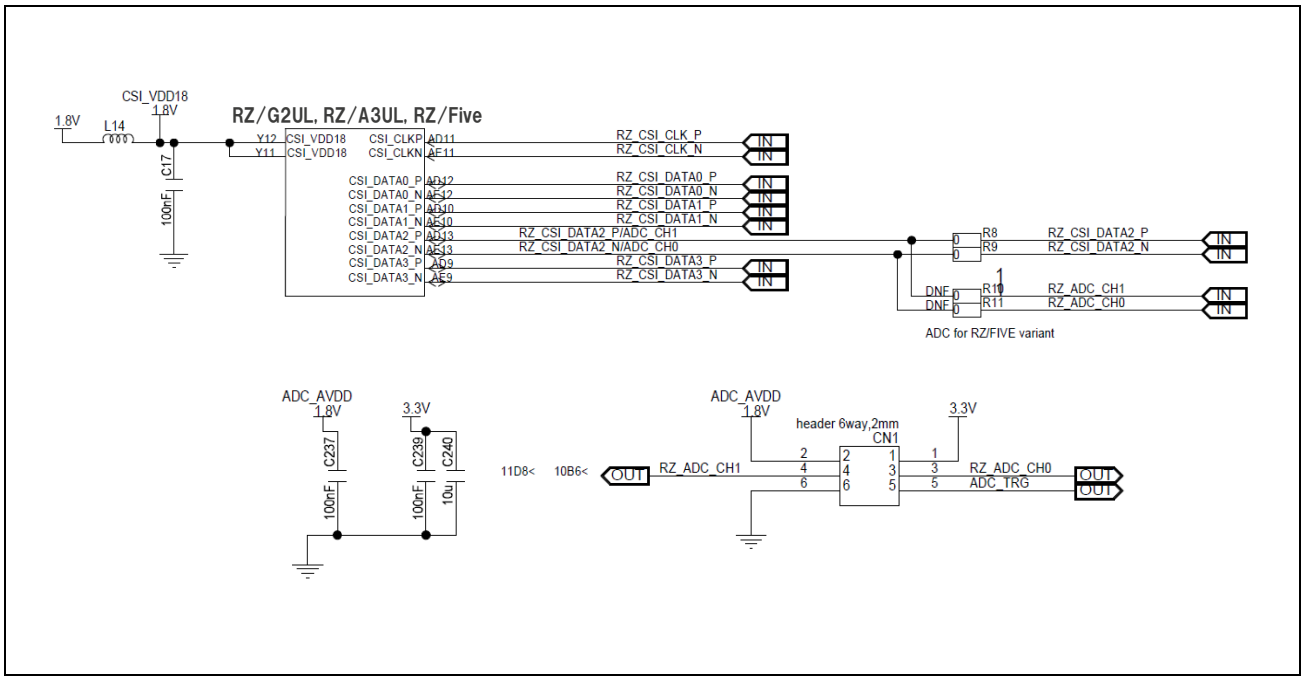


Figure 2.6 Block Diagram of ADC I/F

2.6 Clock Configuration

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Edition | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board OCTAL Edition

Figure 2.7 shows a block diagram of the Clock configuration.

NOTE

SD Interface supports UHS-I mode of 50MB/s (SDR50) and 104MB/s (SDR104).

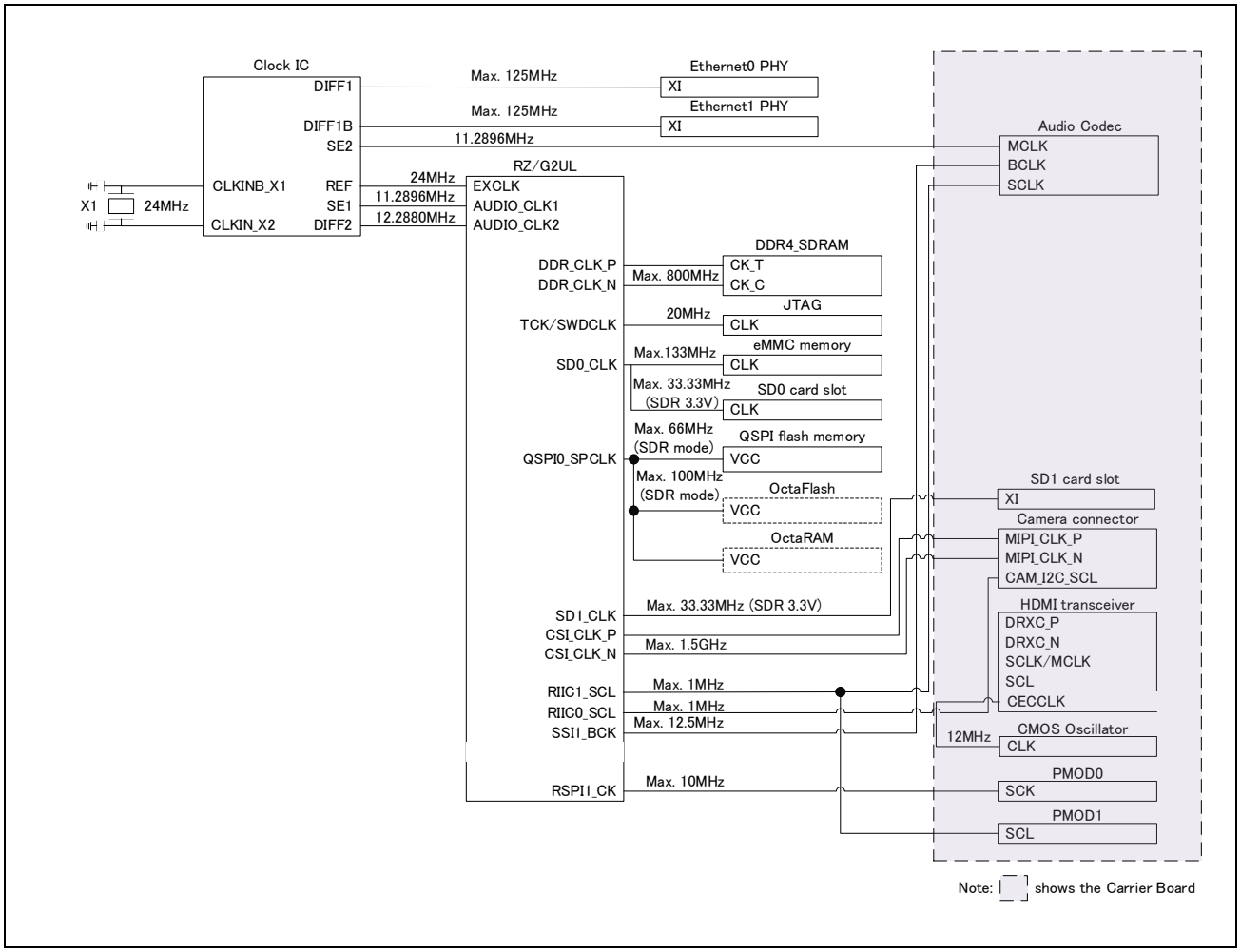


Figure 2.7 Block Diagram of Clock Configuration

2.7 Reset Control

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Edition | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board OCTAL Edition

Figure 2.8 shows block diagrams of a reset control for the RTK9743U11S01000BE (Evaluation board Kit for RZ/G2UL MPU).

For the RTK9743U11C01000BE, the interfaces of DDR4 SDRAM, QSPI flash memory, eMMC memory, Ethernet and Debug are controlled by reset signal from the PMIC.

There are two types of system resets: power-on reset and reset by the button switch.

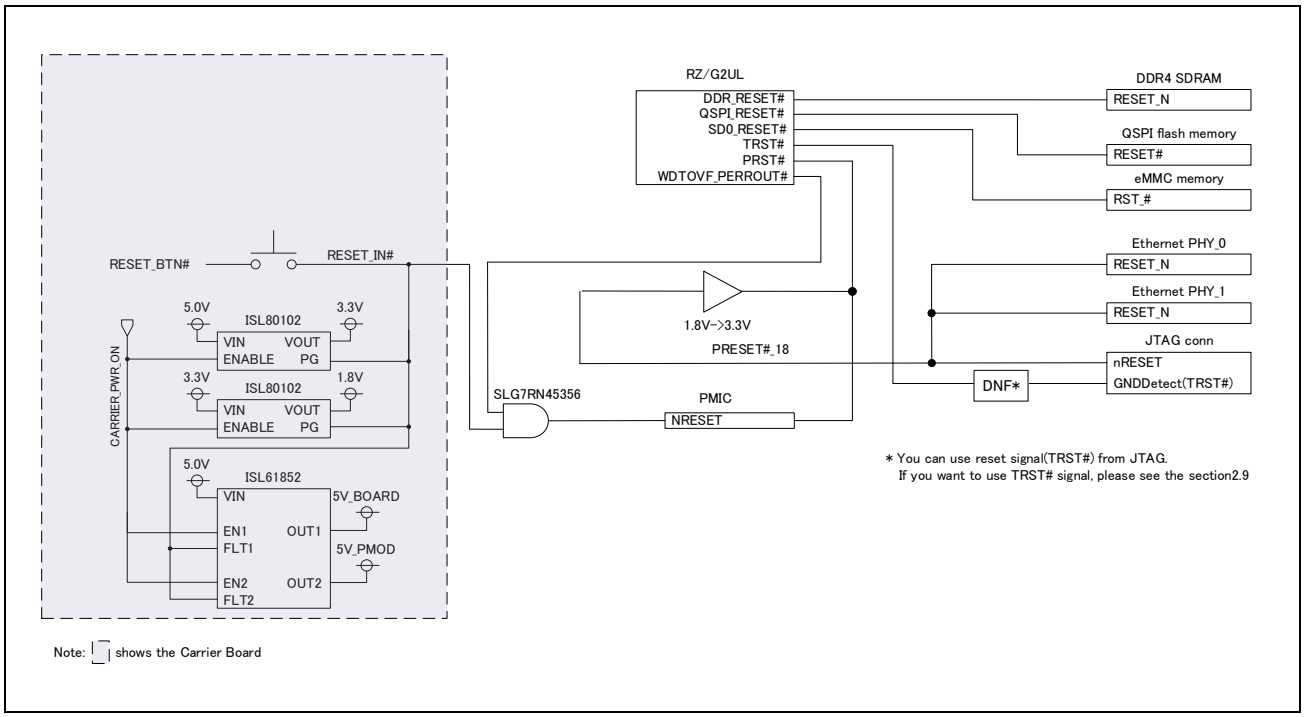


Figure 2.8 Block Diagram of Reset Control

2.8 Power Supply Configuration

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Edition | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board OCTAL Edition

Figure 2.9 shows a block diagram of power configuration for the RTK9743U11S01000BE (Evaluation board Kit for RZ/G2UL MPU).

This board has one USB Type-C receptacle for power input with USB Power Delivery. The input voltage of VBUS can be selected between 5V and 9V.

The default setting for controlling the input voltage level is 5V (max 3A input) with SW11-4 is turned on. When the switch is turned off, the input voltage is 9V (max 3A input). Only when the RTK9743U11S01000BE is connected to external devices that requires a lot of power and is expected to run out of power, the SW 11-4 is turned off.

The 5V power supply is supplied to the PMIC installed on the RTK9743U11C01000BE, and the PMIC generates the power supply voltage for each interface.

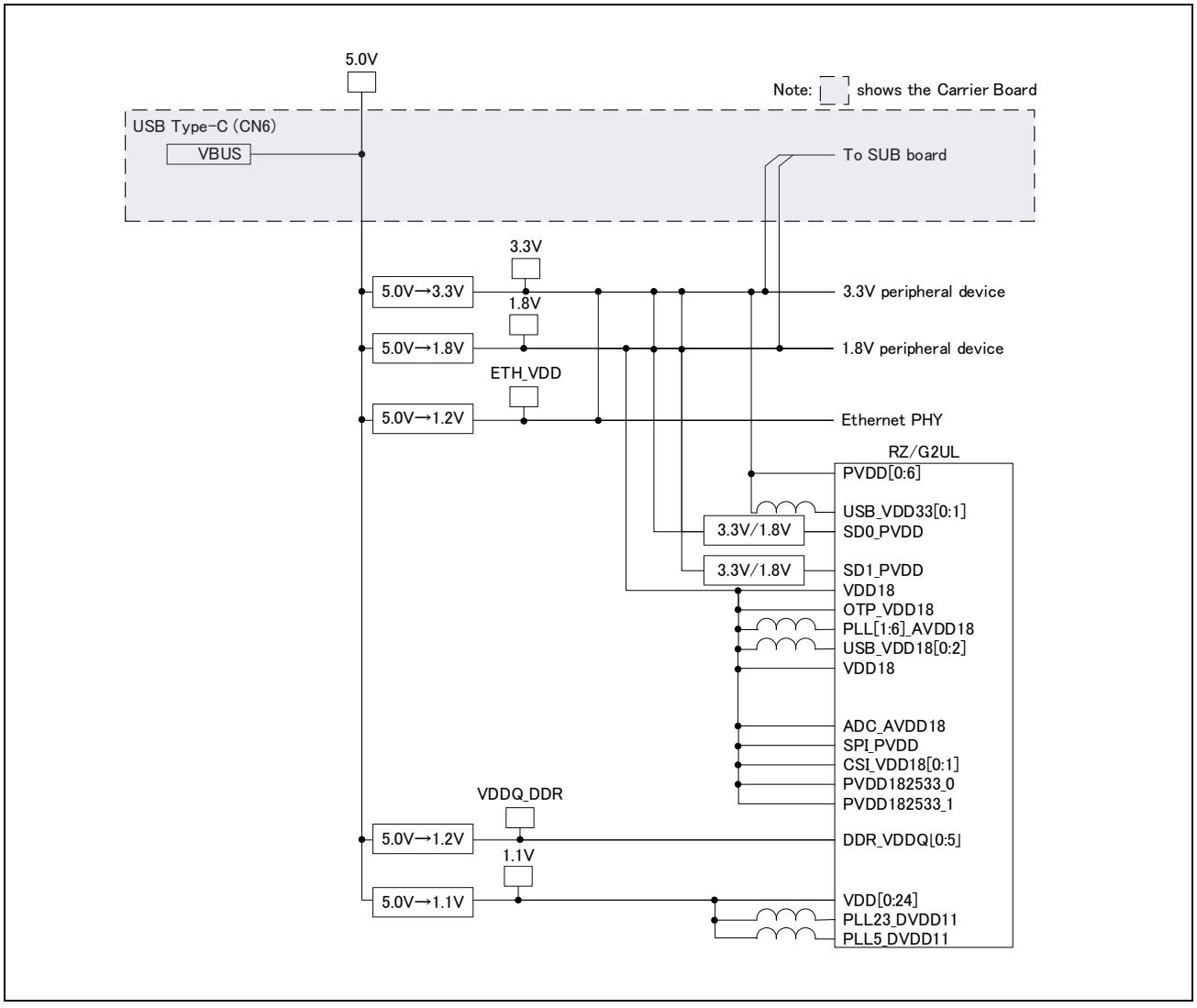


Figure 2.9 Block Diagram of Power Configuration

Figure 2.10 shows block diagrams of power regulation for RTK9743U11C01000BE.

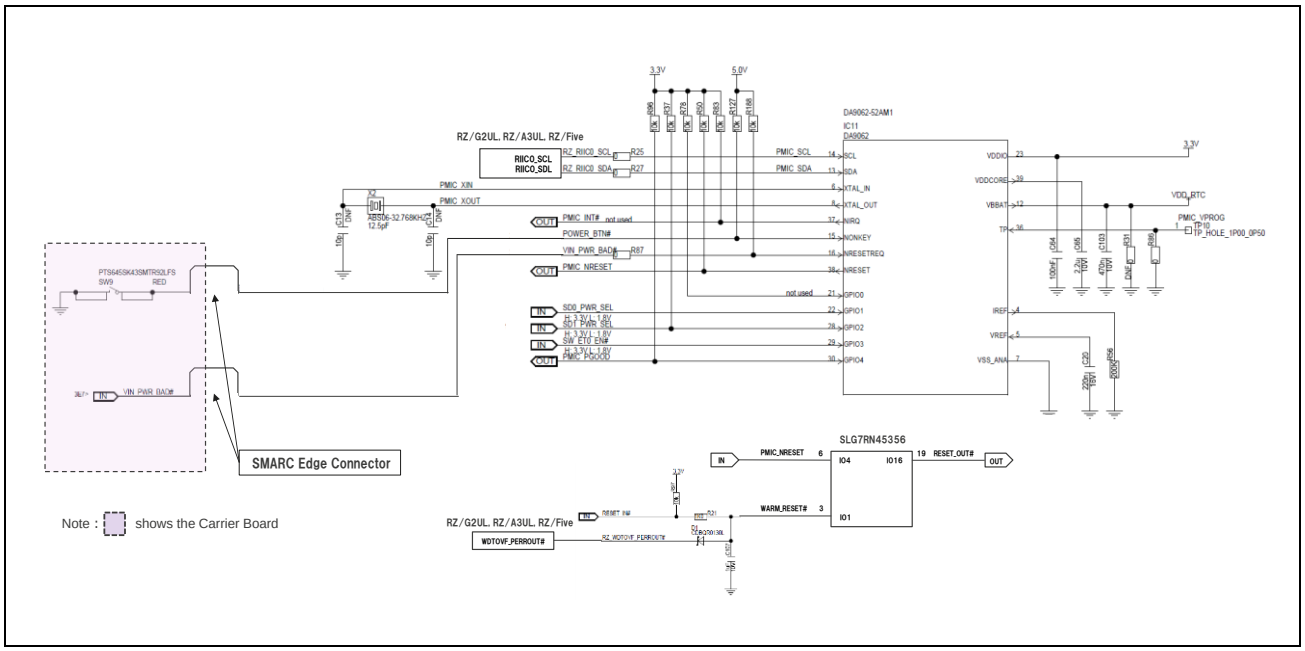


Figure 2.10 Block Diagrams of Power Regulation

2.9 PMIC

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Edition | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board OCTAL Edition

Figure 2.11 shows the RZ/G2UL pin assignment for PMIC.

LDO2 and LDO3 output voltage value for supply SD0_PVDD and SD1_PVDD are fixed by P6_1 and P6_2.

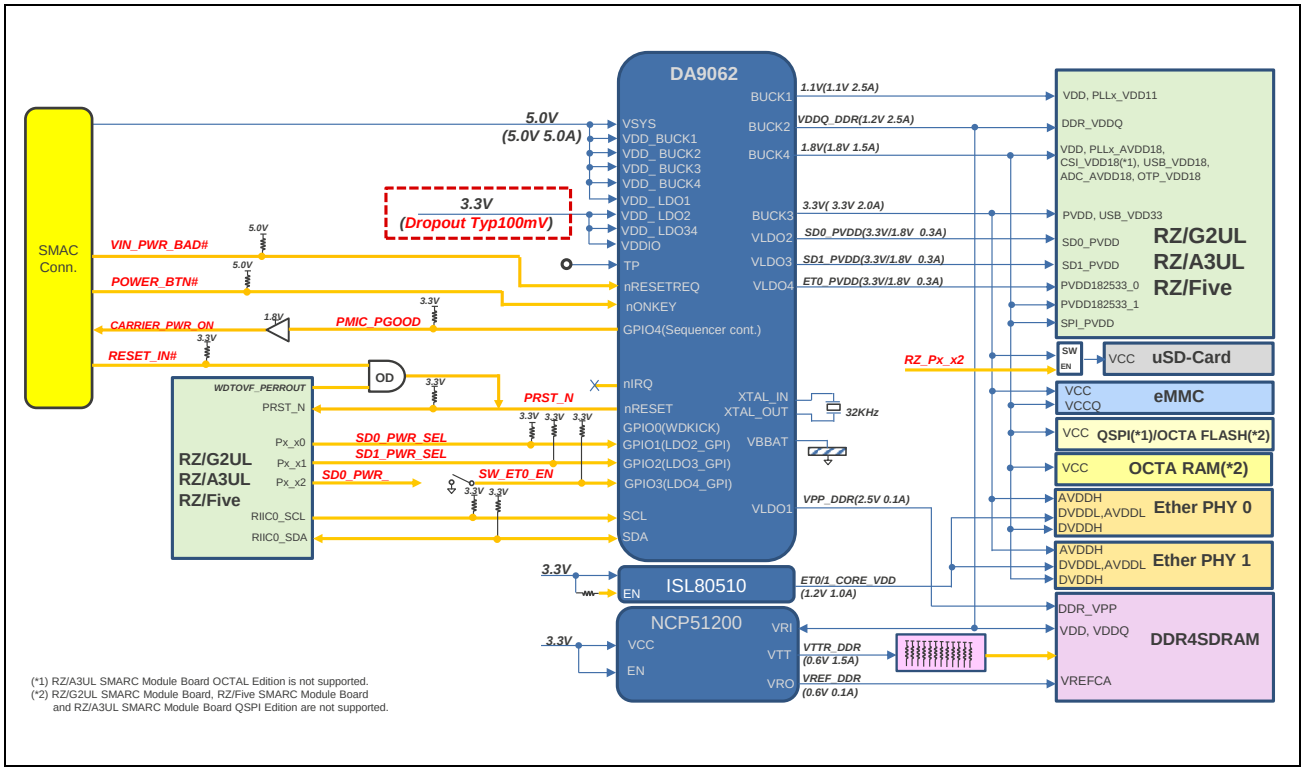


Figure 2.11 Block Diagram around PMIC

2.10 Debug Interface

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Edition | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board OCTAL Edition

Figure 2.12 shows a block diagram of debug interface.

Ths interface supports JTAG and SWD and has debug support for Cortex-A55 and Cortex-M33.

The default operation for the debug interface uses pin 9 as a ground detect, although with resitor(R20) fitting options, it is possible to use this to independently drive the JTAG_TRST#.

When debug mode is disabled (SW1-1: DEBUGEN is ON), JTAG_TRST# is permanently low.

On the other hands, when debug mode is enabled (SW1-1: DEBUGEN is OFF), JTAG_TRST# is initially low on powerup and then ramps up to 1.8V.

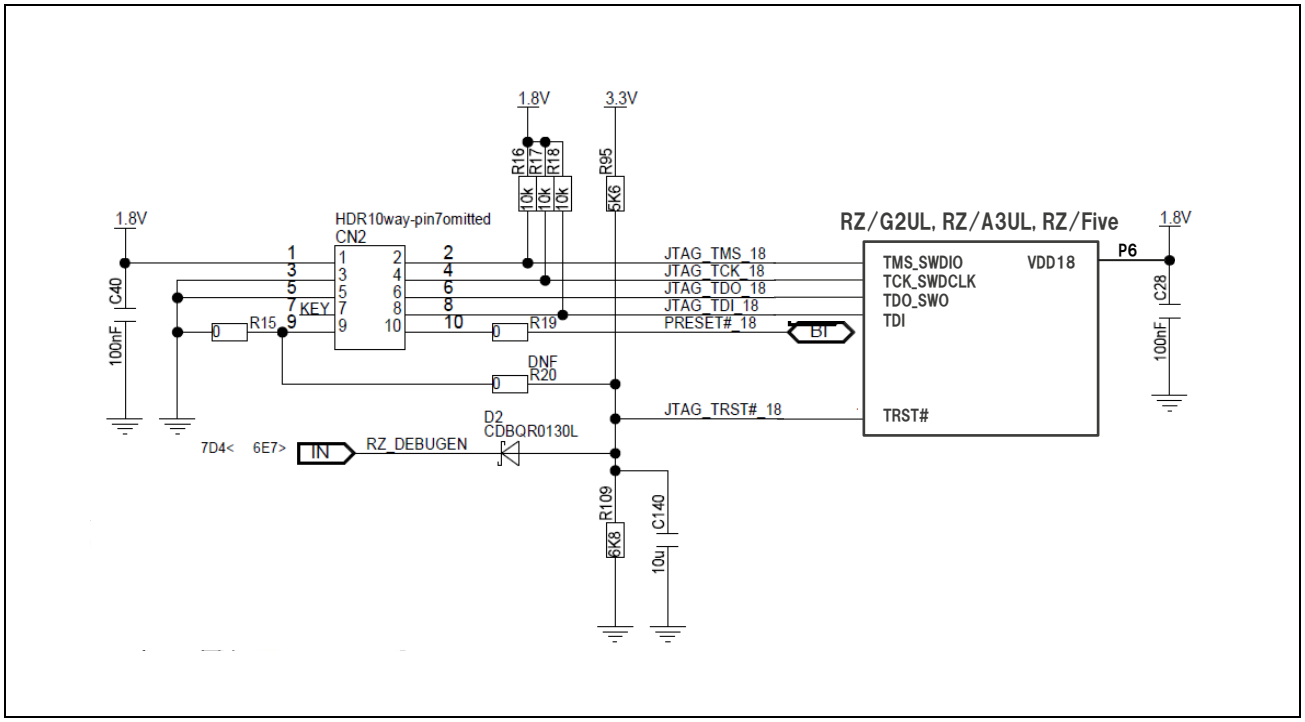


Figure 2.12 Block Diagram of Debug I/F

2.11 SD/MMC Host Interface

2.11.1 eMMC Memory

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Edition | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board OCTAL Edition

Figure 2.13 shows a block diagram of the MMC interface.

The eMMC memory is connected to channel 0 of SD/MMC interface that is with built-in to the RZ/G2UL. This memory is used in conjunction with SD card.

The eMMC memory may be used when

- the SW_SD0_DEV_SEL is enabled (SW1-2: Selection SD/MMC is OFF).

This interface complies with the JEDEC standard version 4.51 and supports HS200 mode.

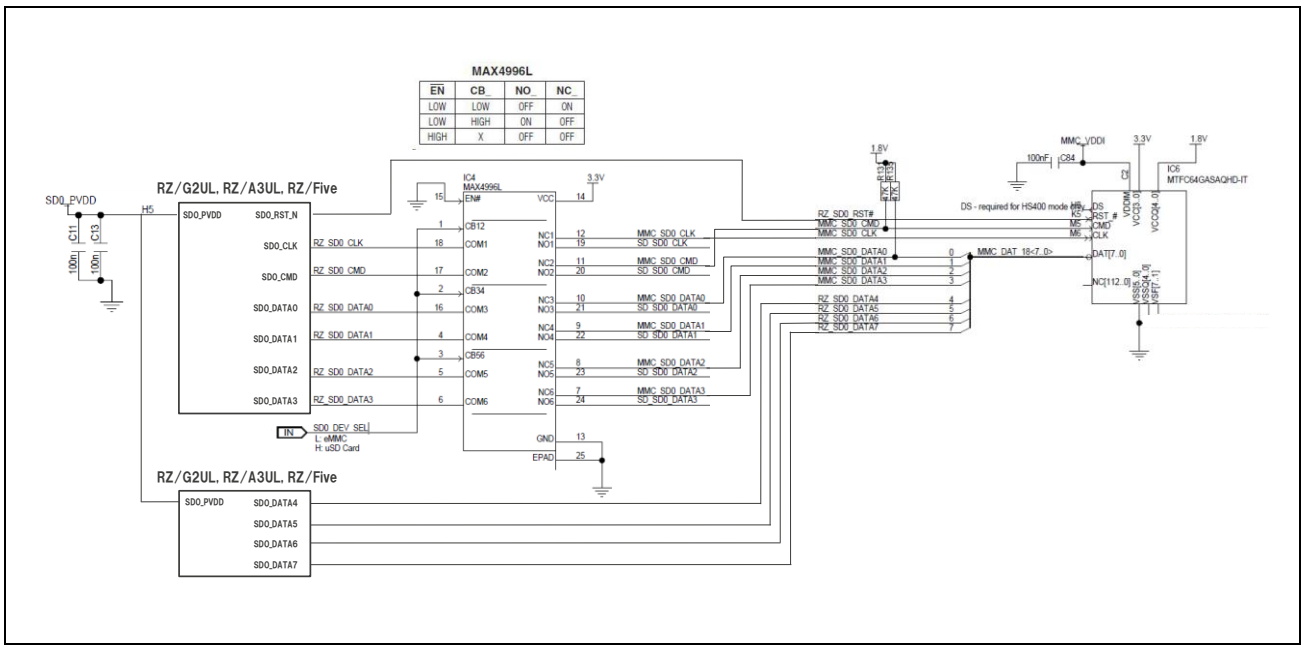


Figure 2.13 Block Diagram of eMMC I/F

2.11.2 SD Card

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Edition | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board OCTAL Edition

Figure 2.14 shows a block diagram of the SD0 interface.

The microSD card is connected to channel 0 of SD/MMC interface that is with built-in to the RZ/G2UL. This memory is used in conjunction with eMMC memory.

The microSD card may be used when

- the microSD is the selected boot mode (SW11-1: ON, SW11-2: ON, SW11-3: OFF)
- the SW_SD0_DEV_SEL is disabled (SW1-2: Selection SD/MMC is ON) and eMMC memory is not the selected boot mode (SW11-1: ON, SW11-2: OFF, SW11-3: OFF).

This interface complies with the memory card standard version 3.0 and supports UHS-I mode of 50MB/s (SDR50) and 104MB/s (SDR104).

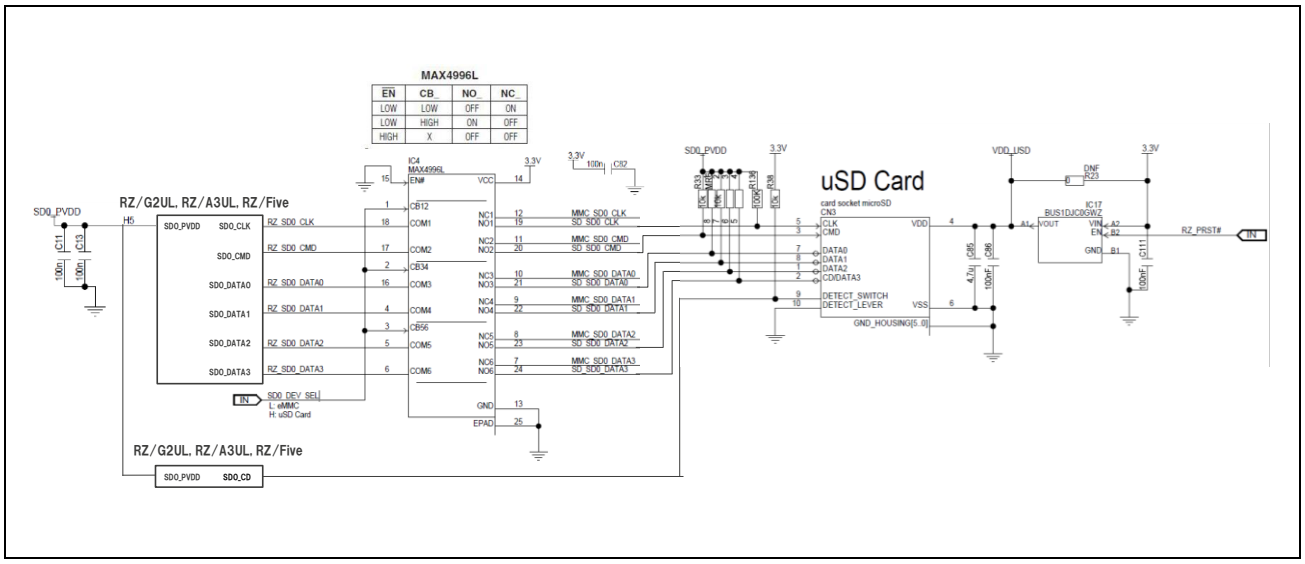


Figure 2.14 Block Diagram of SD0 I/F

2.12 GreenPAK

RZ/G2UL SMARC Module Board | RZ/A3UL SMARC Module Board QSPI Edition | RZ/Five SMARC Module Board | RZ/A3UL SMARC Module Board OCTAL Edition

Figure 2.15 shows a block diagram of the GreenPAK.

This board is implemented several types of the GreenPAK with integrated various peripheral functions. **Table 2.3** shows a function of the each GreenPAK used with this board.

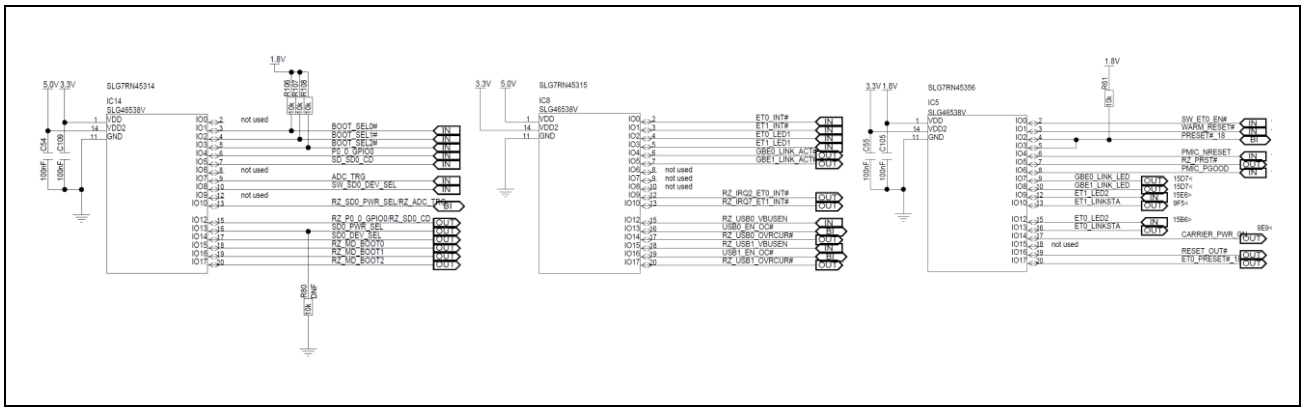


Figure 2.15 Block Diagram of Each GreenPAK

Table 2.3 Features of Each GreenPAK

Type Name	Description
SLG7RN45314	SMARC Boot Mode SD0_CD / GPIO4 multiplexing SD0_PWR_SEL / ADC_TRG multiplexing SD0_DEV_SEL (microSD card or eMMC)
SLG7RN45315	USB0/1 Logic for EN_OC# Etehnet0/1 Logic for interrupt level shifting LINK Active LED drive
SLG7RN45356	Reset Logic SMARC Carrier Power ON Ethernet0/1 LINK LED drive LINK status inversion

The pin configuration and of each GreenPAK is described in the next section. Please refer to the following data sheet included with the design data in detail.

- SLG7RN45314_DS_r014_12152021.pdf
- SLG7RN45315_DS_r011_10292021.pdf
- SLG7RN45356_DS_r010_11012021.pdf

2.13 Parallel Output Interface

RZ/G2UL SMARC Module Board

RZ/A3UL SMARC Module Board QSPI Edition

RZ/A3UL SMARC Module Board OCTAL Edition

Figure 2.16 shows a block diagram of the Parallel Output interface.

This interface is controlled by the LCD controller (LCDC) with that is built-in to the RZ/G2UL. This interface supports RGB888 for input format.

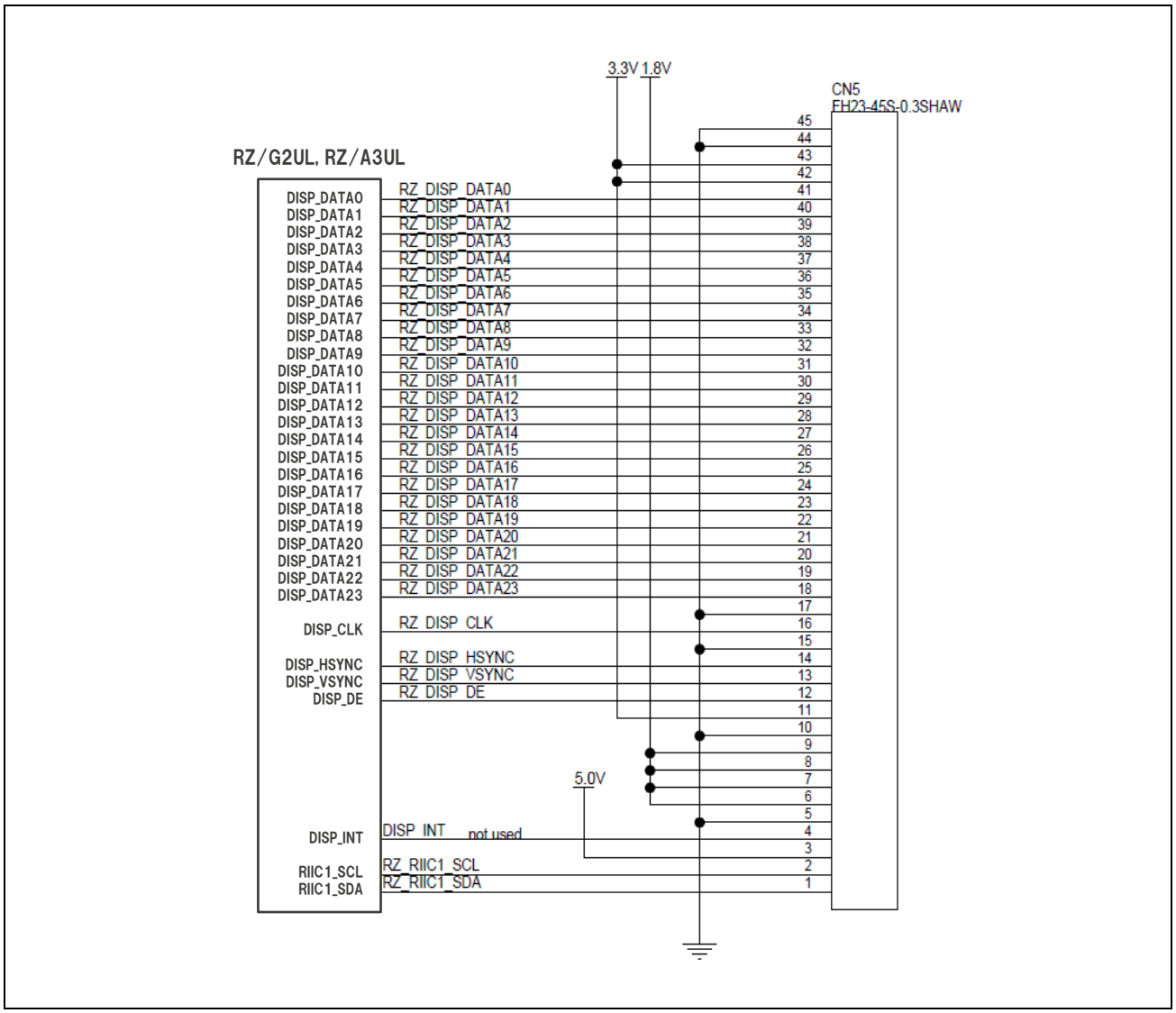


Figure 2.16 Block Diagram of Parallel Output I/F

3. Operation Specifications

3.1 Overview of Connectors

Figure 3.1 Illustrates the layout of connectors of the RTK9743U11C01000BE.

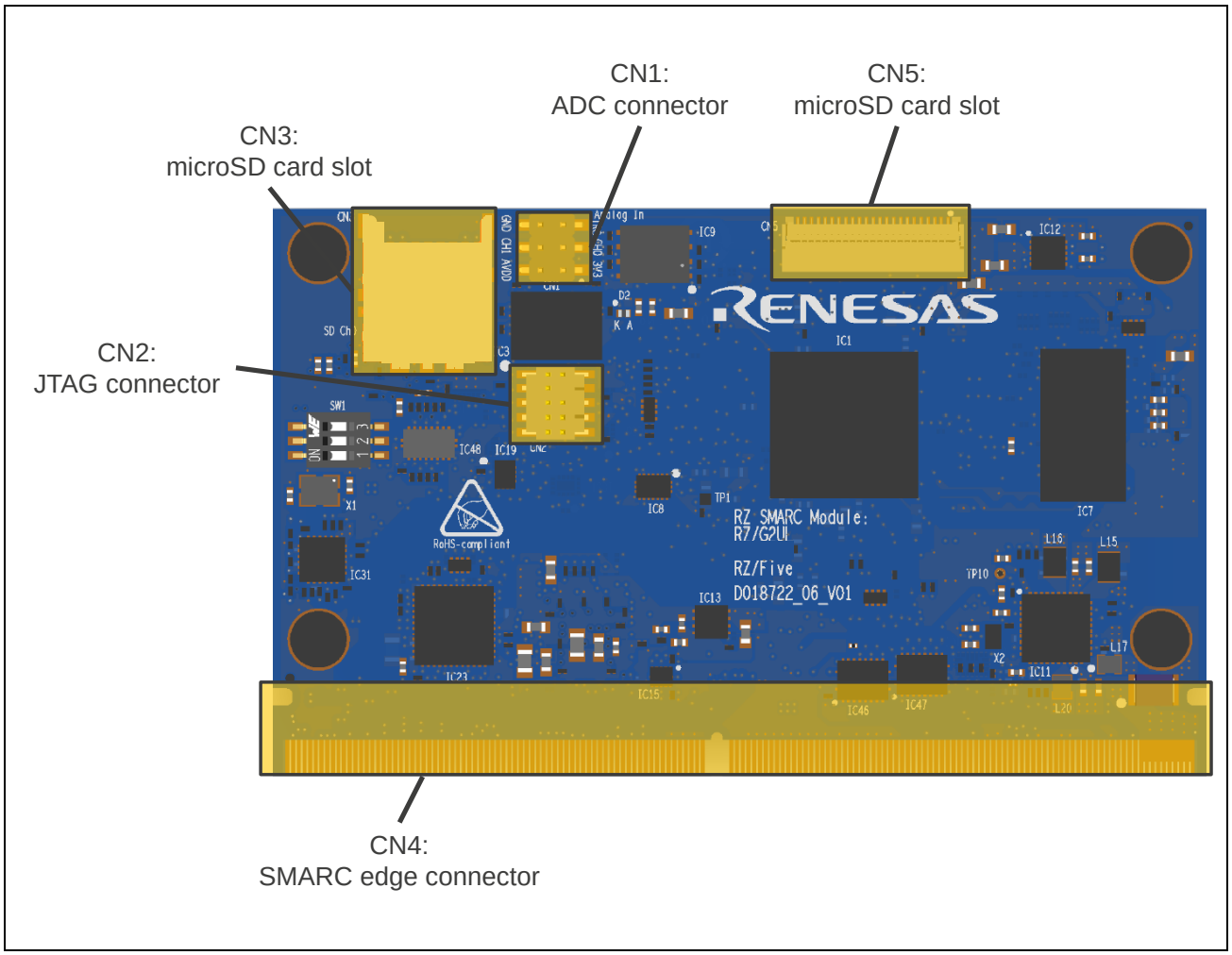


Figure 3.1 Layout of connectors of the RTK9743U11C01000BE (Top side)

3.1.1 ADC Connector (CN1)

The RTK9743U11C01000BE contains a connector of ADC interface (CN1).

Figure 3.2 illustrates the layout of the connector pins. **Table 3.1** shows the assignment of the connector pins.

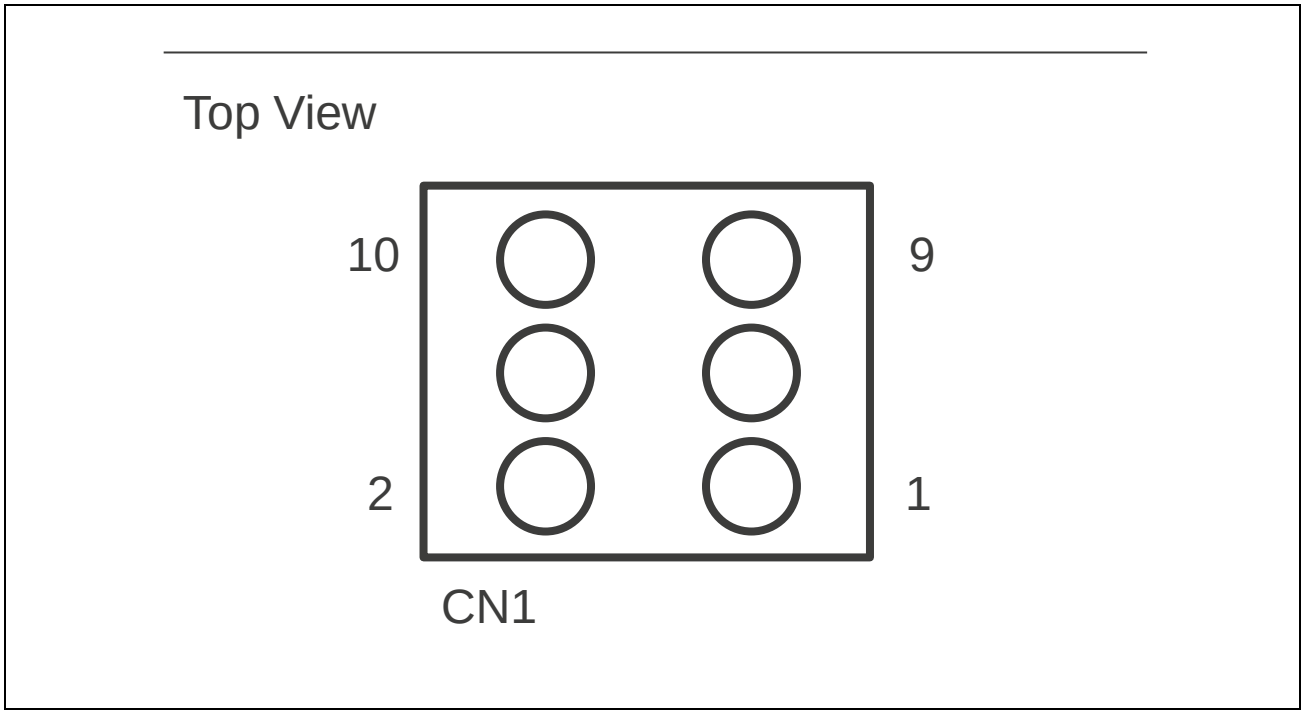


Figure 3.2 ADC Connector (CN1) Pin Layout Diagram

Table 3.1 ADC Connector (CN1) Pin Layout Table

Pin	Signal Name
1	PVDD
2	ADC_AVDD18
3	ADC_CH0
4	ADC_CH1
5	ADC_TRG
6	VSS

3.1.2 JTAG Connector (CN2)

The RTK9743U11C01000BE contains a connector of debug interface (CN2).

Figure 3.3 illustrates the layout of the connector pins. **Table 3.2** shows the assignment of the connector pins.

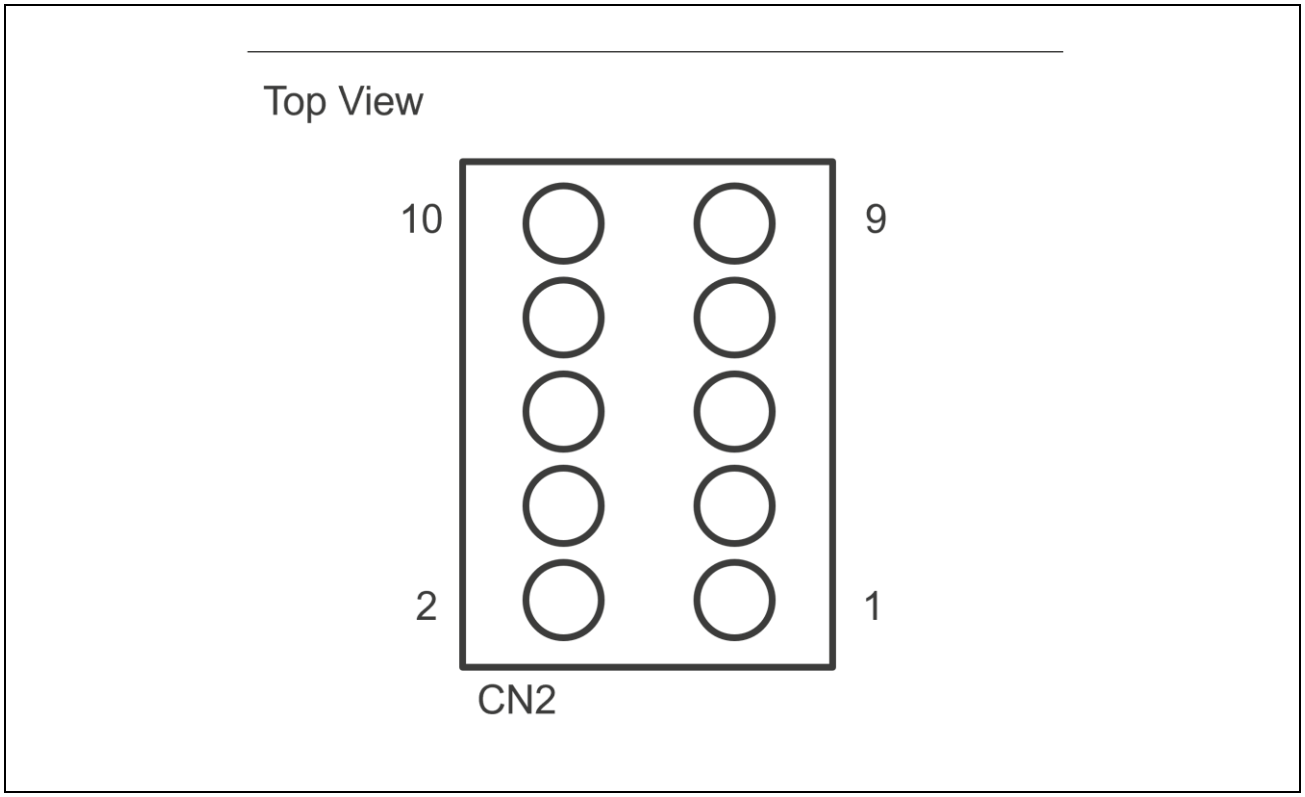


Figure 3.3 JTAG Connector (CN2) Pin Layout Diagram

Table 3.2 JTAG Connector (CN2) Pin Layout Table

Pin	Signal Name
1	PVDD18
2	TMS/SWDIO
3	VSS
4	TCK/SWDCLK
5	VSS
6	TDO
7	—
8	TDI
9	VSS
10	TRST#

3.1.3 MicroSD Card Slot (CN3)

The RTK9743U11C01000BE contains a microSD card slot (CN3).

Figure 3.4 illustrates the layout of microSD card slot pins. **Table 3.3** shows the assignment of microSD card slot pins.

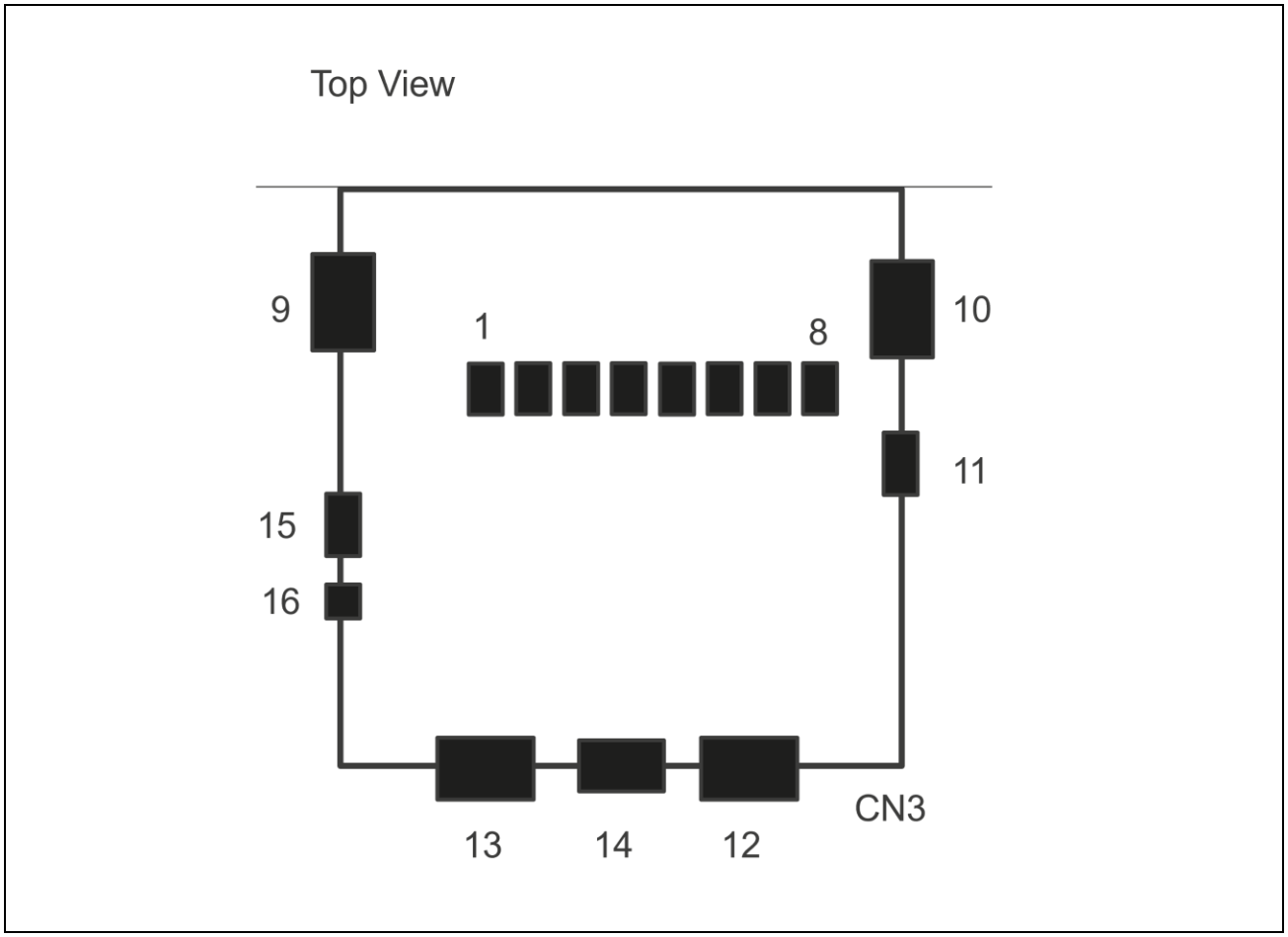


Figure 3.4 microSD Card Slot (CN3) Pin Layout Diagram

Table 3.3 microSD Card Slot (CN3) Pin Layout Table

Pin	Signal Name
1	SD0_DATA2
2	CD/SD0_DATA3
3	SD0_CMD
4	SD0_PVDD
5	SD0_CLK
6	VSS
7	SD0_DATA0
8	SD0_DATA1
9	DETECT_SWITCH
10	DETECT_LEVER

3.1.4 SMARC edge Connector (CN4)

The RTK9743U11C01000BE can be connected to an external expansion board through the Carrier board connecting connector (CN4).

Figure 3.5 illustrates the layout of Carrier board connecting connector pins. For the assignment of Carrier board connecting connector pins, please refer to the section 4 “MODULE PIN-OUT MAP” of the document “SMARC module 2.1 Specification (sget.org)”.

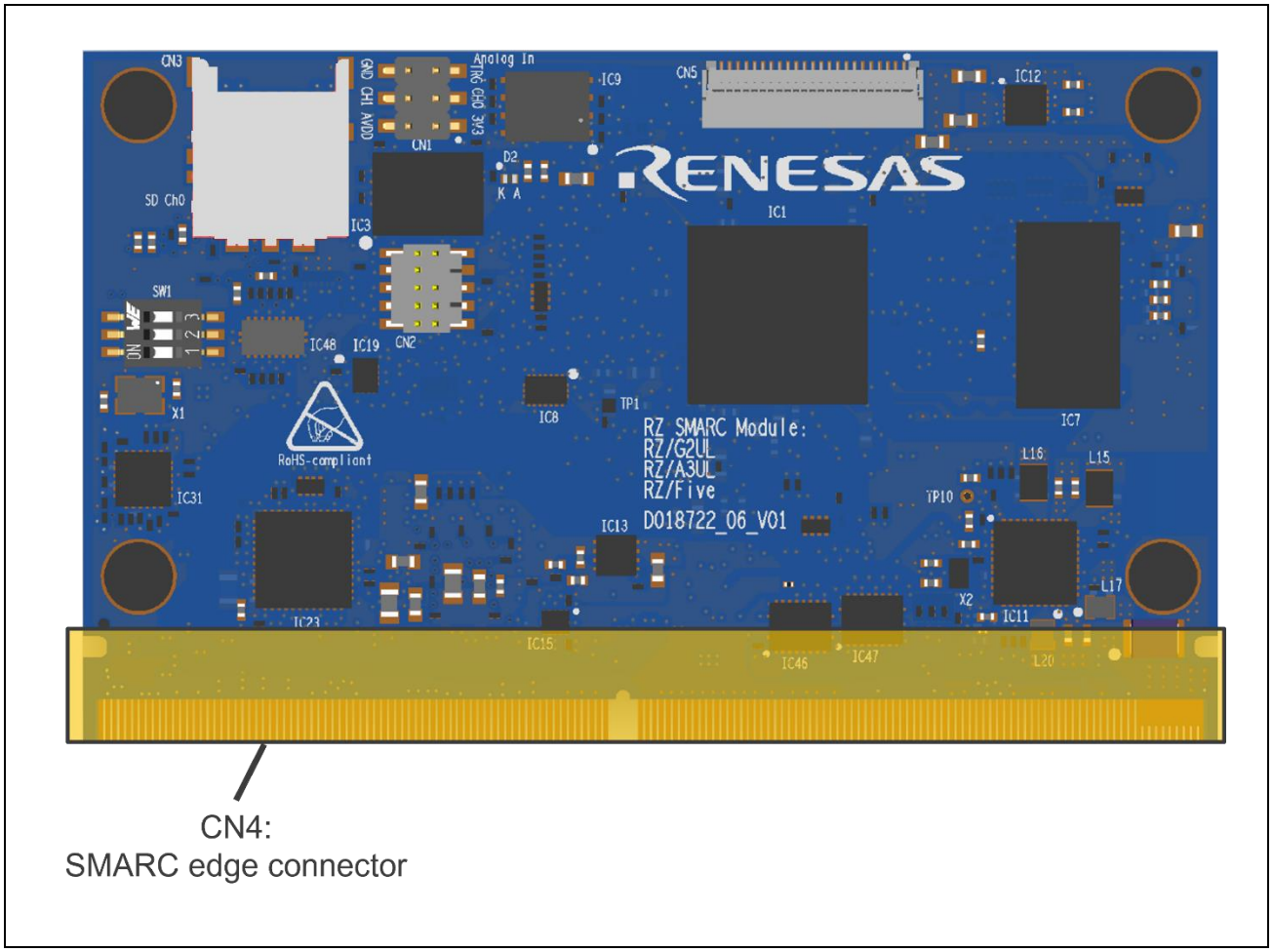


Figure 3.5 Layout of Carrier Board Connecting Pins

3.1.5 FFC/FPC Connector(CN5)

The RTK9743U11C01000BE contains a FFC/FPC Connector for the Parallel Output Interface (CN5).

Figure 3.6 illustrates the layout of the connector pins. **Table 3.4** shows the assignment of the connector pins.

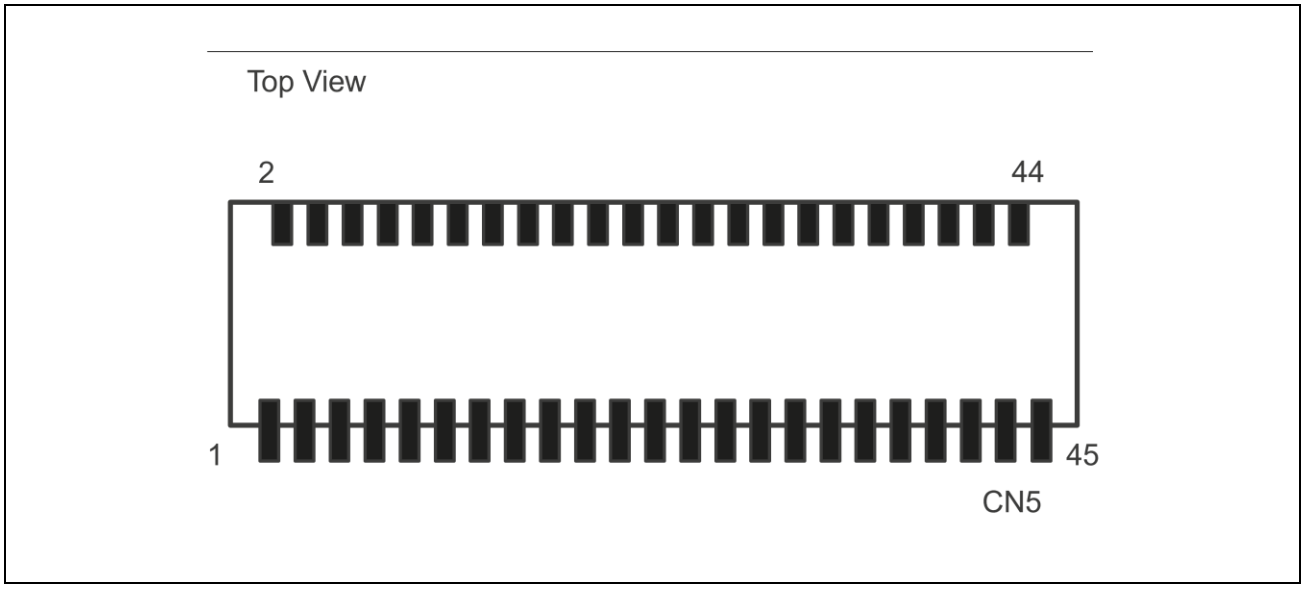


Figure 3.6 FFC/FPC Connector (CN5) Pin Layout Diagram

Table 3.4 FFC/FPC Connector (CN5) Pin Layout Table

Pin	Signal Name	Pin	Signal Name
1	RIIC1_SDA	24	DISP_DATA17
2	RIIC1_SCL	25	DISP_DATA16
3	5.0V	26	DISP_DATA15
4	DISP_INT	27	DISP_DATA14
5	VSS	28	DISP_DATA13
6	1.8V	29	DISP_DATA12
7	1.8V	30	DISP_DATA11
8	1.8V	31	DISP_DATA10
9	1.8V	32	DISP_DATA9
10	VSS	33	DISP_DATA8
11	3.3V	34	DISP_DATA7
12	DISP_DE	35	DISP_DATA6
13	DISP_VSYNC	36	DISP_DATA5
14	DISP_HSYNC	37	DISP_DATA4
15	VSS	38	DISP_DATA3
16	DISP_CLK	39	DISP_DATA2
17	VSS	40	DISP_DATA1
18	DISP_DATA23	41	DISP_DATA0
19	DISP_DATA22	42	3.3V
20	DISP_DATA21	43	3.3V
21	DISP_DATA20	44	VSS
22	DISP_DATA19	45	VSS
23	DISP_DATA18		

3.2 Layout of Operation Components

Figure 3.7 illustrates the layout of operation components of the RTK9743U11C01000BE.

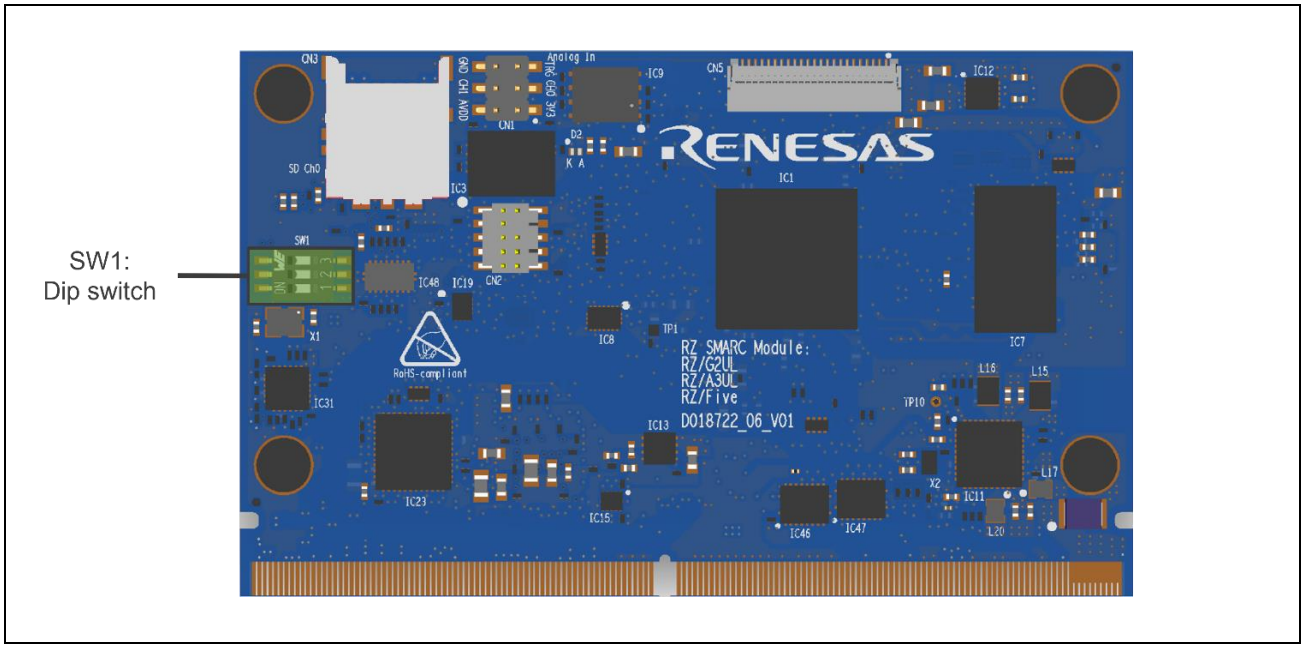


Figure 3.7 Layout of Operation Components of the RTK9743U11C01000BE

3.2.1 Functions of Switches and Mode Terminals

The RTK9743U11C01000BE contains one switch.

Table 3.5 lists mounted switches. **Figure 3.8** shows a block diagram of the System Setting interface.

Table 3.5 Switches Mounted on the RTK9743U11C01000BE

No.	Function	Note
SW1	System setting DIP switch	For details, see **Table 3.6** to **Table 3.8**

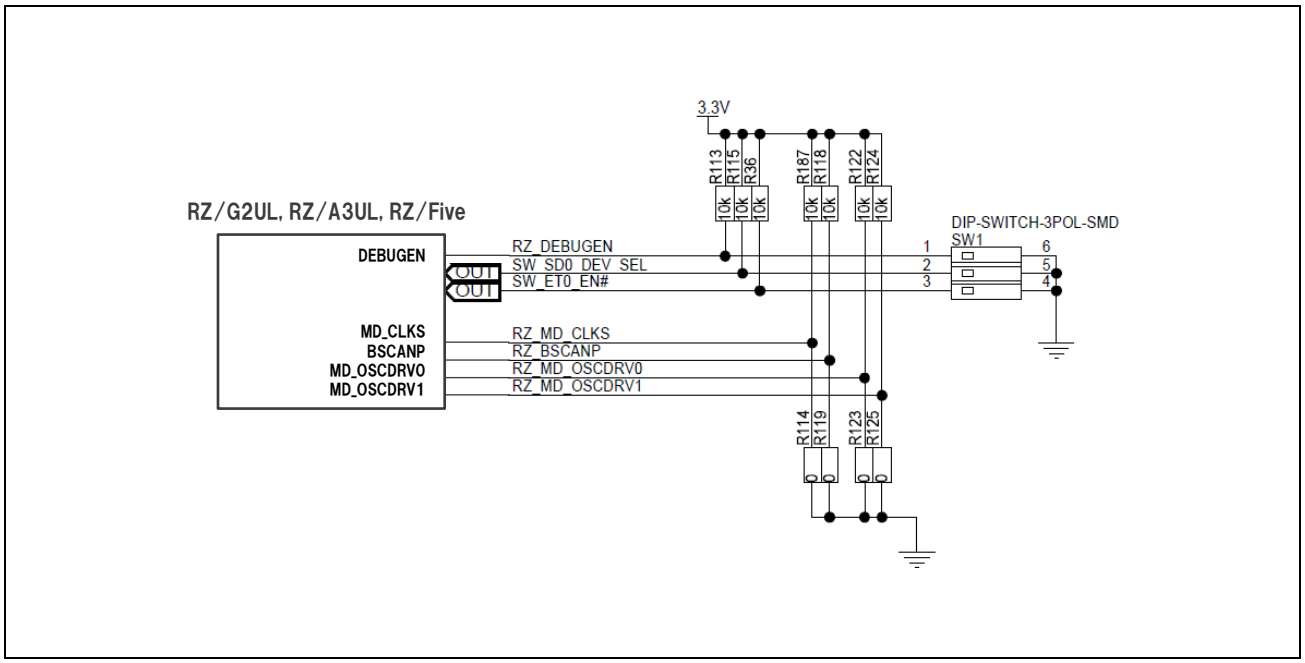


Figure 3.8 Block Diagram of System Setting I/F

Table 3.6 provides functions of the DIP switch and **Figure 3.9** indicates a default terminal state.

Table 3.6 Functions of System Setting DIP Switch (SW1)

No.	Setting		Function
SW1-1 DEBUGEN	OFF	DEBUGEN="H"	JTAG debugging
	ON	DEBUGEN="L"	Normal operation (default)
SW1-2 Selection SD/MMC	OFF	Selection="H"	Select the eMMC memory (default)
	ON	Selection="L"	Select the microSD card
SW1-3 Selection Ethernet0/Peripherals	OFF	Selection="H"	Select the CAN0, Can1, RSPI1, SSI1 signals (default)
	ON	Selection="L"	Select the Ethernet0 signals

Figure 3.9 Default Setting of System Setting DIP Switch (SW1)

By setting SW1-3 to the following settings, the RTK9743U11C01000BE can be used various interfaces. **Table 3.7** provides functions by SW1-3. **Table 3.8** provides functions of mode terminals.

Table 3.7 GPIO Signals by SW1-3

		Setting	
		SW1-3 =“L”	SW1-3 =“H”
Signal Name	P1_2	ET0_TXD0	CAN0_RX
	P1_3	ET0_TXD1	GPIO6
	P1_4	ET0_TXD2	GPIO7
	P2_0	ET0_TXD3	CAN1_TX
	P3_2	ET0_RXD0	SSI1_TXD
	P3_3	ET0_RXD1	SSI1_RXD
	P4_0	ET0_RXD2	RSPI1_CK
	P4_1	ET0_RXD3	RSPI1_MOSI
	P1_0	ET0_TXC	GPIO5
	P1_1	ET0_TX_CTL	CAN0_TX
	P3_0	ET0_RXC	SSI1_BCK
	P3_1	ET0_RX_CTL	SSI1_RCK
	P4_3	ET0_MDC	RSPI1_SSL
	P4_4	ET0_MDIO	GPIO1
	P4_5	ET0_LINKSTA	GPIO11
	P5_1	ET0_INT#	GPIO10
Application		Ethernet0	CAN0/1 Audio PMOD0 (Type-2A) PMOD1 (Type-6)

Table 3.8 Functions of System Setting

No.	Setting		Function
MD_CLKS	0	MD_CLKS=“H”	SSCG ON
	1	MD_CLKS=“L”	SSCG OFF
BSCANP	0	BSCANP=“H”	Select the eMMC memory
	1	BSCANP=“L”	Select the SD card
MD_OSCDRV0	0	MD_OSCDRV0=“H”	Not supported
	1	MD_OSCDRV0=“L”	
MD_OSCDRV1	0	MD_OSCDRV1=“H”	Not supported
	1	MD_OSCDRV1=“L”	

4. Parallel to HDMI Conversion Board

RZ/G2UL SMARC Module Board

RZ/A3UL SMARC Module Board QSPI Edition

RZ/A3UL SMARC Module Board OCTAL Edition

4.1 Configuration

The Parallel to HDMI Conversion Board is connected to the FFC/FPC Connector (CN5) described in the **section 3.1.5** to realize parallel output via the 50mm FPC.

Figure 4.1 shows an example of system configuration using the Parallel to HDMI Conversion Board.

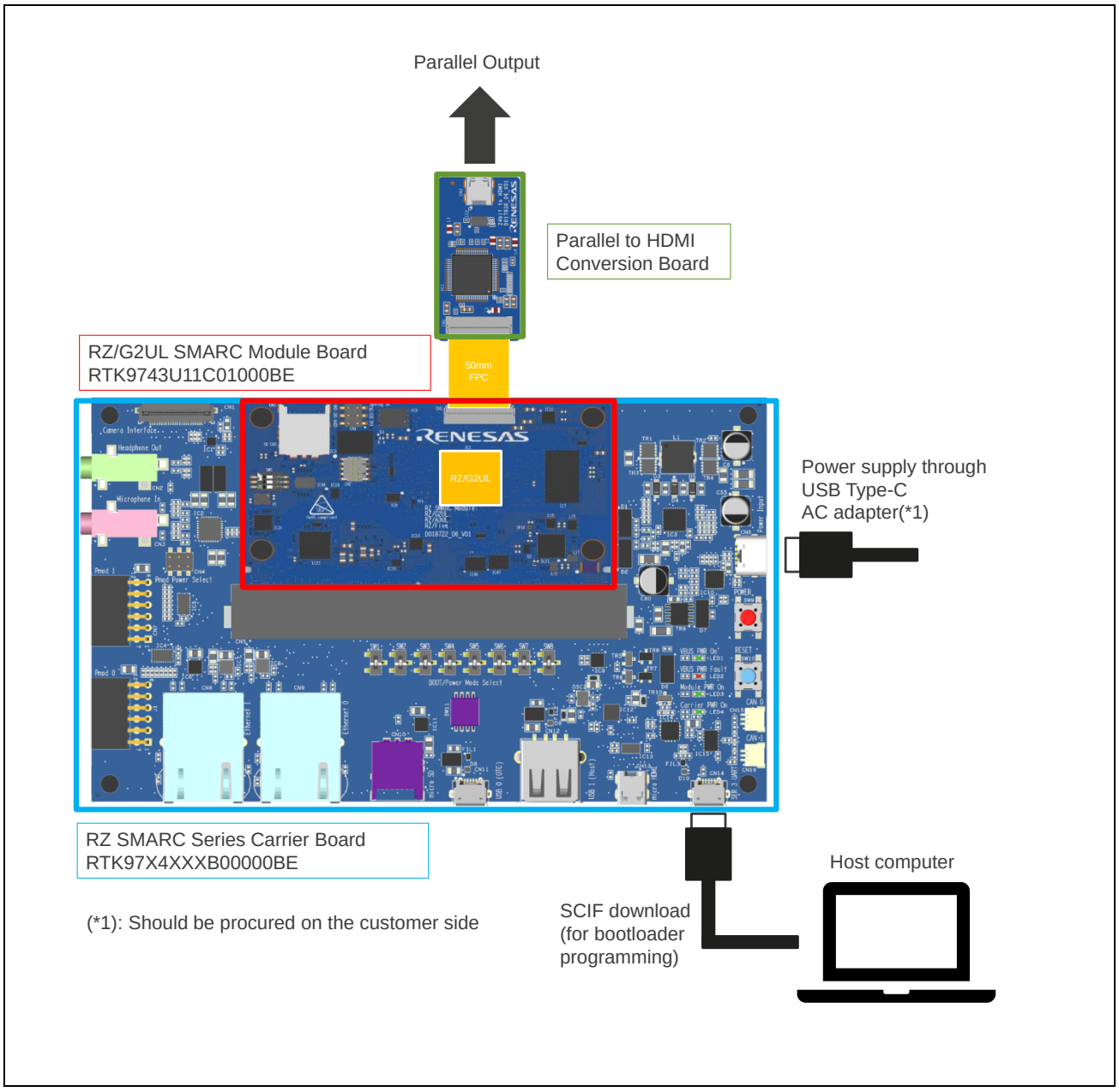


Figure 4.1 Example of System Configuration Using the Parallel to HDMI Conversion Board

The connection procedure of the 50mm FPC is follows.

The top and bottom surfaces of the FPC are shown below.

Top surface

Bottom surface

Figure 4.2 Top and Bottom Views of the 50mm FPC

1. Lift up the actuator. Use thumb or index finger.

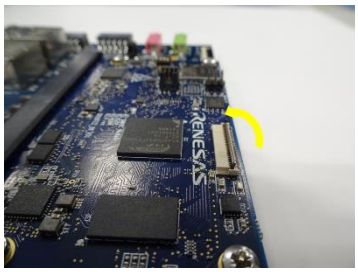


Figure 4.3 How to install the 50mm FPC (1)

2. Fully insert the FPC in the connector parallel to mounting surface, with the exposed conductive traces facing down

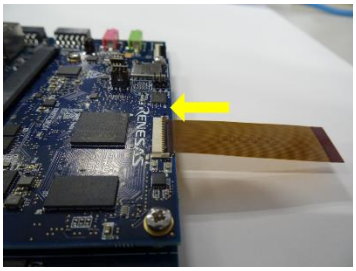


Figure 4.4 How to install the 50mm FPC (2)

3. Rotate down the actuator until firmly closed.

NOTE

The PFC must be fully inserted in the connector. If not fully inserted, the actuator will not close property.

Should this be the case, lift up the actuator and repeat the process (starting with Step 1 above)

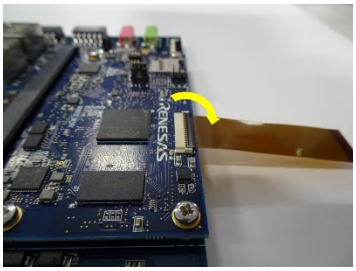


Figure 4.5 How to install the 50mm FPC (3)

4. FPC Removal
   1) Lift up the actuator.
   2) Carefully remove the FPC

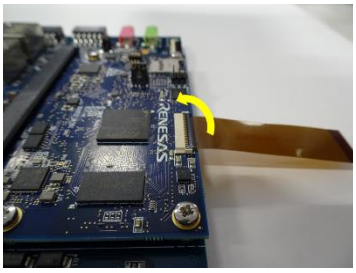


Figure 4.6 How to remove the 50mm FPC

4.2 Features

Table 4.1 shows the features of the Parallel to HDMI Conversion Board.

Table 4.1 Features of the Parallel to HDMI Conversion Board

Item	Details
Video IC	HDMI transceiver: 1pc
Connector	FFC/FPC connector (45pin): 1pc microHDMI connector: 1pc
Circuit board specifications	Dimensions: 20 mm * 40 mm Mount: Single-sided mounting (6 layers)

4.3 Physical View

Figure 4.7 shows the top and bottom views of the Parallel to HDMI Conversion Board..

Figure 4.7 Top and Bottom Views of the Parallel to HDMI Conversion Board

4.4 Component Layout

Figure 4.8 shows the layout of main components of the Parallel to HDMI Conversion Board.

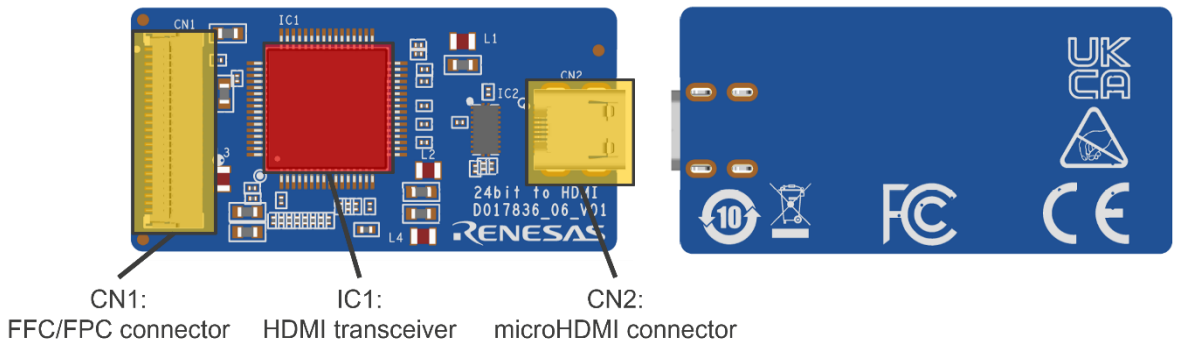


Figure 4.8 Layout of Components of the Parallel to HDMI Conversion Board (Top and bottom View)

Table 4.2 and **Table 4.3** list main components mounted on the Parallel to HDMI Conversion Board.

Table 4.2 Main Components on the Parallel to HDMI Conversion Board (1) IC

Component Number	Component Name	Type (Manufacturer)	Recommended Optional Components
IC1	HDMI Transmitter	ADV7513BSWZ (Analog Devices)	

Table 4.3 Main Components on the Parallel to HDMI Conversion Board (2) Connector

Components Number	Component Name	Type (Manufacturer)	Recommend Optional Parts
CN1	FFC/FPC connector (45pin)	FH23-45S-0.3SHAW(05) (HIROSE)	
CN2	microHDMI connector	46765-1301 (Molex)	

5. Appendix

5.1 Type Name and Features of Each Board

This section describes the the type name and feature of each board here.

The SMARC Module Board is as follows. This picture is of the RTK9743U11C01000BE.

Figure 5.1 Top View of the SMARC Module Board

The SMARC Module Boards with RZ/G2UL, RZ/A3UL and RZ/Five are used common PCB layout and designed to be pin-compatible and available for use.

Please refer to the **section 2 “Functional Specifications”** onwards for the actual functions of the board.

Board Name	Type Name	MPU	Memory Configuration	Parallel to HDMI Conversion Board
RZ/G2UL SMARC Module Board	RTK9743U11C01000BE	RZ/G2UL (R9A07G043U11GBG)	QSPI flash memory DDR4 SDRAM	Included
RZ/Five SMARC Module Board	RTK9743F01C01000BE	RZ/Five (R9A07G043F01GBG)	QSPI flash memory DDR4 SDRAM	Not Included
RZ/A3UL SMARC Module Board QSPI Edition	RTK9763U02C01000BE	RZ/A3UL (R9A07G063U02GBG)	QSPI flash memory DDR4 SDRAM	Included
RZ/A3UL SMARC Module Board OCTAL Edition	RTK9763U02C01001BE	RZ/A3UL (R9A07G063U02GBG)	Octa RAM memory Octa Flash memory DDR4 SDRAM	Included

The RZ SMARC Series Carrier Board is as follows. This picture is of the RTK97X4XXXB00000BE.

Figure 5.2 Top View of the RZ SMARC Series Carrier Board

Board Name	Type Name
RZ SMARC Series Carrier Board	RTK97X4XXXB00000BE

The Evaluation board Kit is as follows. This board consists of the SMARC Module Board and the RZ SMARC Series Carrier Board via a 314-pin 0.5-mm pitch connector. This picture is of the RTK9743U11S01000BE.

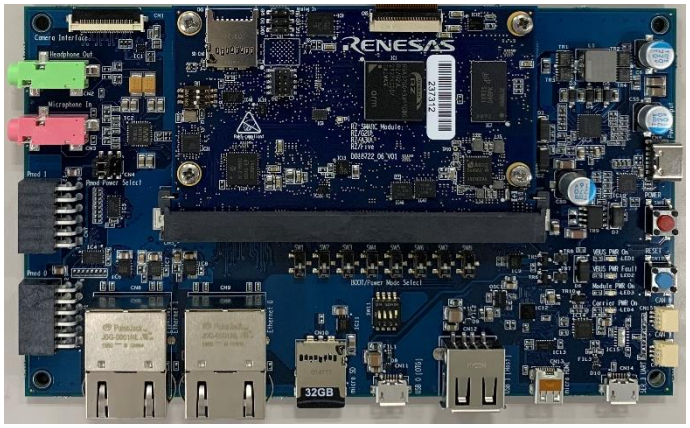


Figure 5.3 Top View of the Evaluation board Kit

The Evaluation board Kits are similarly designed to use a common board layout and to be pin-compatible.

Board Name	Type Name	MPU	Memory Configuration	Parallel to HDMI Conversion Board
Evaluation board Kit for RZ/G2UL MPU	RTK9743U11S01000BE	RZ/G2UL (R9A07G043U11GBG)	QSPI flash memory DDR4 SDRAM	Included
Evaluation board Kit for RZ/Five MPU	RTK9743F01S01000BE	RZ/Five (R9A07G043F01GBG)	QSPI flash memory DDR4 SDRAM	Not Included
Evaluation board Kit for RZ/A3UL MPU QSPI Edition	RTK9763U02S01000BE	RZ/A3UL (R9A07G063U02GBG)	QSPI flash memory DDR4 SDRAM	Included
Evaluation board Kit for RZ/A3UL MPU OCTAL Edition	RTK9763U02S01001BE	RZ/A3UL (R9A07G063U02GBG)	Octa RAM memory Octa Flash memory DDR4 SDRAM	Included

5.2 How to Identify Each SMARC Module Board

The differences between each SMARC Module Board are as follows. This picture is of the RTK9743U11C01000BE.

Table 5.1 Comparison of the RTK9743U11C01000BE and the RTK9743F01C01000BE

Type Name	RTK9743U11C01000BE	RTK9743F01C01000BE
IC1	RZ/G2UL (R9A07G043U11GBG)	RZ/Five (R9A07G043F01GBG)

Table 5.1 Comparison of the RTK9743U11C01000BE and the RTK9763U02C01000BE

Type Name	RTK9743U11C01000BE	RTK9763U02C01000BE
IC1	RZ/G2UL (R9A07G043U11GBG)	RZ/A3UL (R9A07G063U02GBG)

Table 5.2 Comparison of the RTK9763U02C01000BE and the RTK9763U02C01001BE

Type Name	RTK9763U02C01000BE	RTK9763U02C01001BE
IC2	Not mounted	OctaFlash
IC3	Not mounted	OctaRAM
IC9	QSPI flash memory	Not mounted

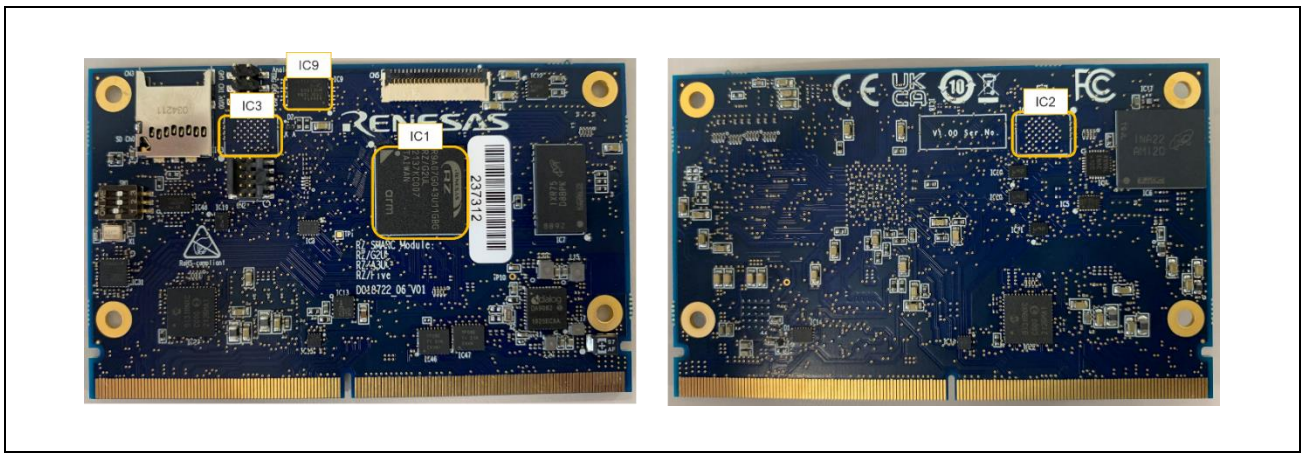


Figure 5.4 Comparison of Each SMARC Module Board

5.3 How to replace the SMARC Module Board

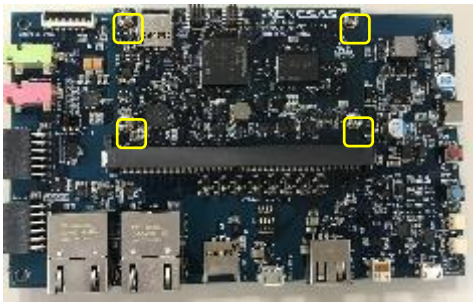
Please be careful when replacing the board as follows.

1. Remove the four screws.

NOTE

The screw thread is a special shape, so be careful not to crush the screw thread.

Please recommend to prepare a torx screwdriver which is a “T6” head size.



Specially shaped screw threads

Figure 5.5 How to remove the screws

2. Remove the screw and the SMARC Module Board will stand up at an angle. Slide it out.

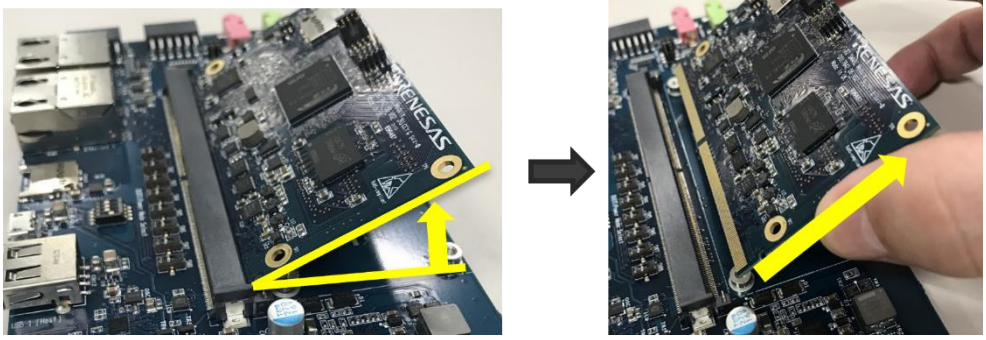


Figure 5.6 How to remove the SMARC Module Board

3. Insert the replacement the SMARC Module Board diagonally, then roll the board parallel to the RZ SMARC Series Carrier Board and fix it with screws.

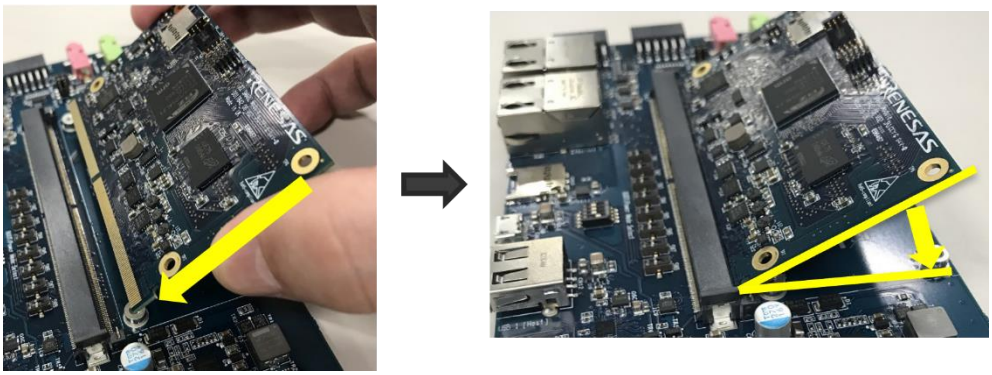


Figure 5.7 How to install the SMARC Module Board

REVISION HISTORY	RZ Family / RZ/G, RZ/A Series RZ/G2UL, RZ/A3UL, RZ/Five SMARC Module Board

Rev.	Date	Description	
		Page	Summary
1.00	Jun 27, 2022	—	First edition issued
1.01	Jul 28, 2022	9, 15	The section title is changed from "RT9743U11C01000BE" to "RTK9743U11C01000BE"
		10, 16	The section title is changed from "RT9763U02C01000BE" to "RTK9763U02C01000BE"
		11, 17	The section title is changed from "RT9763U02C01001BE" to "RTK9763U02C01001BE"
		12, 18	The section title is changed from "RT9743F01C01000BE" to "RTK9743F01C01000BE"

RZ/G2UL, RZ/A3UL, RZ/Five SMARC Module Board
User's Manual: Hardware

Publication Date:	Rev.1.01	Jul 28, 2022
	Rev.1.00	Jun 27, 2022

Published by: Renesas Electronics Corporation

RZ Family / RZ/G, RZ/A Series

Renesas Electronics Corporation

R01UH0990EJ0101