Title	***Reference Design Report for a 7 W, Wide Range Input, Dual Output, Non-Isolated Flyback Converter Using LinkSwitch™-XT2-900 LNK3696P***
Specification	85 VAC – 440 VAC Input; 12.0 V / 500 mA, 5.0 V / 200 mA Outputs
Application	Embedded Power Supply
Author	Applications Engineering Department
Document Number	RDR-736
Date	June 30, 2020
Revision	1.2

Summary and Features

- Highly integrated solution with 900 V rated power MOSFET
- Output voltage regulation: 12 V ±10%, 5 V ±5%
- Programmable current limit selection feature of LinkSwitch-XT2-900
- Extremely fast transient response independent of load timing
- >80% efficiency at full load condition
- <120 mW no-load input power at 230 VAC
- >6 dB conducted EMI margin
- No optocoupler or Zener diode required for regulation
- Can withstand up to 450 VAC line input

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This engineering report describes a non-isolated flyback converter designed to provide dual output of 5 V at 200 mA and 12 V at 500 mA from a wide input voltage range of 85 VAC to 440 VAC. This adapter utilizes the LNK3696P from the LinkSwitch-XT2 900 V family of devices.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

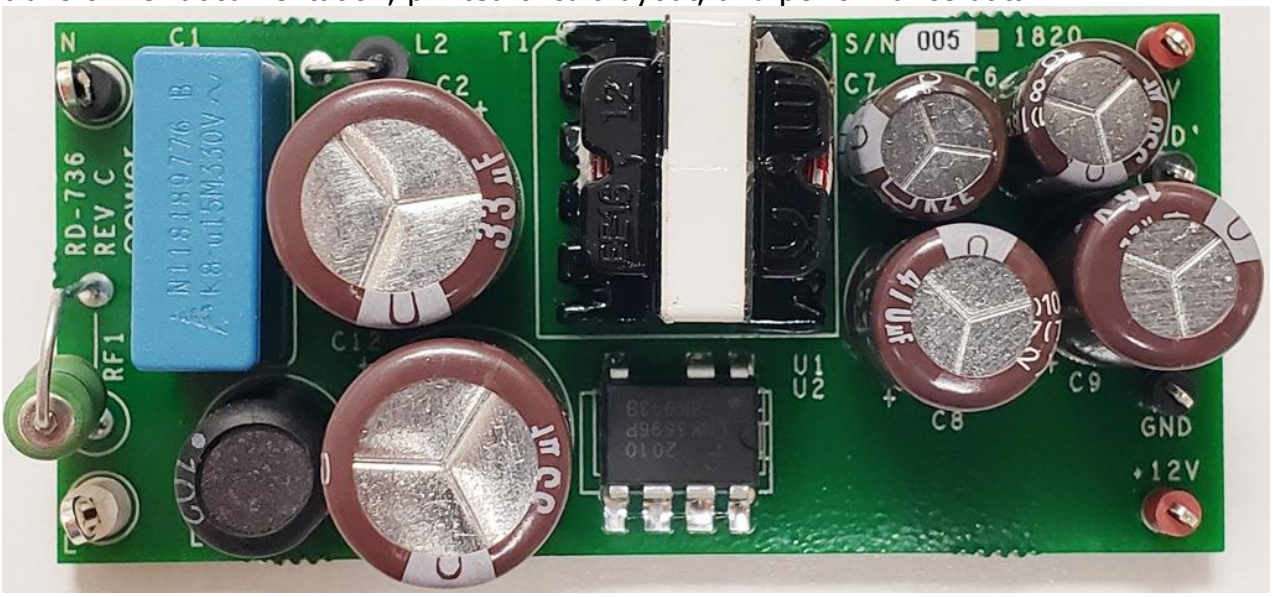

Figure 1 – Populated Circuit Board Photograph, Top.

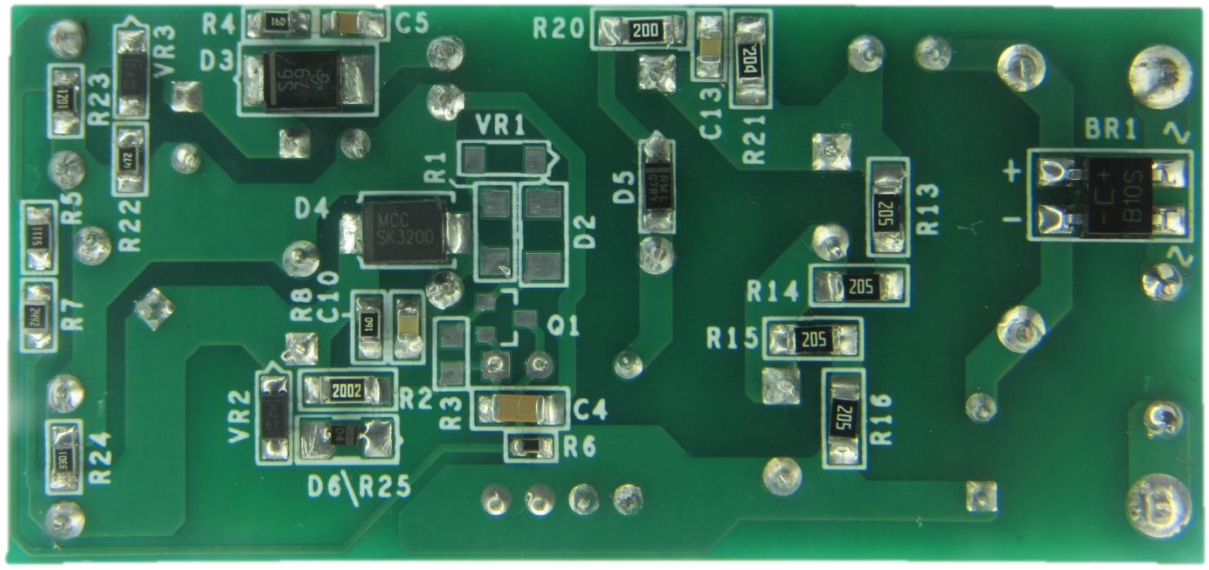

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		440	VAC	2 Wire – no P.E. Verified at 450 VAC.
Frequency	f_{LINE}	50	50/60	60	Hz	
No-load Input Power				200	mW	230 VAC.
Output						
Output Voltage 1	V_{OUT-5}	4.75	5.0	5.25	V	±5%
Output Current 1	I_{OUT-5}	50	200		mA	
Output Voltage 2	V_{OUT-12}	10.8	12.0	13.2	V	±10%
Output Current 2	I_{OUT-12}	50	500		mA	
Output Ripple Voltage	V_{RIPPLE}			200	mV	20 MHz Bandwidth.
Output Power	P_{OUT}		7		W	
Efficiency						
Full Load	$\eta_{Full-Load}$		80		%	Measured at Output Terminal.
Environmental						
Conducted EMI			CISPR22B / EN55022B Load floating			Resistive Load, 6 dB Margin.
Line Surge						
Differential Mode (L/N)				1	kV	Differential: 2 Ω
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level in Sealed Enclosure.

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3 Schematic

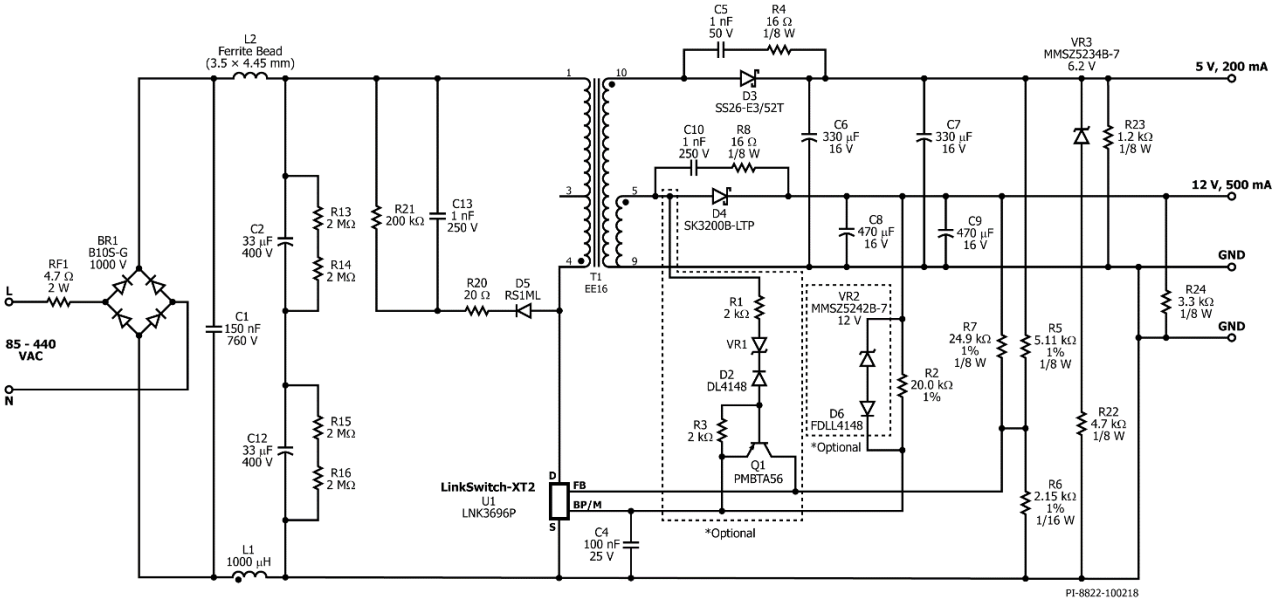

Figure 3 – Schematic.

4 Circuit Description

The LinkSwitch-XT2 900 V family of devices integrates a high-voltage (900 V rated) power MOSFET with an internal oscillator and ON/OFF controller inside a single monolithic IC. Unlike conventional pulse width modulation (PWM) controllers, LinkSwitch-XT2 900 V devices utilize a simple ON/OFF control scheme combined with an internal current limit circuitry to regulate the output voltage. The LNK3696P IC was used in a non-isolated flyback with dual output (12 V and 5 V) delivering 500 mA and 200 mA respectively.

4.1 Input Rectifier and Filter

The AC input is rectified by bridge rectifier BR1 and filtered by the bulk storage capacitors C2 and C3. Resistor RF1 is a flameproof, fusible, wire wound type and functions as a fuse, inrush current limiter and, together with the filter formed by C1, C2, C3, L1 and L2, differential mode noise attenuator. Resistors R13, R14, R15 and R16 function to balance the voltage between the bulk capacitors in series.

4.2 LinkSwitch-XT2 Primary-Side

The rectified and filtered input voltage is applied to the primary winding of flyback transformer T1. T1 is switched and connected to the IC via the DRAIN (D) pin. The D pin provides internal operating current for both start-up and steady-state operating conditions.

During the power MOSFET turn on time, current ramps up in the primary winding, storing energy inside the transformer core, while the two secondaries remain cut-off due to reverse biasing of the diodes. The primary winding current eventually exceeds the internal threshold (I_{LIMIT}), causing the power MOSFET to turn off for the remainder of the switching cycle. At the beginning of the next and all succeeding switching cycles, the IC decides whether to turn ON the power MOSFET or let it remain turned OFF. ON/OFF control is performed by comparing the output voltage to the reference voltage V_{FB}, resulting to the power MOSFET being enabled or disabled. Through the use of ON/OFF control, voltage regulation is maintained by skipping cycles without using an error amplifier and ramp generator, as in traditional power supply controllers.

4.3 Primary RCD Clamp

A low cost RCD clamp is connected across the primary winding of transformer T1. This is composed of resistors R20 and R13, capacitor C13 and diode D5. The clamp helps in dissipating the energy stored in the leakage inductance of T1.

4.4 Output Rectification

Transformer T1 has two secondary windings on its core – one for each output voltage. For both secondaries, the secondary switching voltage is rectified by Schottky diodes D3 and D4, and then filtered by super low ESR type capacitors C6, C7, C8 and C9. For each

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Schottky diode, a snubber network is connected in parallel using resistors R4 and R8, and capacitors C5 and C10. The snubber network helps limit the peak inverse voltage spikes seen by the diode. Pre-load resistors R23 and R23 are connected on each output to improve cross-regulation performance.

4.5 Output Feedback

The two outputs 12 V and 5 V are sensed through resistor dividers R5, R6 and R7. The sensed voltage is fed back to U1 through the FEEDBACK (FB) pin. This voltage V_{FB} must be accurately maintained at 2 V, so the sensing resistors must have 1% tolerance.

A weighted feedback circuit using resistors R5, R6 and R7 are connected to both output voltages and into the FB pin. The magnitude of the weights are determined by the relative contributions of current delivered into the FB pin, which then determine the values of R5 and R7. In the schematic, a larger current is contributed by the 5 V output, due to the larger current through R5 as compared to R7. Effectively, the 5 V output voltage has better feedback sensitivity and output regulation.

4.6 Output Overvoltage Protection

The BYPASS (BP/M) pin has multiple functions: it provides a connection point for an external bypass capacitor as well current limit value selector via the capacitance value, and it provides a shutdown function. Similar to the FB pin, when the current delivered into the BP/M pin exceeds the internal threshold ($I_{BP(SD)}$) for a time equal to 2 to 3 cycles of the switching frequency, the device enters auto-restart. By designing a circuit that injects current into the BP/M pin due to a fault, the device can be equipped with both output overvoltage and line overvoltage protection.

For the 5 V output, a simple clamp circuit using Zener diode VR3 and resistor R22 is used for overvoltage protection. For the 12 V output, Zener diode VR2, diode D6 and resistor R7 comprise the overvoltage protection circuit. A voltage at the 12 V output the exceeds the sum of the VR2 voltage rating, D2 diode drop, and the bypass voltage will cause a current in excess of $I_{BP(SD)}$ to be injected into the BP/M pin, which will trigger the auto-restart and protect the power supply from overvoltage.

4.7 Line Overvoltage Protection

The device indirectly senses the DC bus voltage by sampling the secondary voltage during the power MOSFET on-time. During this time, the voltage across the secondary winding is proportional to the voltage across the primary winding. When the DC bus voltage exceeds the limit, Zener diode VR1 and diode D2 are turned on causing current to flow through transistor Q1 and into the FB pin. The device will go into auto-restart mode if the FB pin current limit is exceeded for at least 2 consecutive switching cycles.

5 PCB Layout

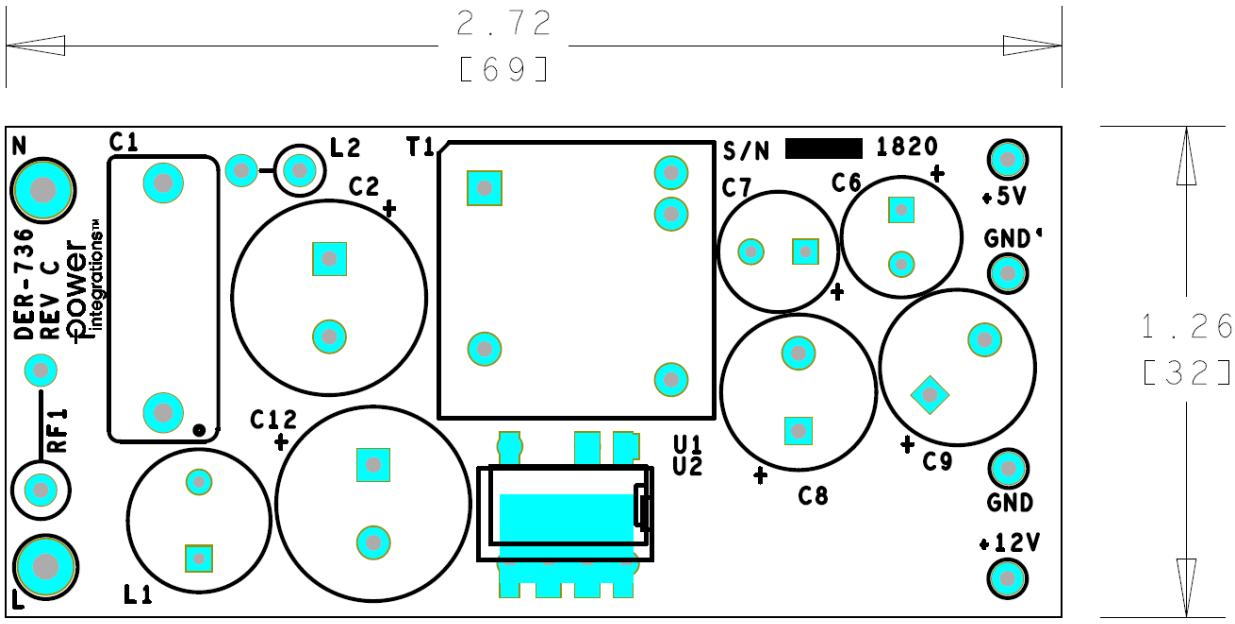

Figure 4 – Printed Circuit Layout, Top.

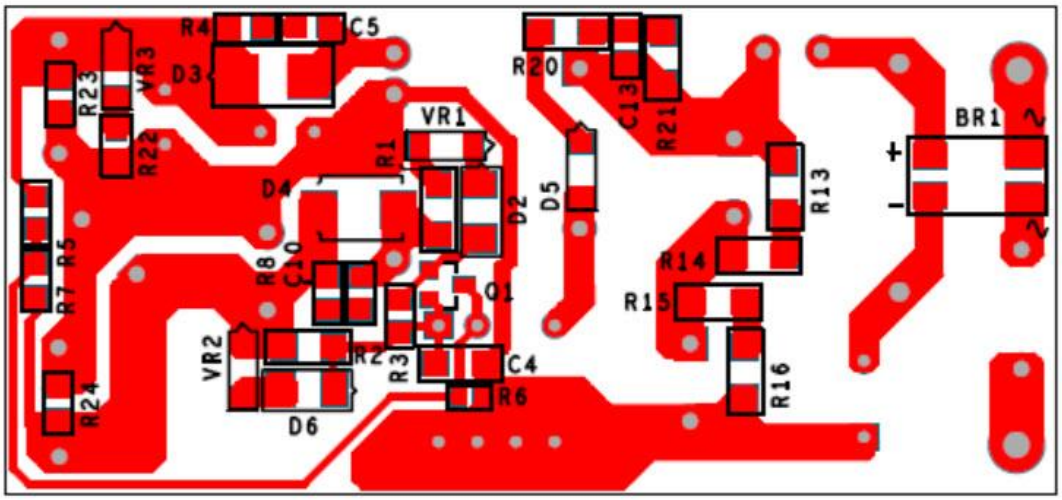

Figure 5 – Printed Circuit Layout, Bottom.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	1	C1	150 nF, 760 V, Polypropylene Film	B32912B3154M	Epcos
3	2	C2 C12	33 μF, 400 V, Electrolytic, (12.5 x 20)	KMG401ELL330MK20S	Nippon Chemi-Con
4	1	C4	100 nF, 25 V, Ceramic, X7R, 1206	C1206F104K3RACTU	Kemet
5	1	C5	1 nF, 50 V, Ceramic, X7R, 0805	08055C102KAT2A	AVX
6	2	C6 C7	330 μF, 16 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	EKZE160ELL331MHB5D	Nippon Chemi-Con
7	2	C8 C9	470 μF, 16 V, Electrolytic, Very Low ESR, 53 mΩ, (10 x 12.5)	EKZE160ELL471MJC5S	Nippon Chemi-Con
8	2	C10 C13	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01D	Murata
9	1	D3	60 V, 2 A, Schottky, SMD, DO-214AA	SS26-E3/52T	Vishay
10	1	D4	200 V, 3 A, DIODE SCHOTTKY 1A 200 V, SMB	SK3200B-LTP	Micro Commercial
11	1	D5	1000 V, 800 mA, Fast Recovery SMF, 5000 ns,	RS1ML	Taiwan Semi
12	1	D6	100 V, 10 mA, Fast Switching, 4 ns, MINI-MELF, SOD-80	FDLL4148	ON Semi
13	1	L1	1000 μH, 0.510 A	RLB9012-102KL	Bourns
14	1	L2	3.5 mm x 4.45 mm, 56 Ω at 100 MHz, #22 AWG hole, Ferrite Bead	2761001112	Fair-Rite
15	1	R2	RES, 20.0 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2002V	Panasonic
16	2	R4 R8	RES, 16 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ160V	Panasonic
17	1	R5	RES, 5.11 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5111V	Panasonic
18	1	R6	RES, 2.15 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2151V	Panasonic
19	1	R7	RES, 24.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2492V	Panasonic
20	4	R13 R14 R15 R16	RES, 2 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ205 V	Panasonic
21	1	R20	RES, 20 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ200V	Panasonic
22	1	R21	RES, 200 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
23	1	R22	RES, 4.7 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ472V	Panasonic
24	1	R23	RES, 1.2 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ122V	Panasonic
25	1	R24	RES, 3.3 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ332V	Panasonic
26	1	RF1	RES, 4.7 Ω, 2 W, Flame Proof, Pulse Withstanding, Wire Wound	FW20A4R70JA	Bourns.
27	1	T1	Bobbin, EE16, Vertical, 10 pins (4 x 6)	EL-16 (YW-193-02B)	Yih-Hwa
28	1	U1	LinkSwitch-XT2-900, DIP-8C	LNK3696P	Power Integrations
39	1	VR2	DIODE ZENER 12 V 500 mW SOD123	MMSZ5242B-7-F	Diodes, Inc.
30	1	VR3	DIODE ZENER 6.2 V 500 mW SOD123	MMSZ5234B-7-F	Diodes, Inc.

Miscellaneous Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	GND GND`	Test Point, BLK,Miniature THRU-HOLE MOUNT	5001	Keystone
2	2	+5V, +12V	Test Point, RED,Miniature THRU-HOLE MOUNT	5000	Keystone
3	1	L	Test Point, WHT,THRU-HOLE MOUNT	5012	Keystone
4	1	N	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone

7 Transformer Specification

7.1 Electrical Diagram

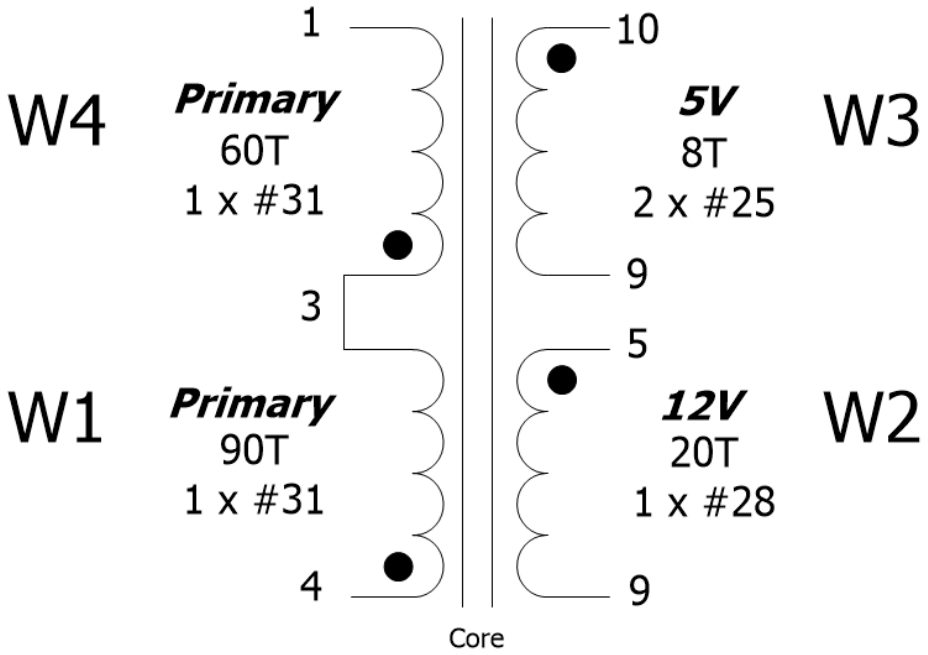

Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec
Electrical Strength	60 Hz, 1 second, from pins 1-4 to pins 9-10	3000 VAC
Primary Inductance	Pins 1-4, all other windings open, measured at 100 kHz, 0.4 V_{RMS}.	1500 µH ±7%
Primary Leakage Inductance	Pins 1-4, all other windings short, measured at 100 kHz, 0.4 V_{RMS}.	<100 µH

7.3 Material List

Item	Description
[1]	Core: EE16, Gapped.
[2]	Bobbin: EE16, Vertical, 10 pins.
[3]	Magnet Wire: #31 AWG.
[4]	Magnet Wire: #28 AWG.
[5]	Magnet Wire: #25 AWG.
[6]	Tape, 3M 1298 Polyester Film, 2.0 Mils Thick, 8.4 mm Wide.
[7]	Tape, 3M 1298 Polyester Film, 2.0 Mils Thick, 4.5 mm Wide.
[8]	Varnish.

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7.4 Transformer Build Diagram

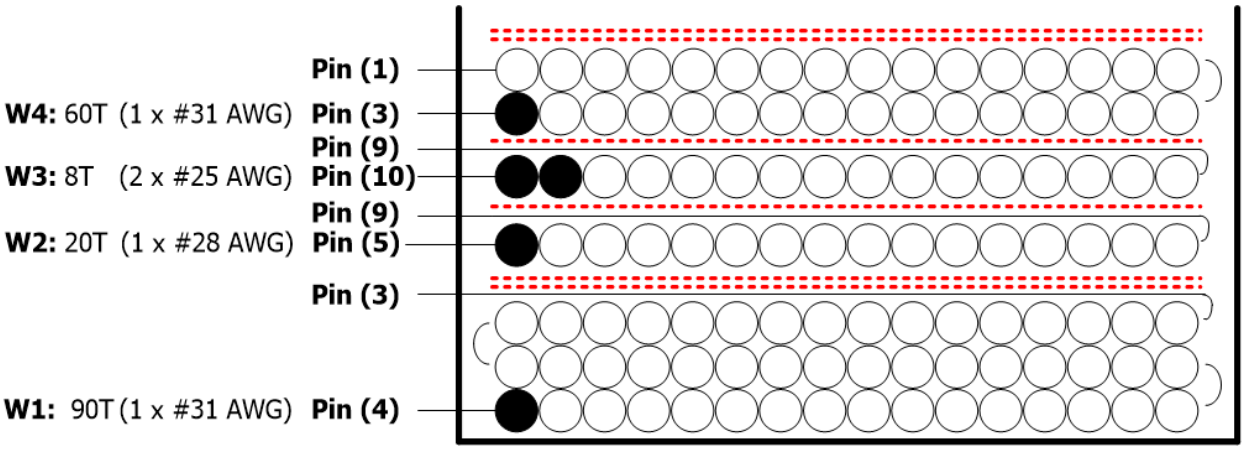
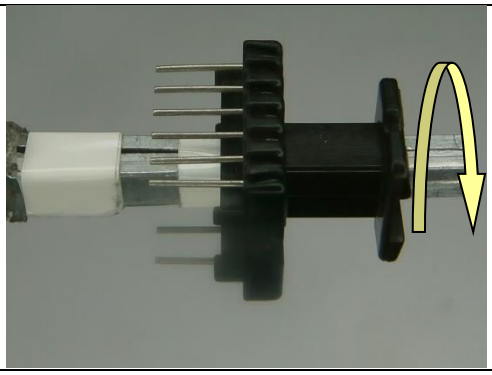


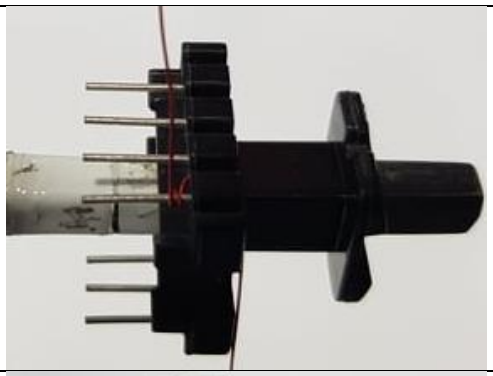
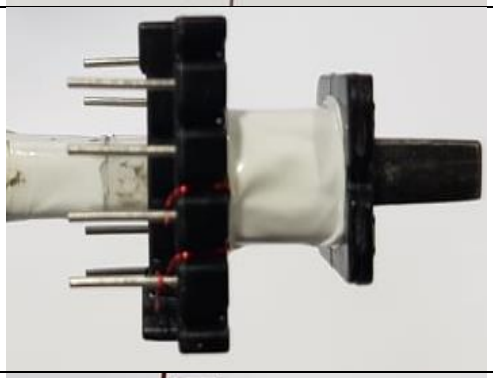
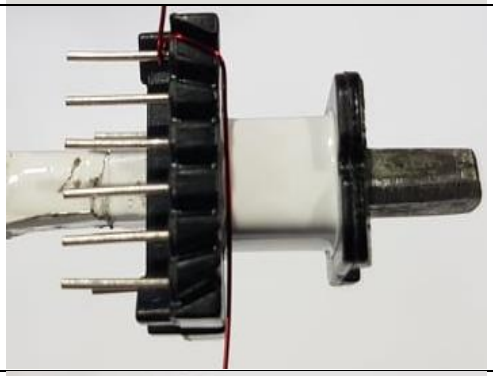
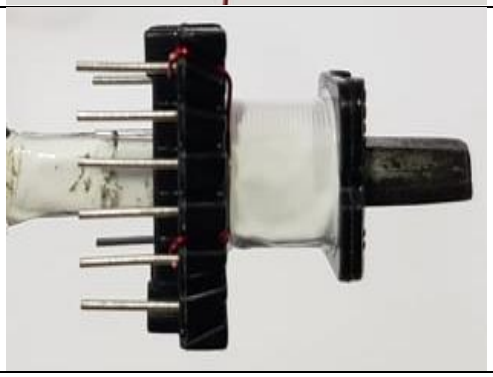
Figure 7 – Transformer Build Diagram.

7.5 Transformer Construction

Winding preparation	Place the bobbin Item [2] such that the pins are facing the winder. Winding direction is counter-clockwise as shown.
W1 1st Primary	Starting at pin 4, wind 90 turns of wire Item [3] in three layers. At the last turn, bring the wire back across the windings and into pin 3.
Insulation	Apply two layers of tape Item [6] for insulation.
W2 12V Winding	Start at pin 5, wind 20 turns of wire Item [4] in one layer. At the last turn, bring the wire back across the windings and into pin 9.
Insulation	Use 1 layer of tape Item [6] for insulation.
W3 5V Winding	Starting at pin 10, wind 7.7 turns of two strands of wire Item [5] in one layer. At the last turn, bring the wire back across the windings and into pin 9.
Insulation	Use 1 layer of tape Item [6] for insulation.
W4 2nd Primary	Continue the primary winding at pin 3. Wind 60 turns of wire Item [3] in two layers. Finish at pin 1.
Insulation	Apply two layers of tape Item [6] for insulation.
Assembly	Grind core halves for specified primary inductance, insert bobbin, and secure core halves with tape Item [7]. Cut pin 3 short. Remove pins 2, 6, 7 and 8. Dip varnish.

7.6 Transformer Winding Illustrations

Winding preparation		Place the bobbin Item [2] such that the pins are facing the winder. Winding direction is counter-clockwise as shown.

W1 **1st Primary**		Starting at pin 4, wind 90 turns of wire Item [3] in three layers. At the last turn, bring the wire back across the windings and into pin 3.
Insulation		Apply two layers of tape Item [6] for insulation.
W2 **12V Winding**		Start at pin 5, wind 20 turns of wire Item [4] in one layer. At the last turn, bring the wire back across the windings and into pin 9.
Insulation		Use 1 layer of tape Item [6] for insulation.

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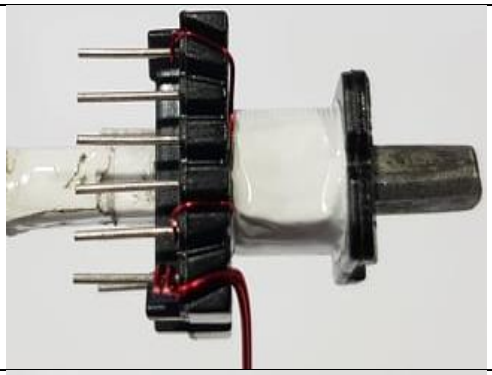
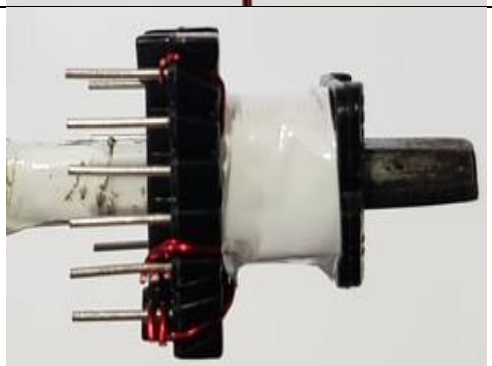
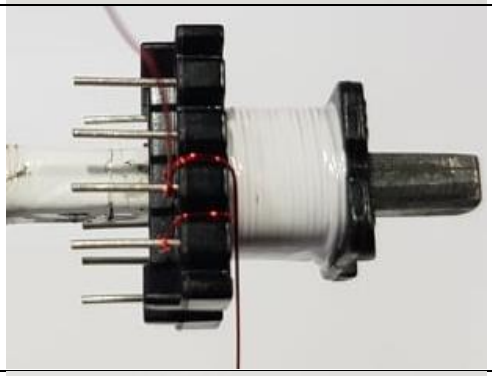
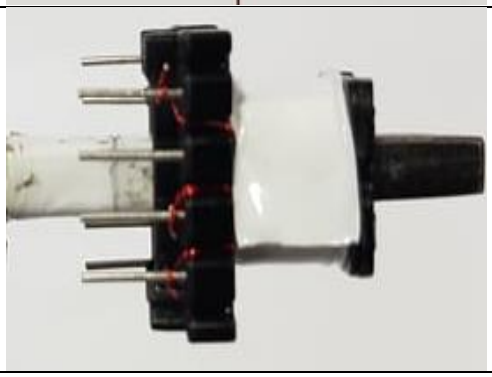
W3 **5V Winding**		Starting at pin 10, wind 8 turns of two strands of wire Item [5] in one layer. At the last turn, bring the wire back across the windings and into pin 9.
Insulation		Use 1 layer of tape Item [6] for insulation.
W4 **2nd Primary**		Continue the primary winding at pin 3. Wind 60 turns of wire Item [3] in two layers. Finish at pin 1.
Insulation		Apply two layers of tape Item [6] for insulation.

Assembly	 	Grind core halves for specified primary inductance, insert bobbin, and secure core halves with tape Item [7]. Cut pin 3 short. Remove pins 2, 6, 7 and 8. Dip varnish.

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8 Transformer Design Spreadsheet

Note: The output current entered in the spreadsheet was increased such that POUT matches the combined power of the dual outputs.

ACDC_LinkSwitchXT2900V_092018; Rev.1.1; Copyright Power Integrations 2018	***INPUT***	***INFO***	***OUTPUT***	***UNIT***	***ACDC_LinkSwitchXT2 900V Flyback Design Spreadsheet***
ENTER APPLICATION VARIABLES					
LINE VOLTAGE RANGE			UNIVERSAL		AC line voltage range
VACMIN	85.00		85.00	Volts	Minimum AC line voltage
VACTYP	115.00		115.00	Volts	Typical AC line voltage
VACMAX	440.00		440.00	Volts	Maximum AC line voltage
fL			50	Hertz	AC mains frequency
TIME_BRIDGE_CONDUCTION			2.87	mseconds	Input bridge rectifier diode conduction time
LINE RECTIFICATION			F		Select 'F'ull wave rectification or 'H'alf wave rectification
VOUT	12.00		12.00	Volts	Output voltage
IOUT	0.600		0.600	Amperes	Average output current specification
EFFICIENCY	0.80		0.80		Efficiency Estimate at output terminals. Under 0.8 if no better data available
LOSS ALLOCATION FACTOR			0.50		The ratio of power losses during the MOSFET off-state to the total system losses
POUT			7.20	Watts	Continuous Output Power
CIN	16.50		16.50	uFarads	Input capacitor
VMIN			79.59	Volts	Valley of the rectified VACMIN
VMAX			622.25	Volts	Peak of the VACMAX
FEEDBACK	MAIN		MAIN		Select the type of feedback required. (MAIN = feedback via Main Output - Non-isolated)
BIAS WINDING			NO		Select whether a bias winding is required
LINKSWITCH-XT2 VARIABLES					
CURRENT LIMIT MODE			STD		Pick between 'RED' (Reduced) or 'STD' (Standard) current limit mode of operation
PACKAGE			DIP-8C		Device package
ENCLOSURE			OPEN FRAME		Device enclosure
GENERIC DEVICE	LNK3696		LNK3696		Device series
DEVICE CODE			LNK3696P		Device code
PMAX			8.00	Watts	Device maximum power capability
VOR	95		95	Volts	Voltage reflected to the primary winding when the MOSFET is off
VDSON			10.0	Volts	MOSFET on-time drain to source peak voltage
VDSOFF			841.8	Volts	The off-time drain to source voltage is higher than 90% of the device breakdown voltage (900V)
ILIMITMIN			0.446	Amperes	Minimum current limit
ILIMITTYP			0.482	Amperes	Typical current limit
ILIMITMAX			0.518	Amperes	Maximum current limit
FSMIN			62000	Hertz	Minimum switching frequency
FSTYP			66000	Hertz	Typical switching frequency
FSMAX			70000	Hertz	Maximum switching frequency
RDSON			9.70	Ohms	MOSFET drain to source resistance at 25degC
PRIMARY WAVEFORM PARAMETERS					
MODE OF OPERATION			CCM		Mode of operation
KRP/KDP			0.995		Measure of continuous/discontinuous

					mode of operation
KP_TRANSIENT			0.698		KP under conditions of a transient
DMAX			0.577		Maximum duty cycle at VMIN
TIME_ON			9.310	useconds	MOSFET conduction time at the minimum line voltage
TIME_ON_MIN			1.076	useconds	MOSFET conduction time at the maximum line voltage
IAVG_PRIMARY			0.129	Amperes	Average input current
IRMS_PRIMARY			0.196	Amperes	Root mean squared value of the primary current
LPRIMARY_MIN			1314	uH	Minimum primary inductance
LPRIMARY_TYP			1460	uH	Typical primary inductance
LPRIMARY_MAX			1606	uH	Maximum primary inductance
LPRIMARY_TOL			10		Tolerance of the Primary inductance
SECONDARY WAVEFORM PARAMETERS					
IPEAK_SECONDARY			3.885	Amperes	Peak secondary current
IRMS_SECONDARY			1.462	Amperes	Root mean squared value of the secondary current
PIV_SECONDARY			94.97	Volts	Peak inverse voltage on the secondary diode, not including the leakage spike
VF_SECONDARY			0.70	Volts	Secondary diode forward voltage drop
TRANSFORMER CONSTRUCTION PARAMETERS					
Core selection					
CORE	EE16		EE16		Select the transformer core
BOBBIN			B-EE16-H		Bobbin name
AE			19.20	mm^2	Cross sectional area of the core
LE			35.00	mm	Effective magnetic path length of the core
AL			1140.0	nH/(turns^2)	Ungapped effective inductance of the core
VE			795.0	mm^3	Volume of the core
AW			14.76	mm^2	Window area of the bobbin
BW			8.50	mm	Width of the bobbin
MLT			0.00	mm	Mean length per turn of the bobbin
MARGIN			0.00	mm	Safety margin
Primary winding					
NPRIMARY			150		PrImary number of turns
BMAX_TARGET			1500	Gauss	Target value of the magnetic flux density
BMAX_ACTUAL			2625	Gauss	The actual flux density of the device has been exceeded
BAC			1306	Gauss	AC flux density
ALG			65	nH/T^2	Gapped core effective inductance
LG			0.351	mm	Core gap length
LAYERS_PRIMARY			4		Number of primary layers
AWG_PRIMARY			33		Primary winding wire AWG
OD_PRIMARY_INSULATED			0.219	mm	Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE			0.180	mm	Primary winding wire outer diameter without insulation
CMA_PRIMARY			256	mil^2/Amperes	Primary winding wire CMA
Secondary winding					
NSECONDARY	20		20		Secondary turns
AWG_SECONDARY			25		Secondary winding wire AWG
OD_SECONDARY_INSULATED			0.760	mm	Secondary winding wire outer diameter with insulation
OD_SECONDARY_BARE			0.455	mm	Secondary winding wire outer diameter without insulation
CMA_SECONDARY			219	mil^2/Amperes	Secondary winding CMA
Bias winding					

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NBIAS			N/A		Bias turns
VF_BIAS			N/A	Volts	Bias diode forward voltage drop
VBIAS			N/A	Volts	Bias winding voltage
PIVB			N/A	Volts	Peak inverse voltage on the bias diode
CBP			0.1	uF	BP pin capacitor
FEEDBACK PARAMETERS					
DIODE_BIAS			1N4003-4007		Recommended diode is 1N4003. Place diode on return leg of bias winding for optimal EMI
RUPPER			15000	ohms	CV bias resistor for CV/CC circuit. See LinkSwitch-XT2 Design Guide
RLOWER			3000	ohms	Resistor to set CC linearity for CV/CC circuit. See LinkSwitch-XT2 900V Design Guide
MULTIPLE OUTPUT PARAMETERS					
Output 1					
VOUT1			12.00	Volts	Output Voltage 1
IOUT1			0.600	Amperes	Output Current 1
POUT1			7.20	Watts	Output Power 1
VD1			0.70	Volts	Secondary diode forward voltage drop for output 1
NS1			20		Number of turns for output 1
ISRMS1			1.462	Amperes	Root mean squared value of the secondary current for output 1
IRIPPLE1			1.333	Amperes	Current ripple on the secondary waveform for output 1
PIV1			94.97	Volts	Peak inverse voltage on the secondary diode for output 1
DIODE1_RECOMMENDED			BYV27-200		Recommended diode for output 1
PRELOAD			6.04	kohms	Preload resistor to ensure a load of at least 3mA on the first output for BIAS, 2mA for MAIN
CMS1			292.4	Cmils	Bare conductor effective area in circular mils for output 1
AWGS1			25	AWG	Wire size for output 1
Output 2					
VOUT2	5.00		5.00	Volts	Output Voltage 2
IOUT2	0.200		0.200	Amperes	Output Current 2
POUT2			1.00	Watts	Output Power 2
VD2			0.70	Volts	Secondary diode forward voltage drop for output 2
NS2			9		Number of turns for output 2
ISRMS2			0.487	Amperes	Root mean squared value of the secondary current for output 2
IRIPPLE2			0.444	Amperes	Current ripple on the secondary waveform for output 2
PIV2			42.34	Volts	Peak inverse voltage on the secondary diode for output 2
DIODE2_RECOMMENDED			SB160		Recommended diode for output 2
CMS2			97.5	Cmils	Bare conductor effective area in circular mils for output 2
AWGS2			30	AWG	Wire size for output 2
Output 3					
VOUT3			0.00	Volts	Output Voltage 3
IOUT3			0.000	Amperes	Output Current 3
POUT3			0.00	Watts	Output Power 3
VD3			0.70	Volts	Secondary diode forward voltage drop for output 3
NS3			2		Number of turns for output 3
ISRMS3			0.000	Amperes	Root mean squared value of the secondary current for output 3
IRIPPLE3			0.000	Amperes	Current ripple on the secondary

					waveform for output 3
PIV3			8.30	Volts	Peak inverse voltage on the secondary diode for output 3
DIODE3_RECOMMENDED			NA		Recommended diode for output 3
CMS3			0.0	Cmils	Bare conductor effective area in circular mils for output 3
AWGS3			0	AWG	Wire size output for 3
PO_TOTAL			8.20	Watts	The total power of all outputs exceeds the design power
NEGATIVE OUTPUT			N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

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9 Performance Data

9.1 No-Load Input Power

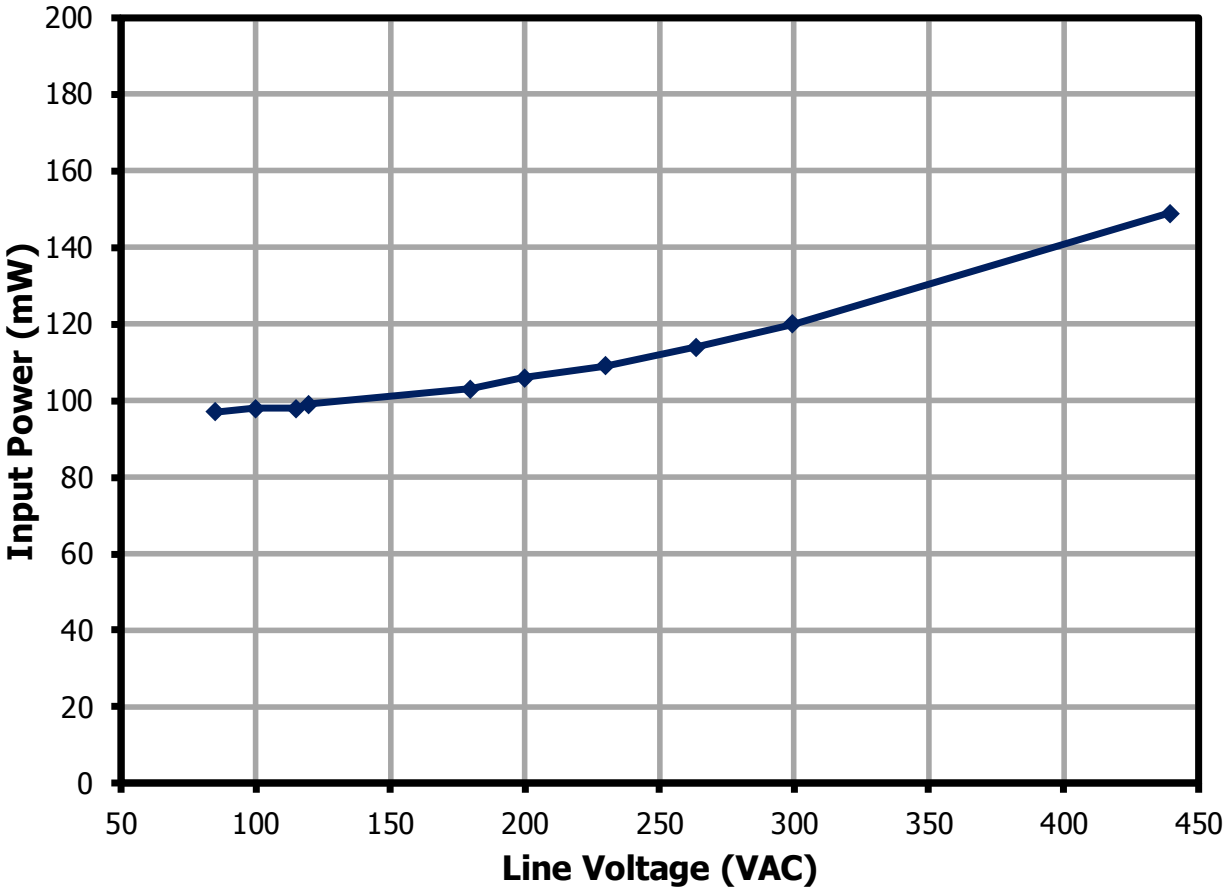

Figure 8 – No-Load Power vs. Input Line Voltage.

9.2 **Efficiency**

9.2.1 *Efficiency vs Line*

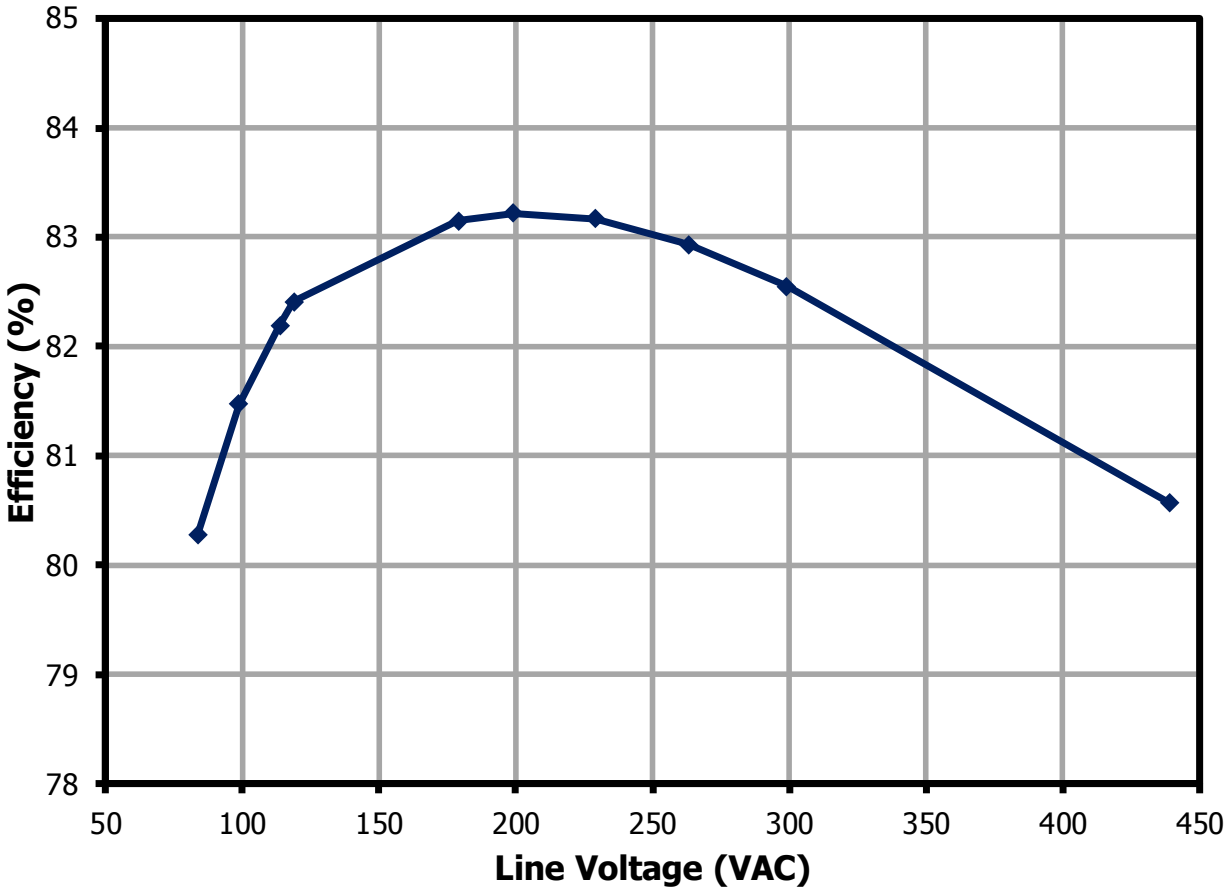

Figure 9 – Full Load Efficiency vs. Input Line Voltage.

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9.2.2 *Efficiency vs Load*

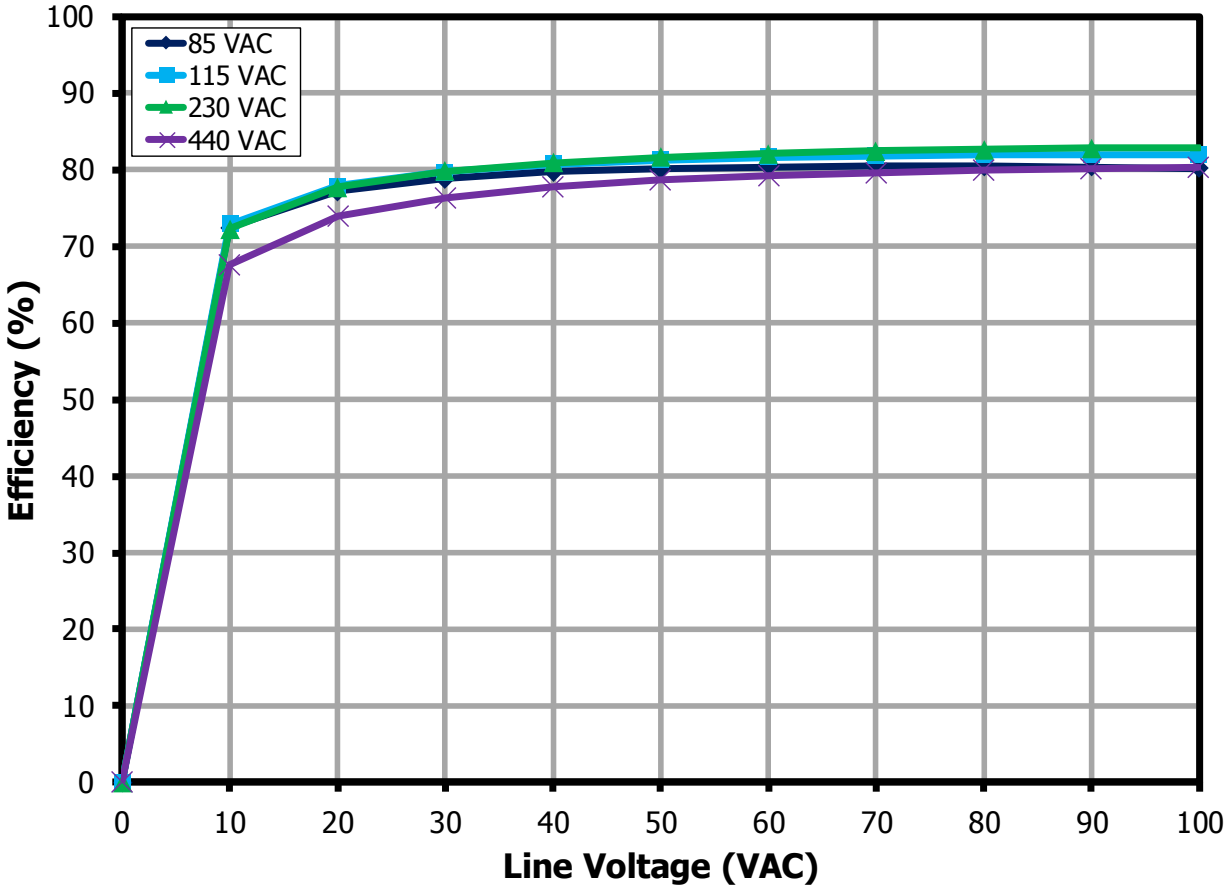

Figure 10 – Efficiency vs. Percent Load, at Different Input Line Voltages.

9.2.3 *Average Efficiency*

9.2.3.1 85 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
83	163.1	8.71	12.01	500.0	6.01	4.94	198.1	0.98	80.2
84	124.1	6.52	12.02	375.0	4.51	4.95	148.0	0.73	80.4
84	85.8	4.36	12.04	249.9	3.01	4.95	98.2	0.49	80.1
84	46.8	2.23	12.06	145.0	1.51	4.95	48.2	0.24	78.2
						Average Efficiency			**79.7**

9.2.3.2 115 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
114	123.2	8.52	12.01	500.0	6.00	4.94	198.1	0.98	82.0
114	95.0	6.40	12.03	375.0	4.51	4.95	148.0	0.73	81.9
114	66.4	4.30	12.04	250.0	3.01	4.95	98.1	0.49	81.2
114	36.6	2.21	12.07	125.0	1.51	4.95	48.2	0.24	79.1
						Average Efficiency			**81.0**

9.2.3.3 230 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
229	72.1	8.43	12.03	500.0	6.02	4.94	198.0	0.98	83.0
229	56.1	6.36	12.04	374.9	4.52	4.94	148.1	0.73	82.5
229	39.5	4.29	12.06	249.9	3.01	4.95	98.1	0.49	81.6
230	22.0	2.21	12.08	125.0	1.51	4.95	48.2	0.24	78.9
						Average Efficiency			**81.5**

9.2.3.4 440 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
439	45.0	8.70	12.03	500.0	6.02	4.94	197.9	0.98	80.4
439	35.1	6.57	12.03	375.0	4.51	4.95	148.0	0.73	79.8
439	24.9	4.45	12.05	249.9	3.01	4.95	98.2	0.49	78.7
439	14.0	2.32	12.08	125.0	1.51	4.95	48.1	0.24	75.4
						Average Efficiency			**78.6**

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9.3 Output Voltage Regulation

9.3.1 *5 V Load Regulation with Balanced Load*

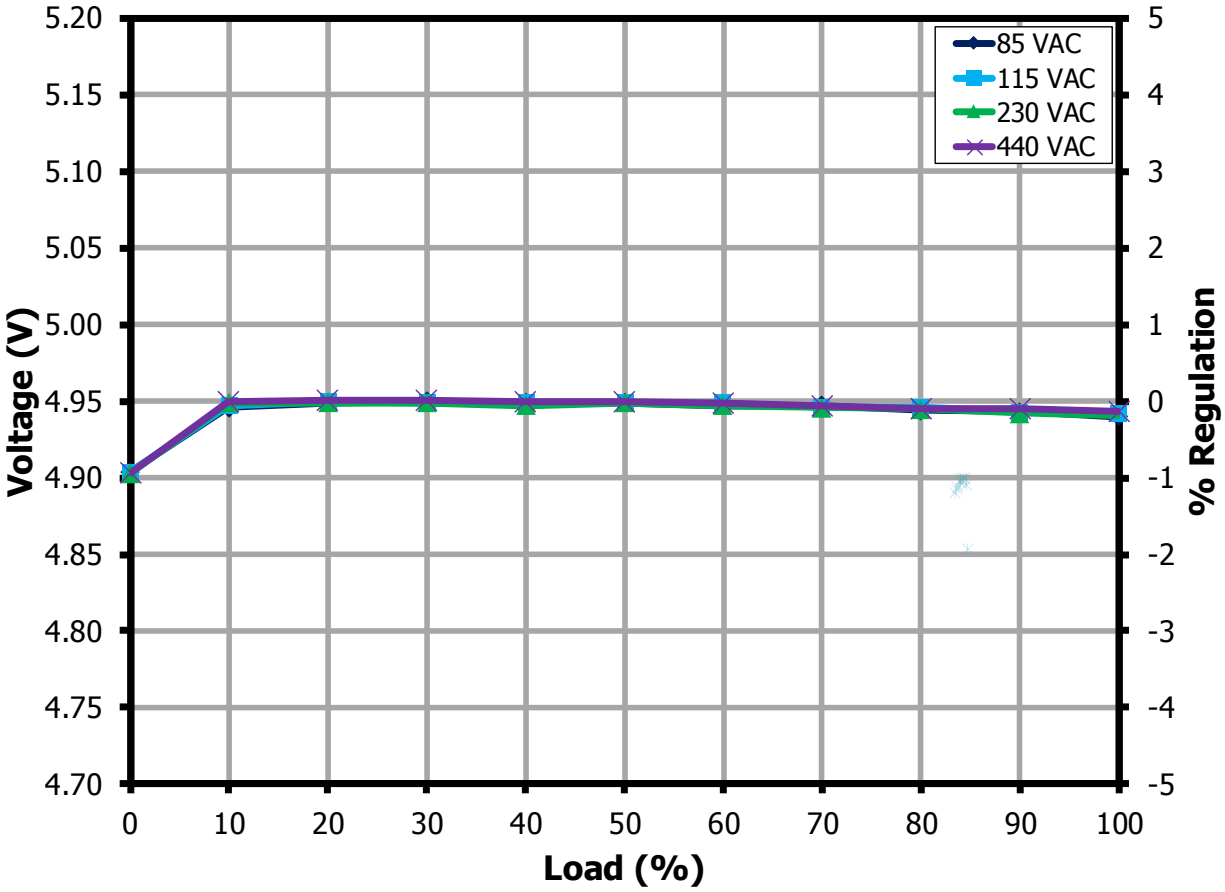

Figure 11 – 5 V Load Regulation.
Condition: Simultaneous Load Decrement.

9.3.2 *12 V Load Regulation with Balanced Load*

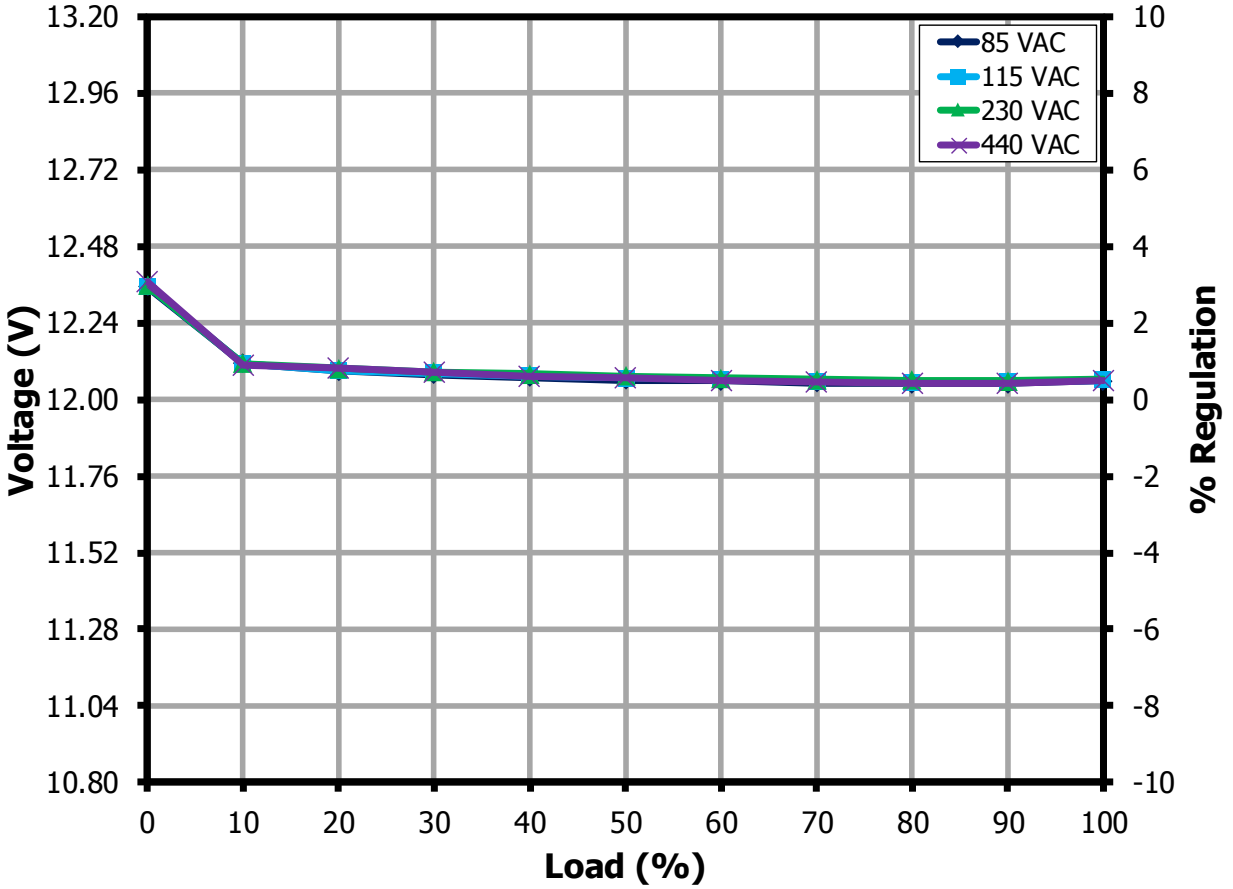

Figure 12 – 12 V Load Regulation.
Condition: Simultaneous Load Decrement.

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9.3.3 *5 V Load Regulation with Unbalanced Load*

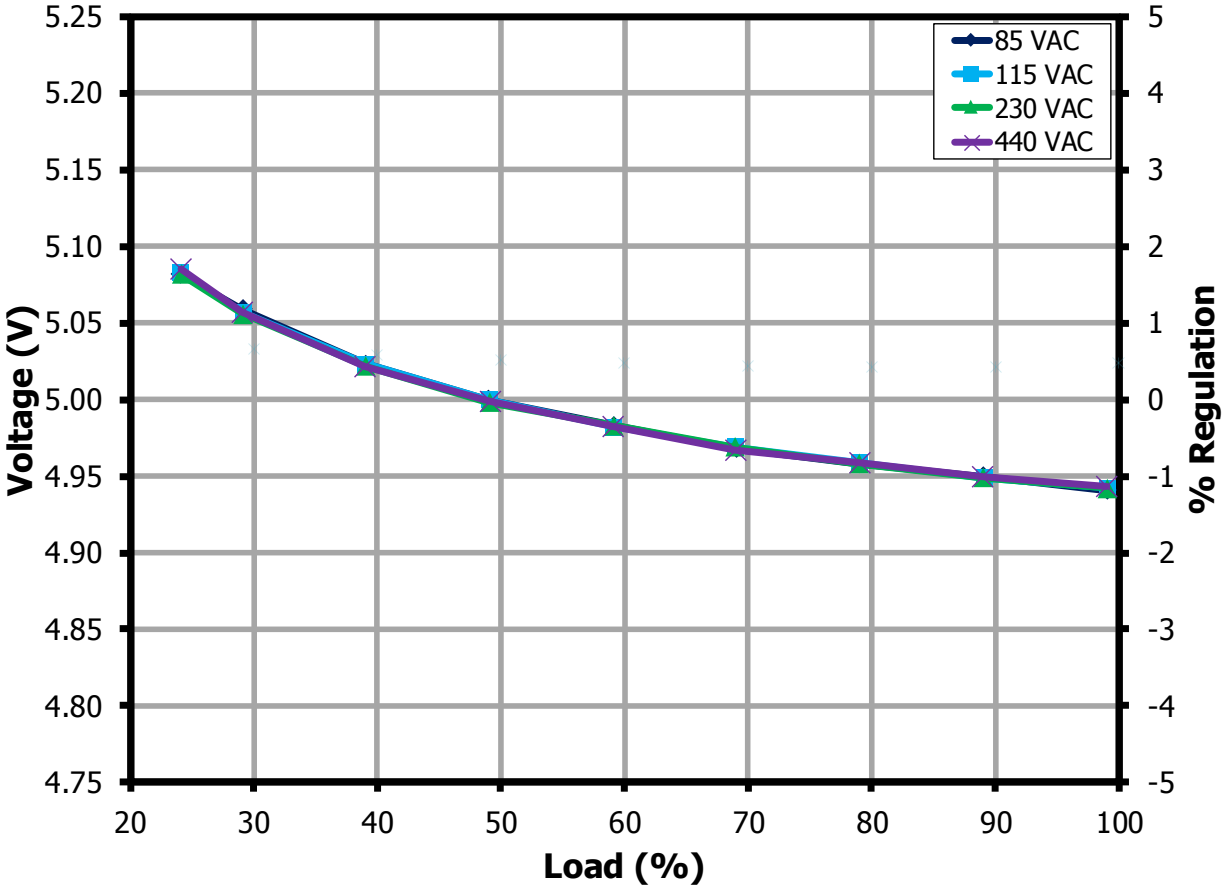

Figure 13 – 5 V Load Regulation.
Condition: 12 V at 500 mA, 5 V Load Sweep.

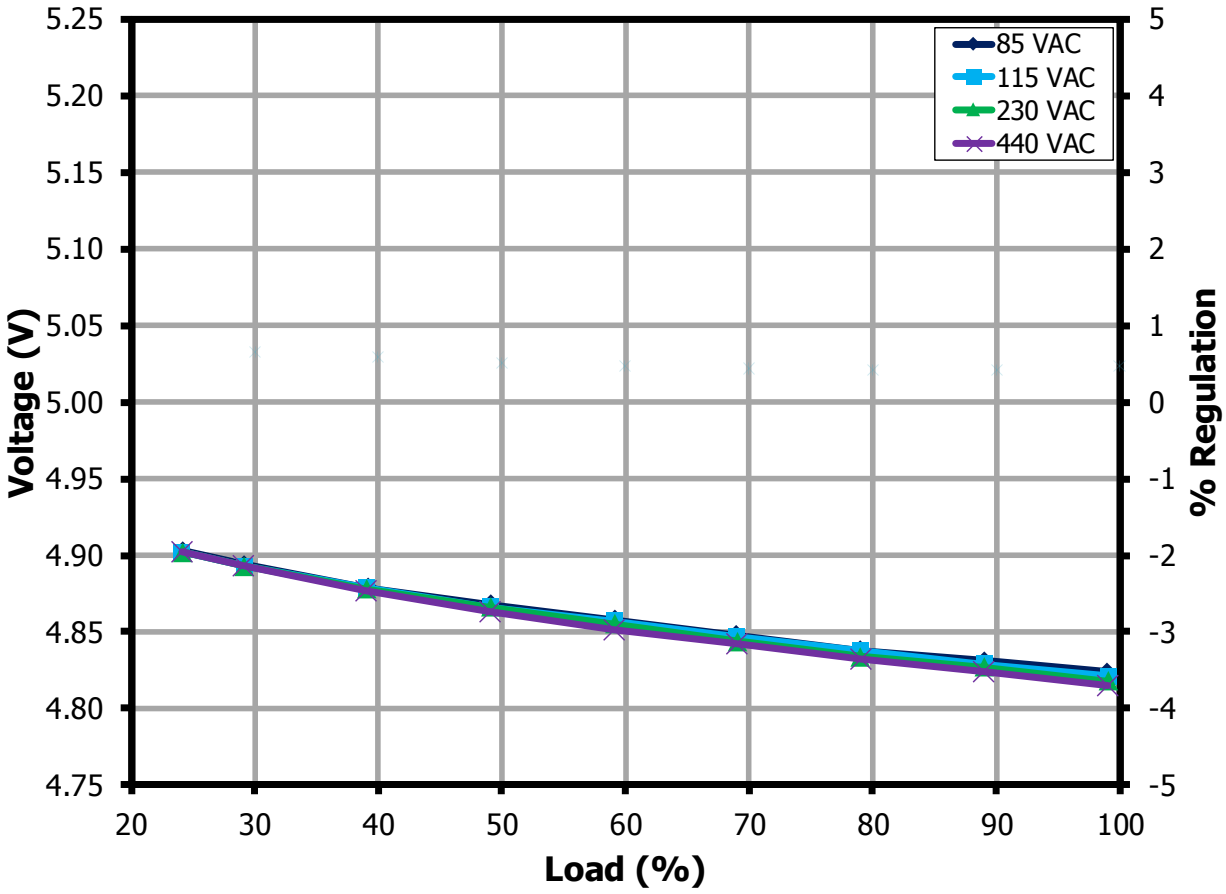

Figure 14 – 5 V Load Regulation.
Condition: 12 V at 50 mA, 5 V Load Sweep.

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9.3.4 *12 V Load Regulation with Unbalanced Load*

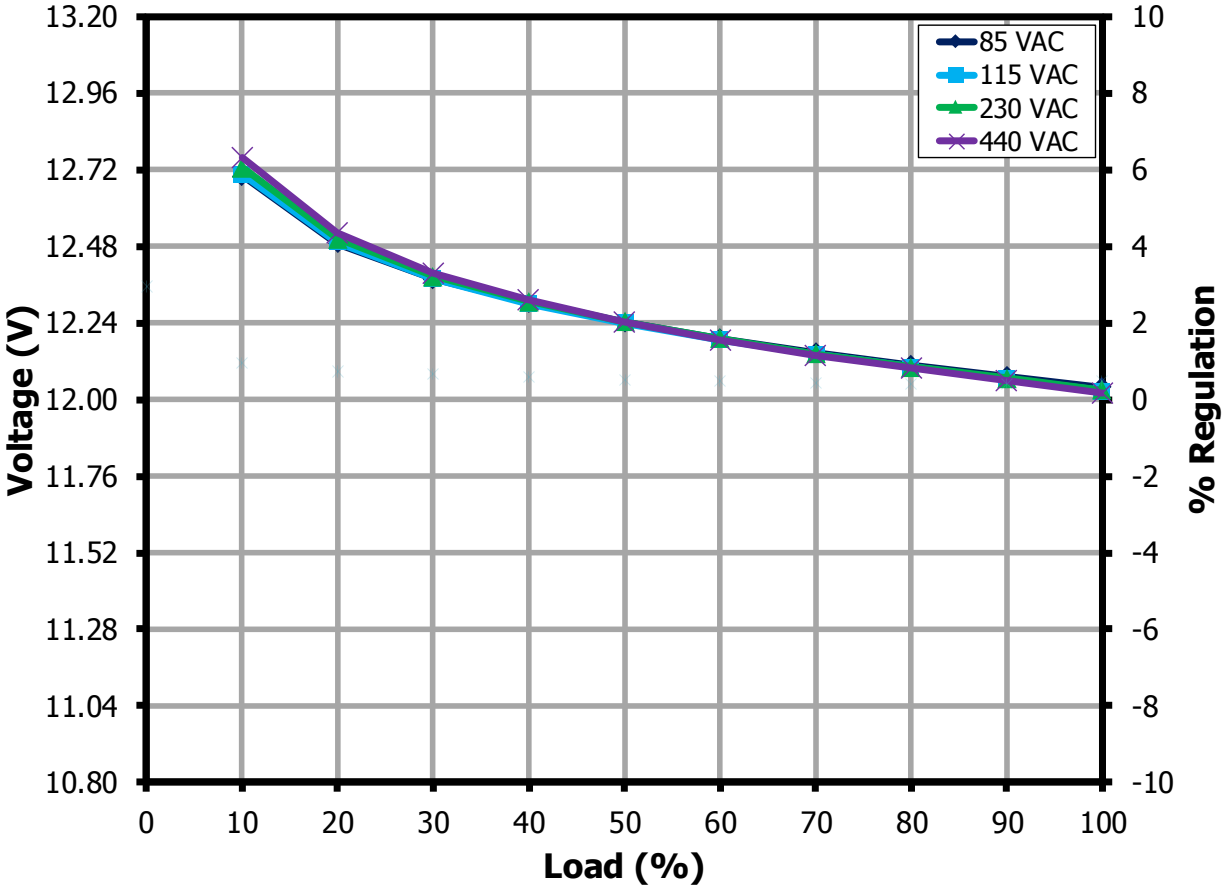

Figure 15 – 12 V Load Regulation.
Condition: 12 V Load Sweep, 5 V at 200 mA.

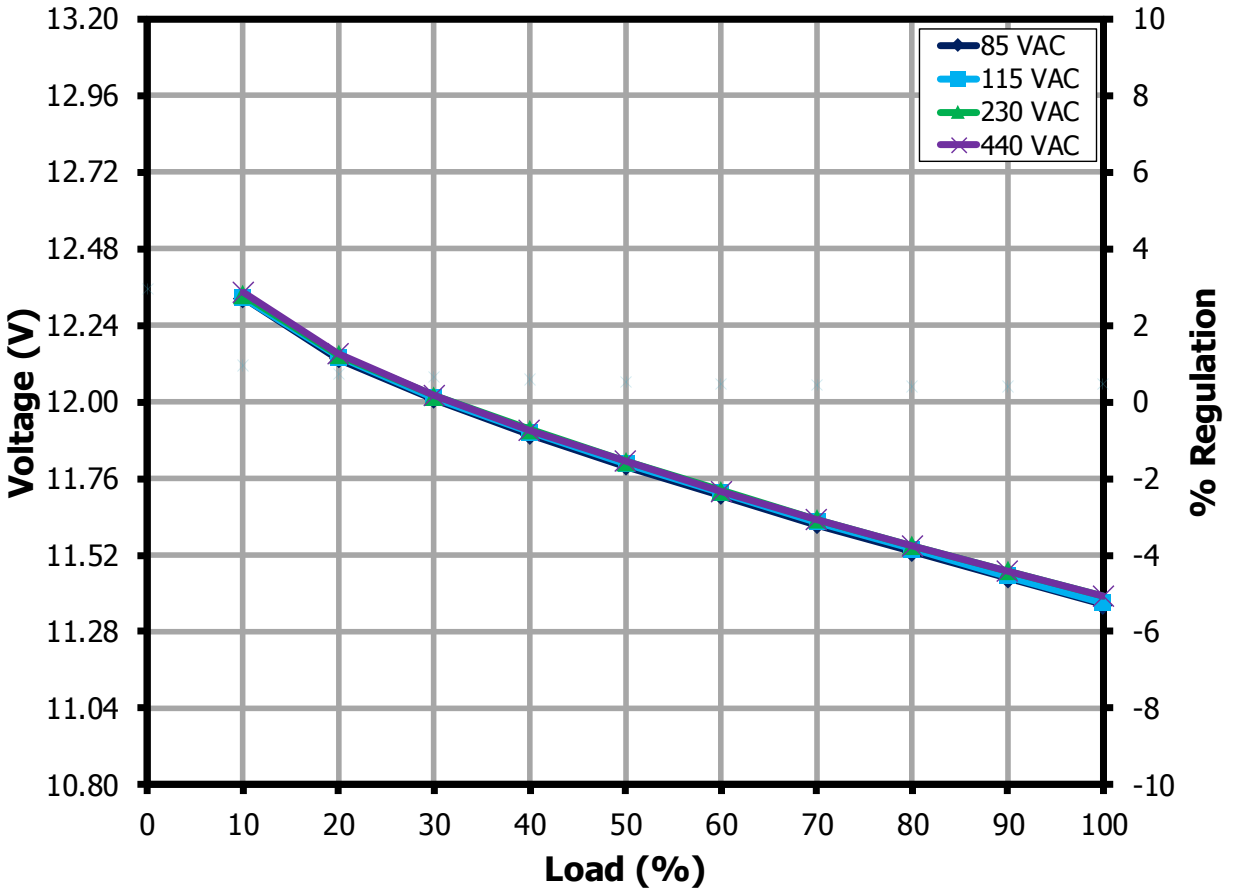

Figure 16 – 12 V Load Regulation.
Condition: 12 V Load Sweep, 5 V at 50 mA.

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9.3.5 *Line Regulation*

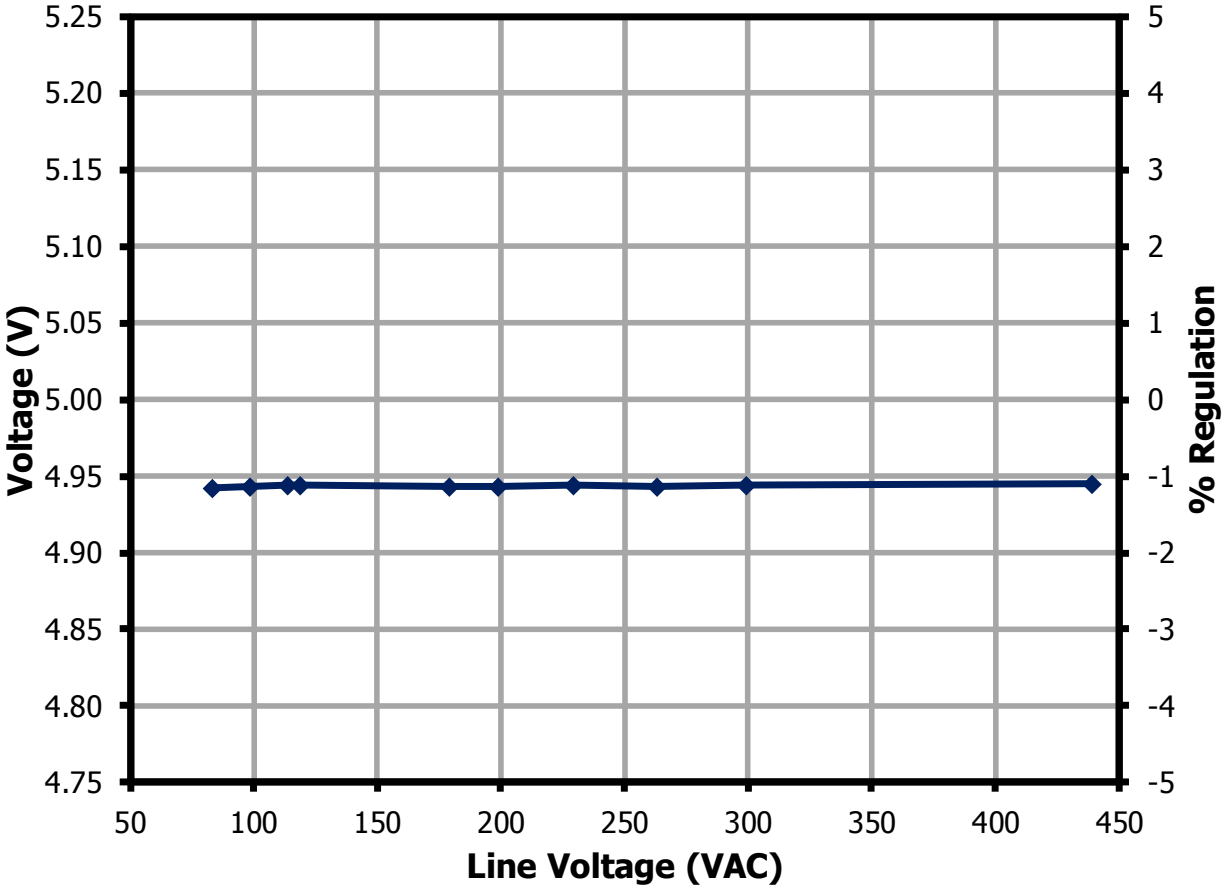

Figure 17 – 5 V Output Regulation vs. Input Line Voltage.

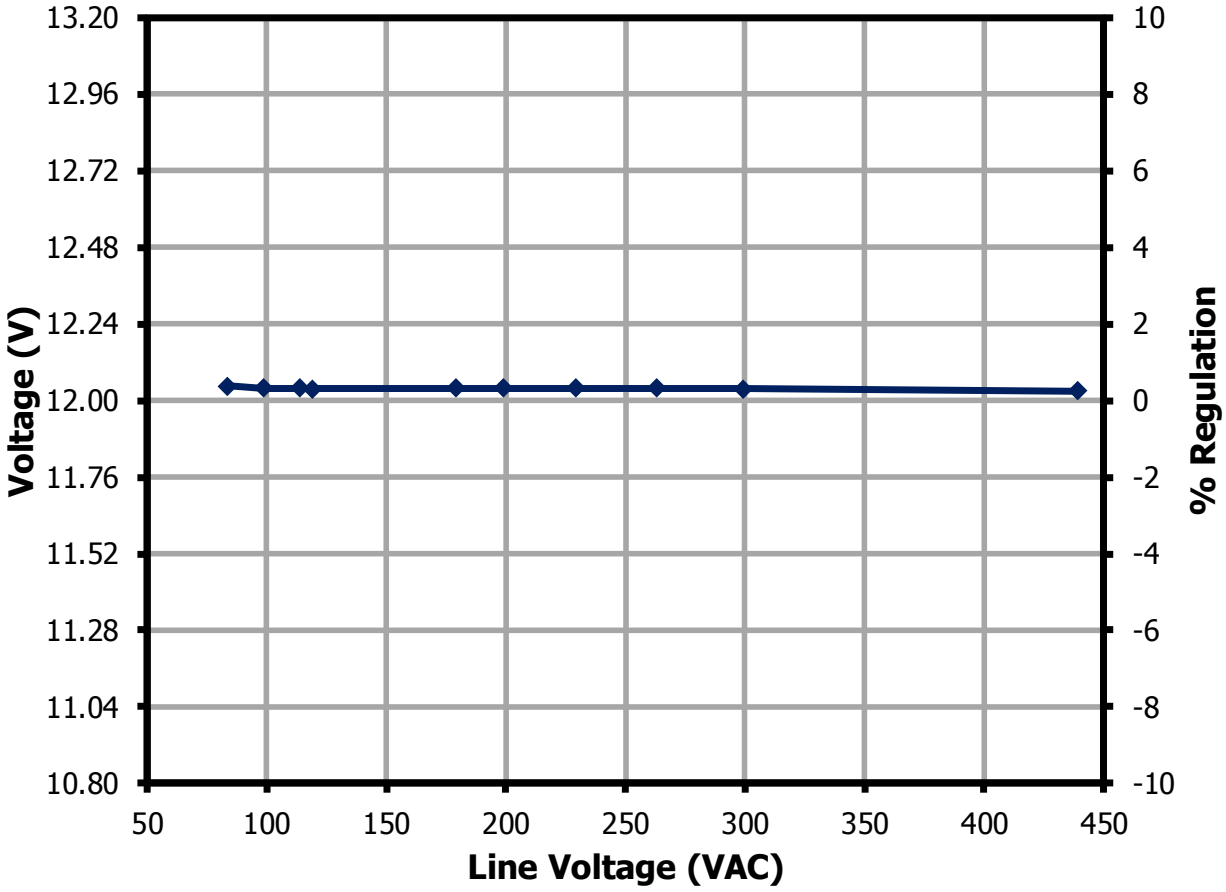

Figure 18 – 12 V Output Regulation vs. Input Line Voltage.

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10 Waveforms

10.1 Output Voltage Ripple

10.1.1 *Ripple Measurement Technique*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below). Ripple measurement done at the end of a 100 mΩ cable.

Figure 19 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

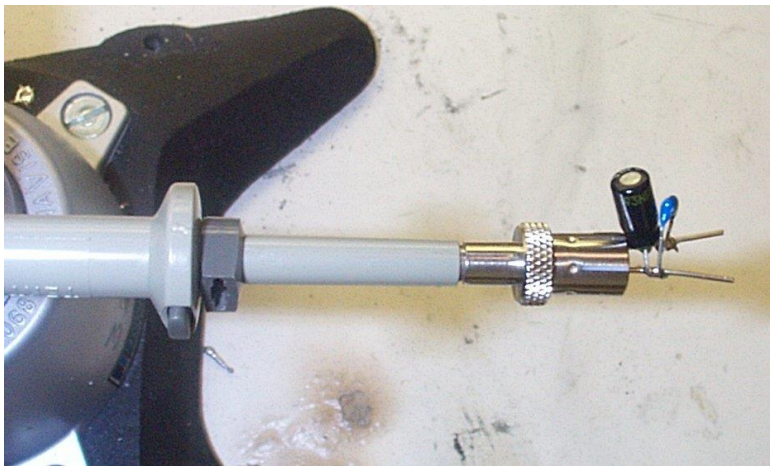

Figure 20 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

10.1.2 *Ripple Waveforms at Full Load*

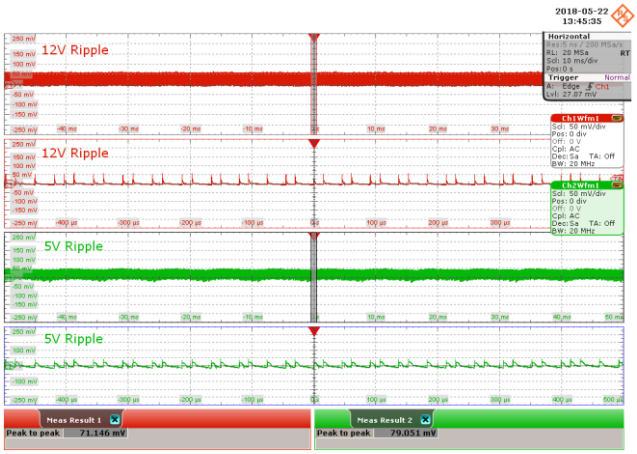

Figure 21 – 85 VAC Input.
Vertical: 50 mV / div.
Horizontal: 10 ms / div., 100 μs / div.
12 V Ripple: 71.146 $mV_{PK-PK.}$
5 V Ripple: 79.051 $mV_{PK-PK.}$

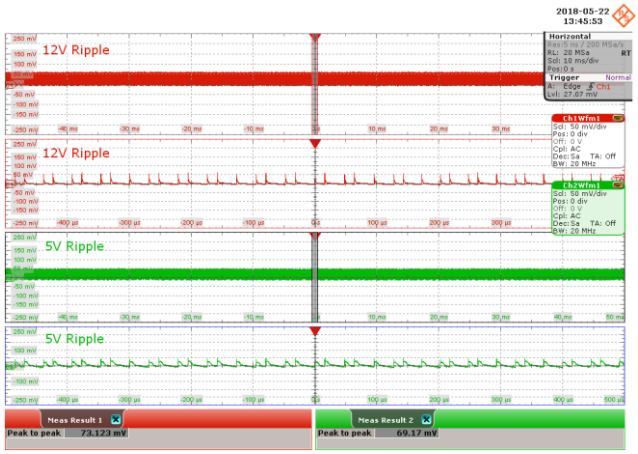

Figure 22 – 115 VAC Input.
Vertical: 50 mV / div.
Horizontal: 10 ms / div., 100 μs / div.
12 V Ripple: 73.123 $mV_{PK-PK.}$
5 V Ripple: 69.170 $mV_{PK-PK.}$

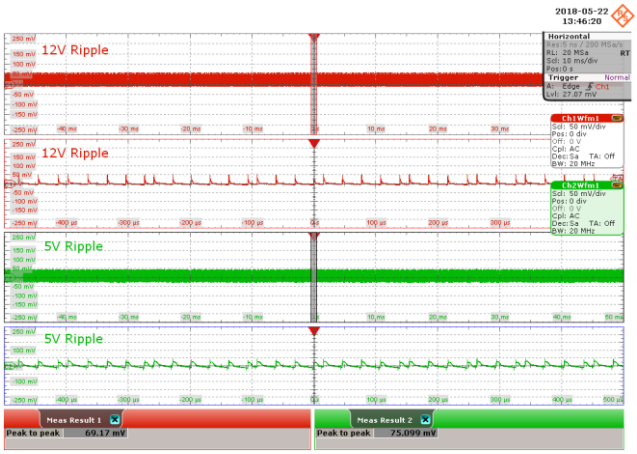

Figure 23 – 230 VAC Input.
Vertical: 50 mV / div.
Horizontal: 10 ms / div., 100 μs / div.
12 V Ripple: 69.170 $mV_{PK-PK.}$
5 V Ripple: 75.099 $mV_{PK-PK.}$

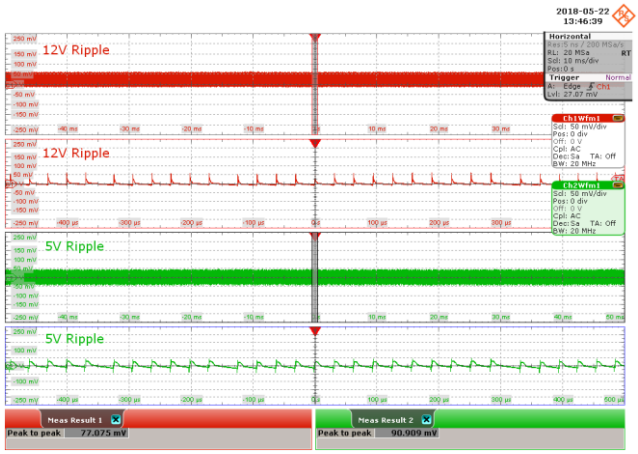

Figure 24 – 440 VAC Input.
Vertical: 50 mV / div.
Horizontal: 10 ms / div., 100 μs / div.
12 V Ripple: 77.075 $mV_{PK-PK.}$
5 V Ripple: 90.909 $mV_{PK-PK.}$

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10.1.3 *Ripple Waveforms at No-Load*

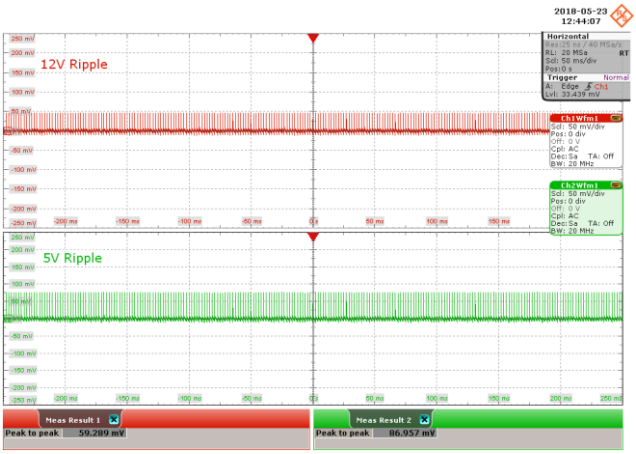

Figure 25 – 85 VAC Input.
Vertical: 50 mV / div.
Horizontal: 50 ms / div.
12 V Ripple: 59.289 $mV_{PK-PK.}$
5 V Ripple: 86.957 $mV_{PK-PK.}$

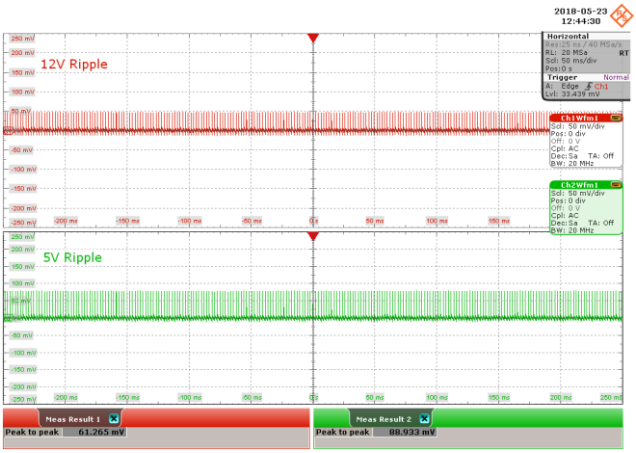

Figure 26 – 115 VAC Input.
Vertical: 50 mV / div.
Horizontal: 50 ms / div.
12 V Ripple: 61.265 $mV_{PK-PK.}$
5 V Ripple: 88.933 $mV_{PK-PK.}$

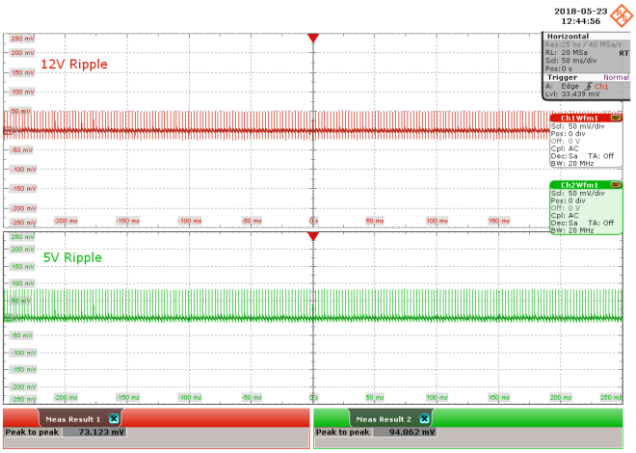

Figure 27 – 230 VAC Input.
Vertical: 50 mV / div.
Horizontal: 50 ms / div.
12 V Ripple: 73.123 $mV_{PK-PK.}$
5 V Ripple: 94.862 $mV_{PK-PK.}$

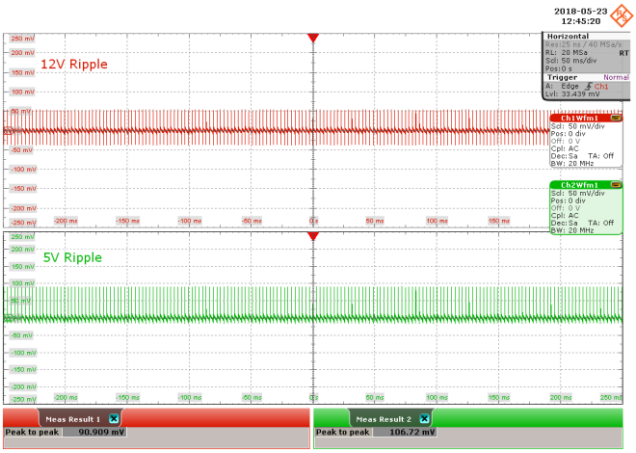

Figure 28 – 440 VAC Input.
Vertical: 50 mV / div.
Horizontal: 50 ms / div.
12 V Ripple: 90.909 $mV_{PK-PK.}$
5 V Ripple: 106.72 $mV_{PK-PK.}$

10.1.4 *Ripple vs. Load*

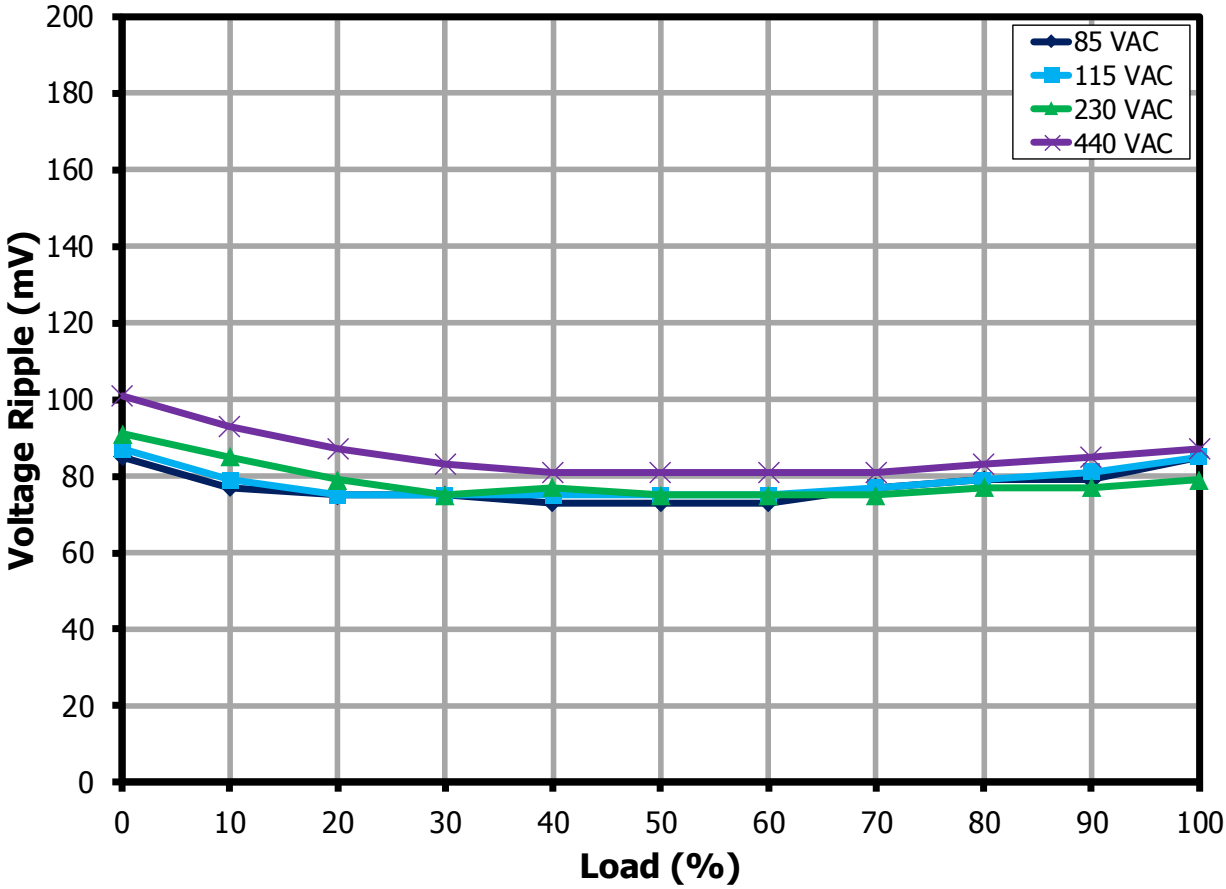

Figure 29 – 5 V Output Ripple vs. Percent Load.

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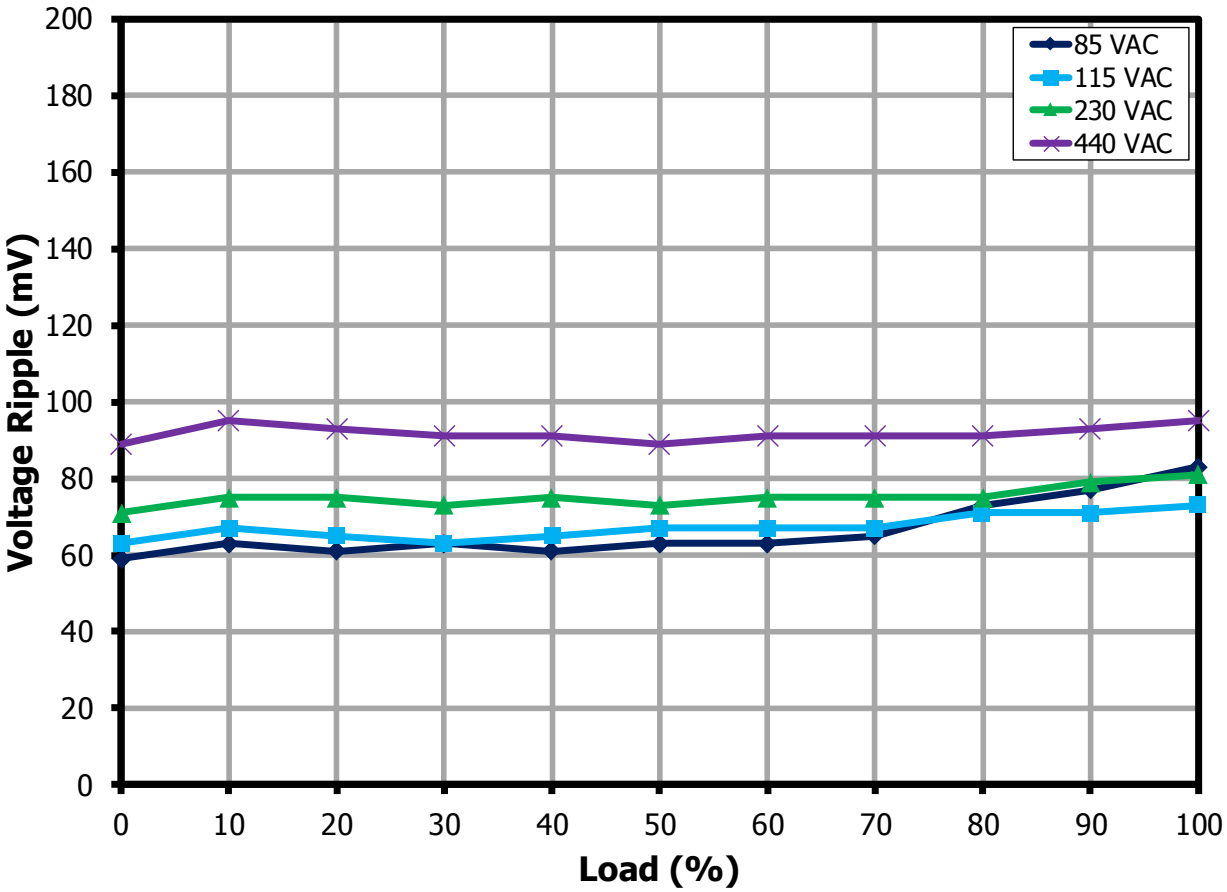

Figure 30 – 12 V Output Ripple vs. Percent Load.

10.2 **Switching Waveforms**

10.2.1 *V_{DS} and I_{DS}*

Test conditions: 12 V load set to CC at 500 mA, 5 V load set to CC at 200 mA

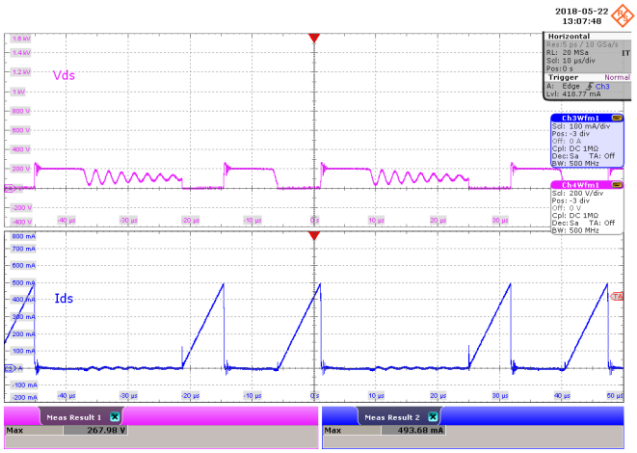

Figure 31 – 85 VAC Input.
Upper: V_{DS}, 200 V / div., 10 µs / div.
Lower: I_{DS}, 100 mA / div.
$V_{DS(MAX)}$: 267.98 V.
$I_{DS(MAX)}$: 493.68 mA.

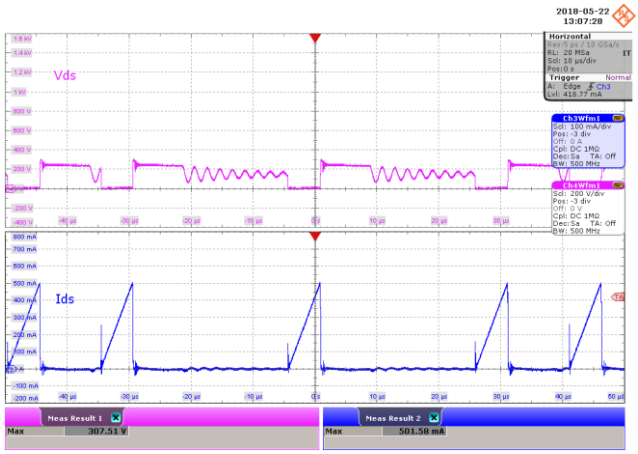

Figure 32 – 115 VAC Input.
Upper: V_{DS}, 200 V / div., 10 µs / div.
Lower: I_{DS}, 100 mA / div.
$V_{DS(MAX)}$: 307.51 V.
$I_{DS(MAX)}$: 501.58 mA.

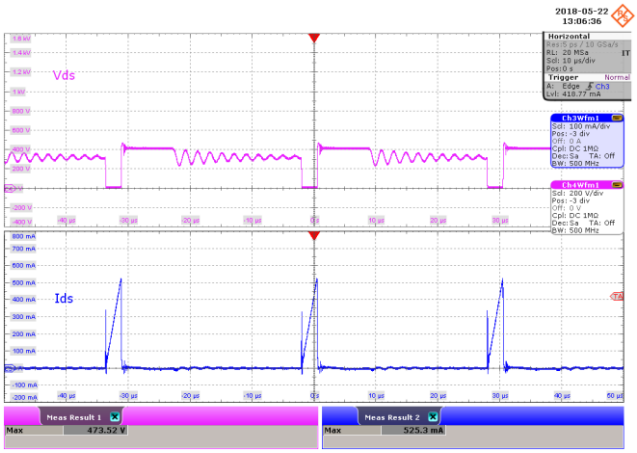

Figure 33 – 230 VAC Input.
Upper: V_{DS}, 200 V / div., 10 µs / div.
Lower: I_{DS}, 100 mA / div.
$V_{DS(MAX)}$: 473.52 V.
$I_{DS(MAX)}$: 523.30 mA.

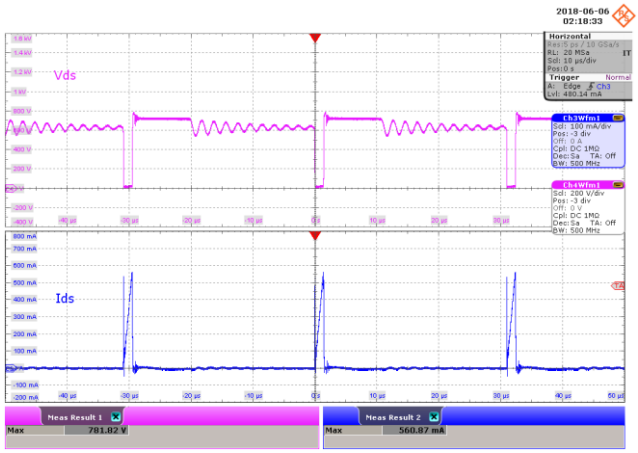

Figure 34 – 450 VAC Input.
Upper: V_{DS}, 200 V / div., 10 µs / div.
Lower: I_{DS}, 100 mA / div.
$V_{DS(MAX)}$: 781.82 V.
$I_{DS(MAX)}$: 560.87 mA.

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10.2.2 *5 V Output Diode Voltage and Current*

Test conditions: 12 V load set to CC at 500 mA, 5 V load set to CC at 200 mA

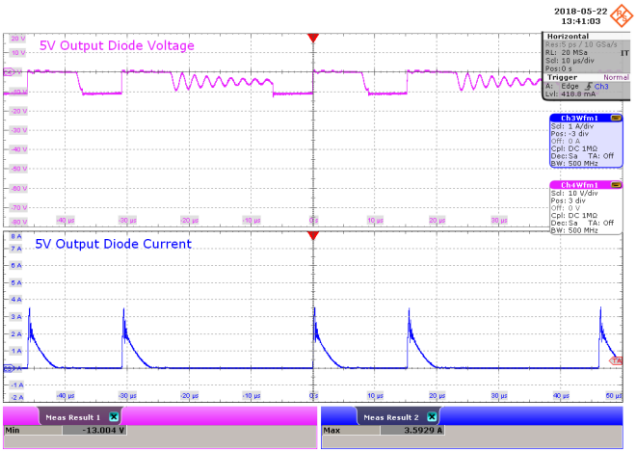

Figure 35 – 85 VAC Input.
Upper: PIV, 10 V / div., 10 μs / div.
Lower: $I_{D(MAX)}$, 1 A / div.
PIV: 13.004 V.
$I_{D(MAX)}$: 3.5929 A.

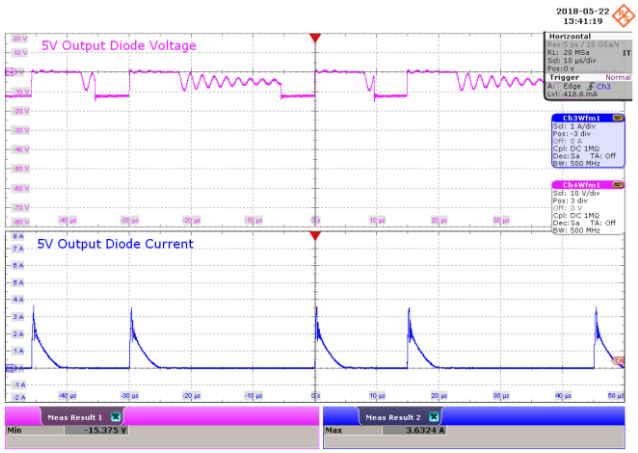

Figure 36 – 115 VAC Input.
Upper: PIV, 10 V / div., 10 μs / div.
Lower: $I_{D(MAX)}$, 1 A / div.
PIV: 15.375 V.
$I_{D(MAX)}$: 3.6324 A.

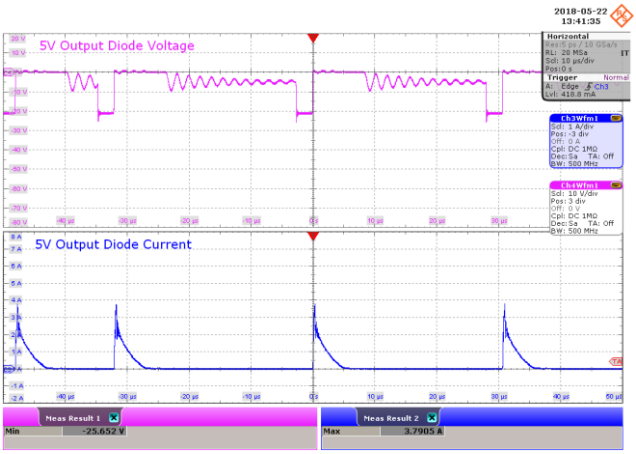

Figure 37 – 230 VAC Input.
Upper: PIV, 10 V / div., 10 μs / div.
Lower: $I_{D(MAX)}$, 1 A / div.
PIV: 25.652 V.
$I_{D(MAX)}$: 3.7905 A.

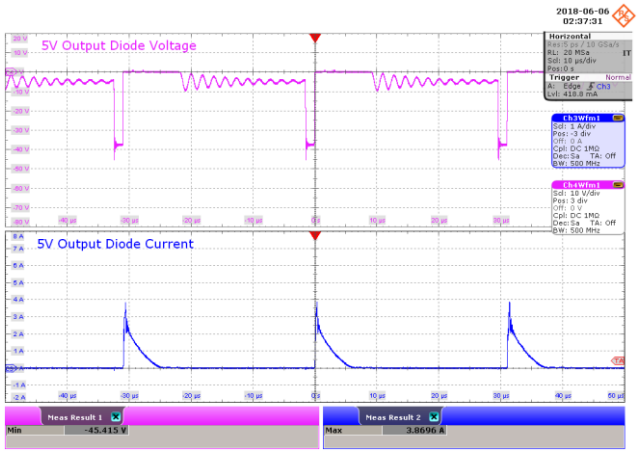

Figure 38 – 450 VAC Input.
Upper: PIV, 10 V / div., 10 μs / div.
Lower: $I_{D(MAX)}$, 1 A / div.
PIV: 45.415 V.
$I_{D(MAX)}$: 3.9091 A.

10.2.3 *12 V Output Diode Voltage and Current*

Test conditions: 12 V load set to CC at 500 mA, 5 V load set to CC at 200 mA

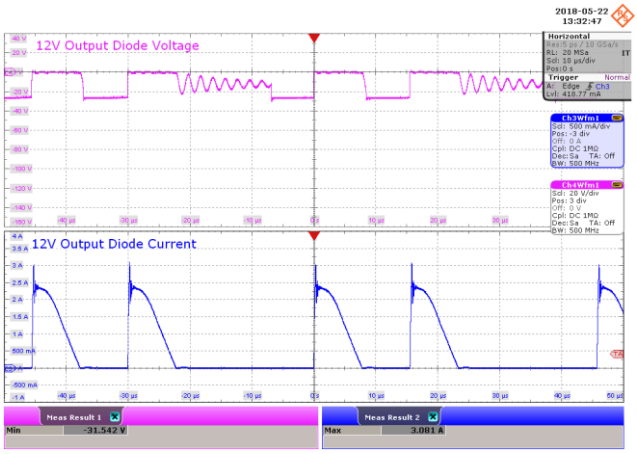

Figure 39 – 85 VAC Input.
Upper: PIV, 20 V / div., 10 µs / div.
Lower: $I_{D(MAX)}$, 500 mA / div.
PIV: 31.542 V.
$I_{D(MAX)}$: 3.0810 A.

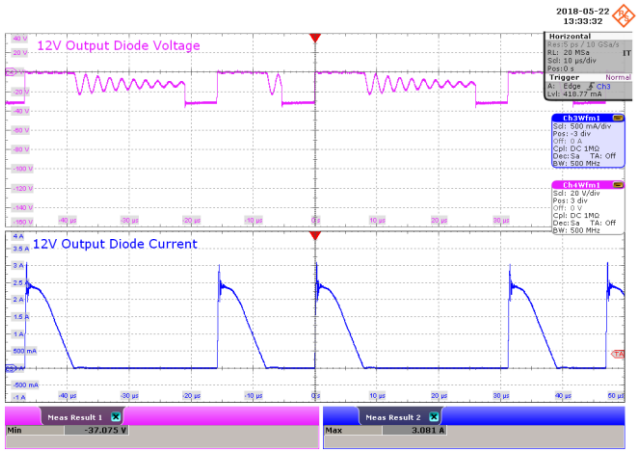

Figure 40 – 115 VAC Input.
Upper: PIV, 20 V / div., 10 µs / div.
Lower: $I_{D(MAX)}$, 500 mA / div.
PIV: 37.075 V.
$I_{D(MAX)}$: 3.0810 A.

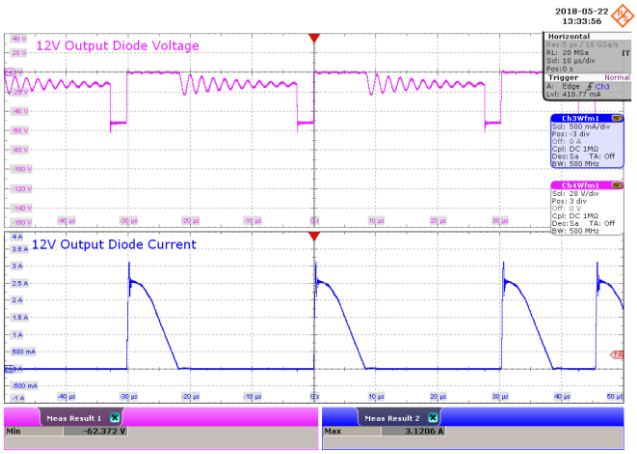

Figure 41 – 230 VAC Input.
Upper: PIV, 20 V / div., 10 µs / div.
Lower: $I_{D(MAX)}$, 500 mA / div.
PIV: 62.372 V.
$I_{D(MAX)}$: 3.1206 A.

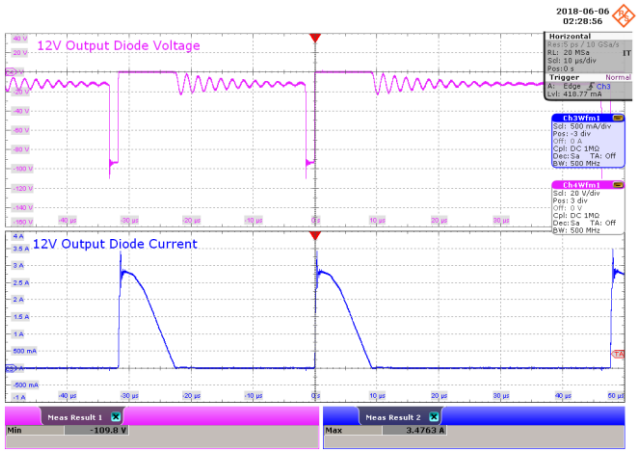

Figure 42 – 450 VAC Input.
Upper: PIV, 20 V / div., 10 µs / div.
Lower: $I_{D(MAX)}$, 500 mA / div.
PIV: 109.80 V.
$I_{D(MAX)}$: 3.4763 A.

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10.3 **Start-up Performance**

10.3.1 *12 V Start-up Operation V_{IN}, V_{OUT} and I_{OUT}*

Test conditions: 12 V load set to CR at 24 Ω, 5 V load set to CR at 25 Ω

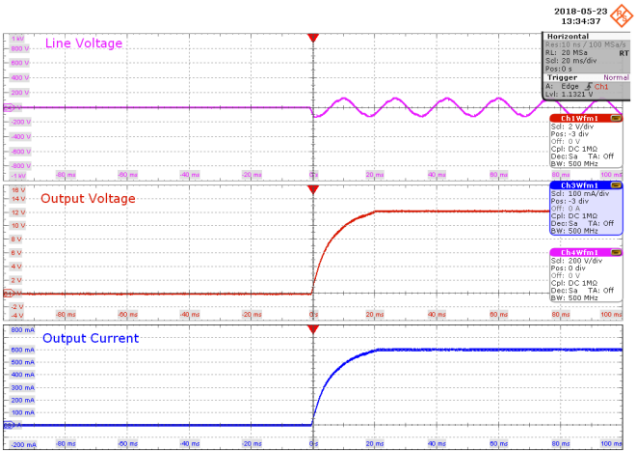

Figure 43 – 85 VAC Input.
Upper: V_{IN}, 200 V / div., 20 ms / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 100 mA / div.

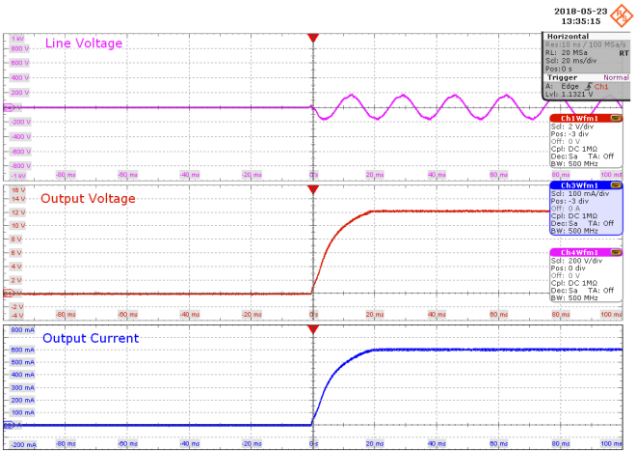

Figure 44 – 115 VAC Input.
Upper: V_{IN}, 200 V / div., 20 ms / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 100 mA / div.

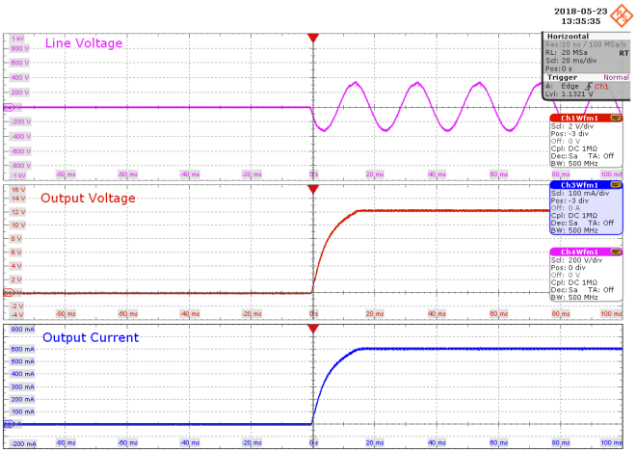

Figure 45 – 230 VAC Input.
Upper: V_{IN}, 200 V / div., 20 ms / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 100 mA / div.

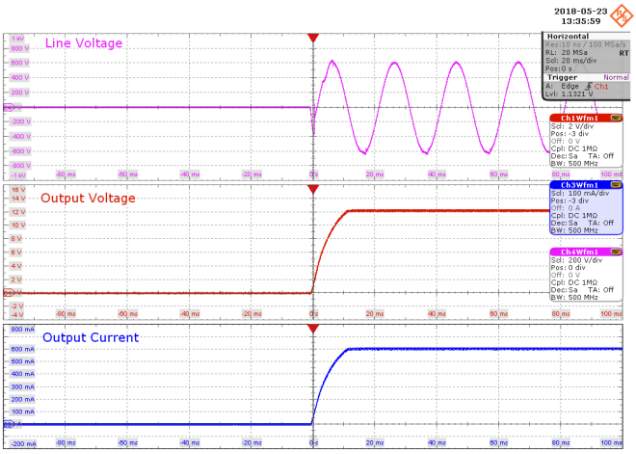

Figure 46 – 440 VAC Input.
Upper: V_{IN}, 200 V / div., 20 ms / div.
Middle: V_{OUT}, 2 V / div.
Lower: I_{OUT}, 100 mA / div.

10.3.2 *5 V Start-up Operation V_{IN}, V_{OUT} and I_{OUT}*

Test conditions: 12 V load set to CR at 24Ω, 5 V load set to CR at 25Ω

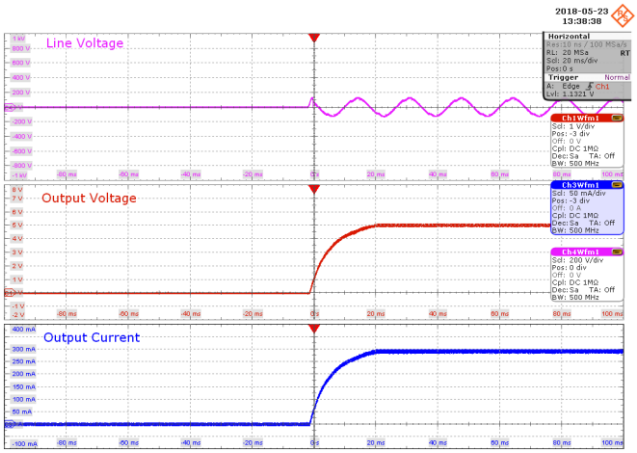

Figure 47 – 85 VAC Input.
Upper: V_{IN}, 200 V / div., 20 ms / div.
Middle: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 50 mA / div.

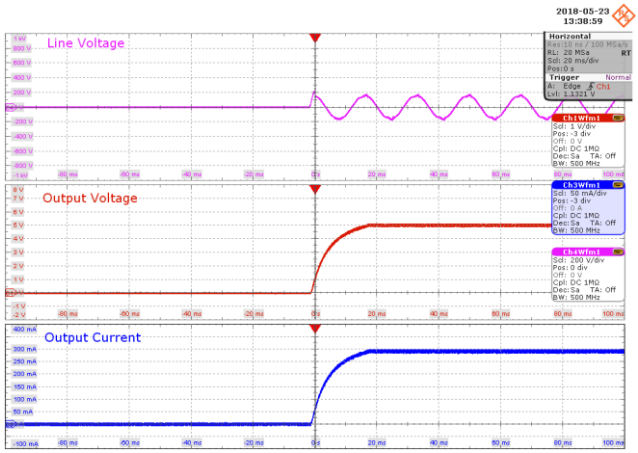

Figure 48 – 115 VAC Input.
Upper: V_{IN}, 200 V / div., 20 ms / div.
Middle: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 50 mA / div.

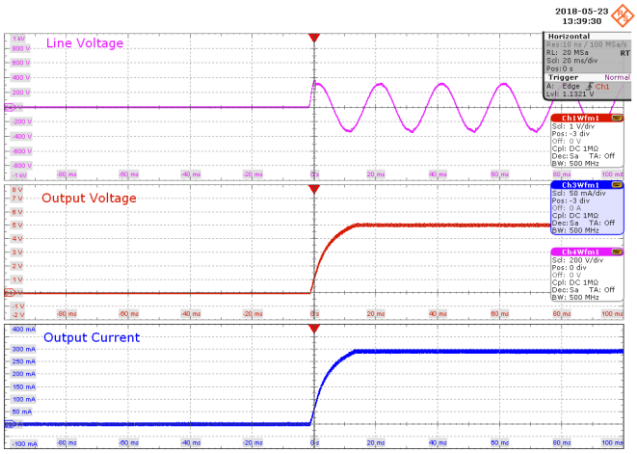

Figure 49 – 230 VAC Input.
Upper: V_{IN}, 200 V / div., 20 ms / div.
Middle: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 50 mA / div.

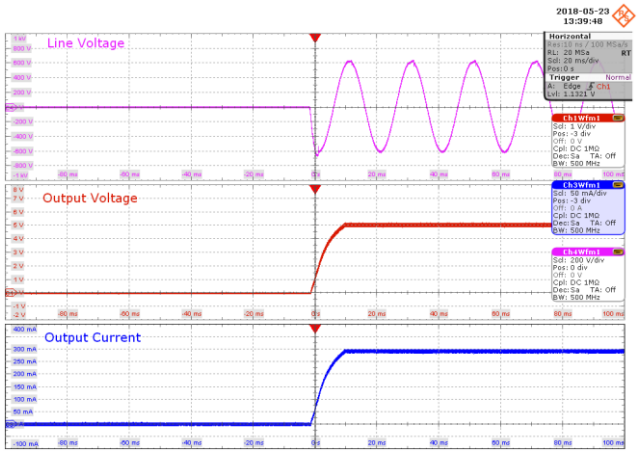

Figure 50 – 440 VAC Input.
Upper: V_{IN}, 200 V / div., 20 ms / div.
Middle: V_{OUT}, 1 V / div.
Lower: I_{OUT}, 50 mA / div.

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10.3.3 *Start-up Operation V_{DS} and I_{DS}*

Test conditions: 12 V load set to CC at 500 mA, 5 V load set to CC at 200 mA

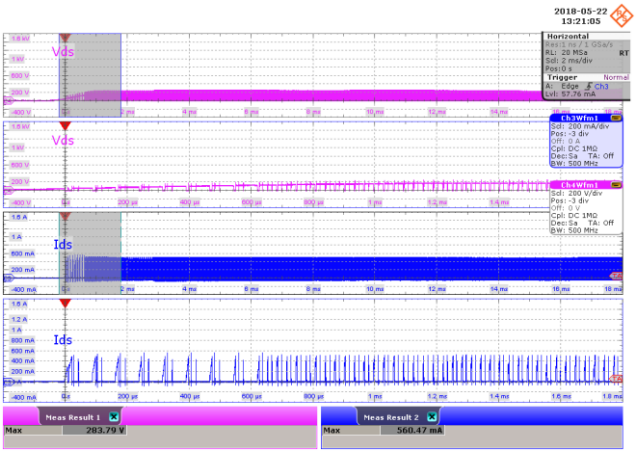

Figure 51 – 85 VAC Input.
Upper: V_{DS}, 200 V / div., 2 ms / div.
Lower: I_{DS}, 200 mA / div.
Zoom: 200 µs / div.
$V_{DS(MAX)}$: 283.79 V.
$I_{DS(MAX)}$: 560.47 mA.

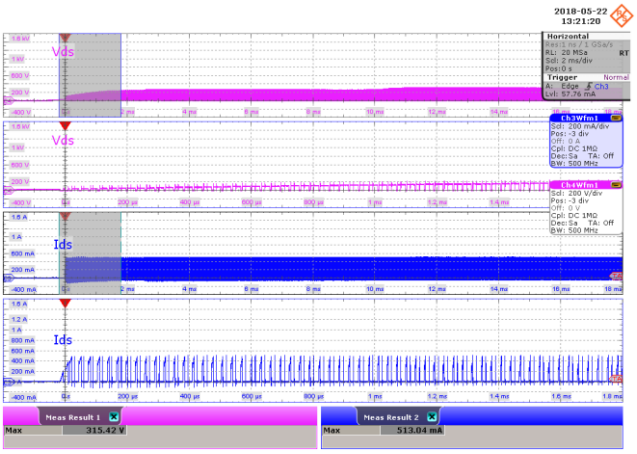

Figure 52 – 115 VAC Input.
Upper: V_{DS}, 200 V / div., 2 ms / div.
Lower: I_{DS}, 200 mA / div.
Zoom: 200 µs / div.
$V_{DS(MAX)}$: 315.42 V.
$I_{DS(MAX)}$: 513.04 mA.

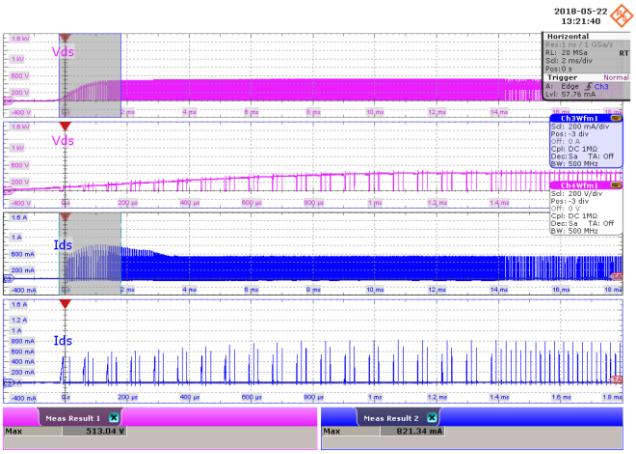

Figure 53 – 85 VAC Input.
Upper: V_{DS}, 200 V / div., 2 ms / div.
Lower: I_{DS}, 200 mA / div.
Zoom: 200 µs / div.
$V_{DS(MAX)}$: 513.04 V.
$I_{DS(MAX)}$: 821.34 mA.

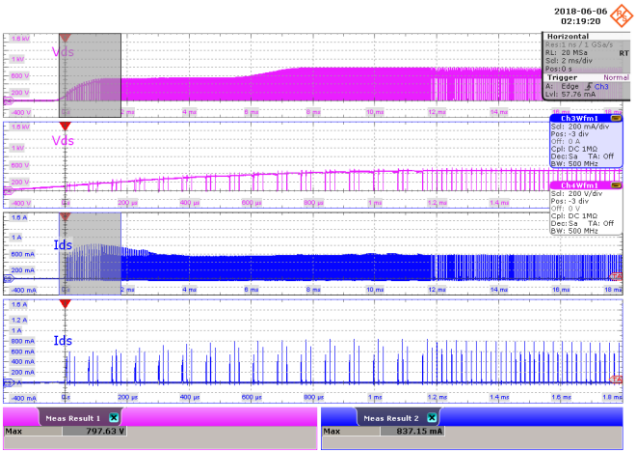

Figure 54 – 450 VAC Input.
Upper: V_{DS}, 200 V / div., 10 µs / div.
Lower: I_{DS}, 100 mA / div.
$V_{DS(MAX)}$: 797.63 V.
$I_{DS(MAX)}$: 837.15 mA.

10.4 **Output Load Transient**

10.4.1 *5 V Output Transient*

Test conditions: 5 V load swings from 50 mA to full load, 12 V at full load

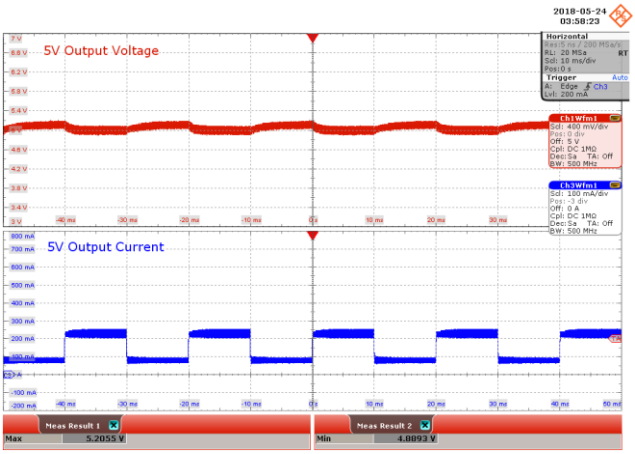

Figure 55 – 85 VAC Input.
Upper: 5 V V_{OUT}, 400 mV / div., 10 ms / div.
Lower: 5 V I_{OUT}, 100 mA / div.
V_{MAX}: 5.2055 V.
V_{MIN}: 4.8893 V.

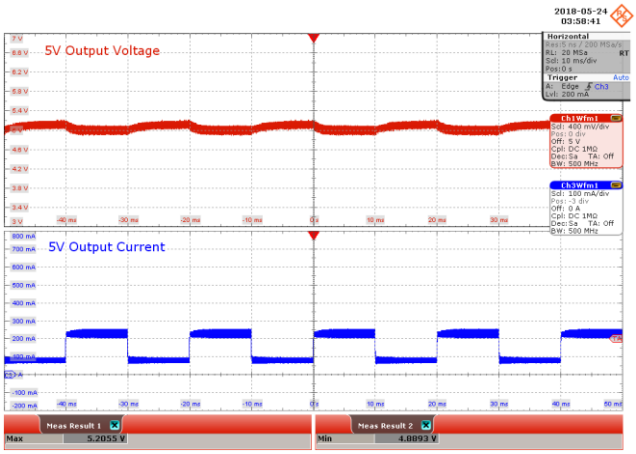

Figure 56 – 115 VAC Input.
Upper: 5 V V_{OUT}, 400 mV / div., 10 ms / div.
Lower: 5 V I_{OUT}, 100 mA / div.
V_{MAX}: 5.2055 V.
V_{MIN}: 4.8893 V.

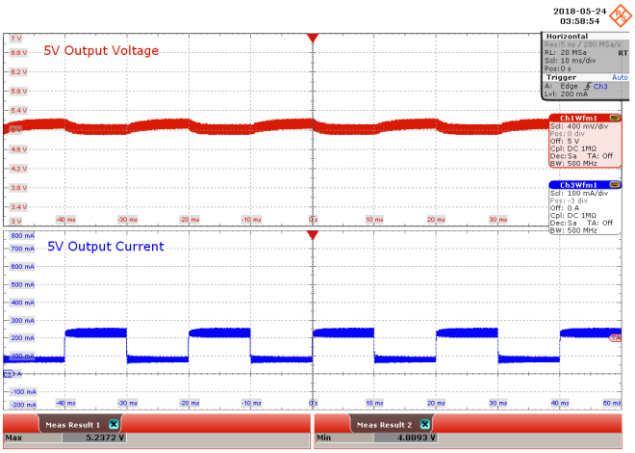

Figure 57 – 230 VAC Input.
Upper: 5 V V_{OUT}, 400 mV / div., 10 ms / div.
Lower: 5 V I_{OUT}, 100 mA / div.
V_{MAX}: 5.2372 V.
V_{MIN}: 4.8893 V.

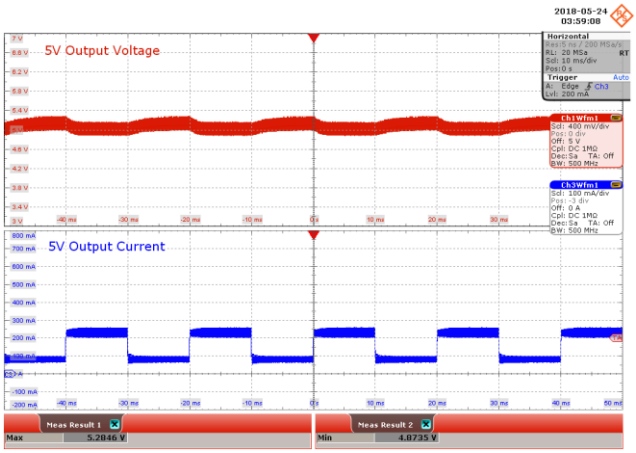

Figure 58 – 440 VAC Input.
Upper: 5 V V_{OUT}, 400 mV / div., 10 ms / div.
Lower: 5 V I_{OUT}, 100 mA / div.
V_{MAX}: 5.2846 V.
V_{MIN}: 4.8735 V.

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10.4.2 *12 V Output Transient*

Test conditions: 12 V load swings from 50 mA to full load, 5 V at full load

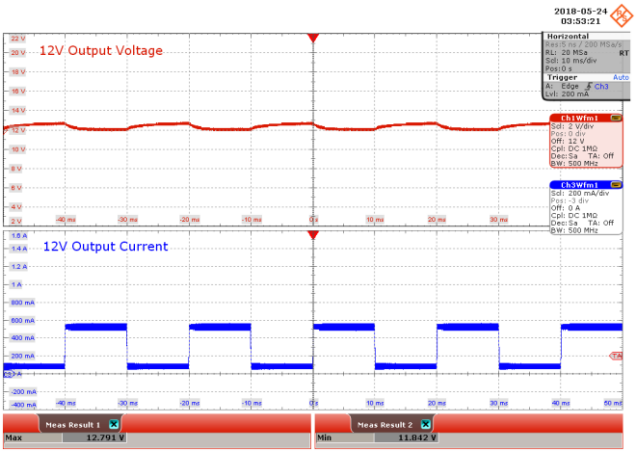

Figure 59 – 85 VAC Input.
Upper: 12 V V_{OUT}, 2 V / div., 10 ms / div.
Lower: 12 V I_{OUT}, 200 mA / div.
V_{MAX}: 12.791 V.
V_{MIN}: 11.842 V.

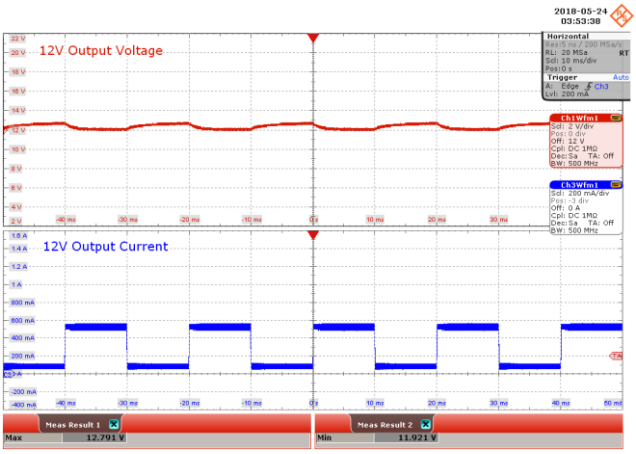

Figure 60 – 115 VAC Input.
Upper: 12 V V_{OUT}, 2 V / div., 10 ms / div.
Lower: 12 V I_{OUT}, 200 mA / div.
V_{MAX}: 12.791 V.
V_{MIN}: 11.921 V.

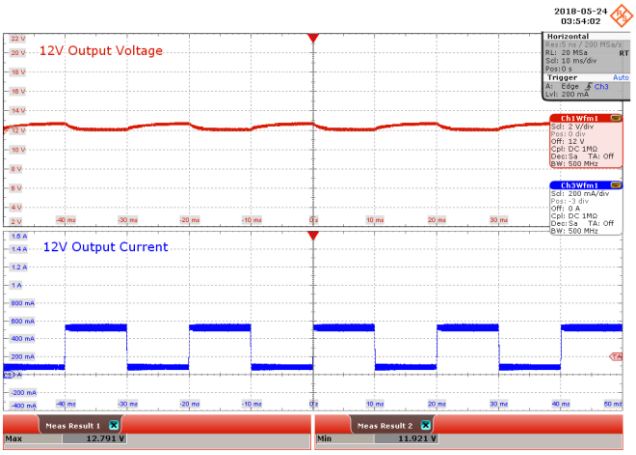

Figure 61 – 230 VAC Input.
Upper: 12 V V_{OUT}, 2 V / div., 10 ms / div.
Lower: 12 V I_{OUT}, 200 mA / div.
V_{MAX}: 12.791 V.
V_{MIN}: 11.921 V.

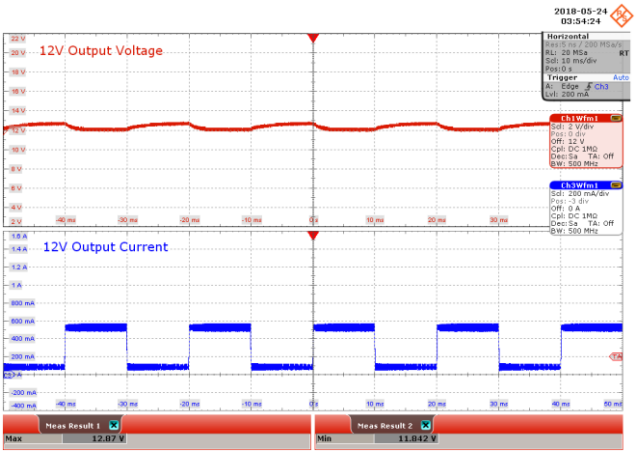

Figure 62 – 440 VAC Input.
Upper: 12 V V_{OUT}, 2 V / div., 10 ms / div.
Lower: 12 V I_{OUT}, 200 mA / div.
V_{MAX}: 12.870 V.
V_{MIN}: 11.842 V.

10.5 **Fault Waveforms**

10.5.1 *5 V Output Short*

Test conditions: Both outputs at full load before short

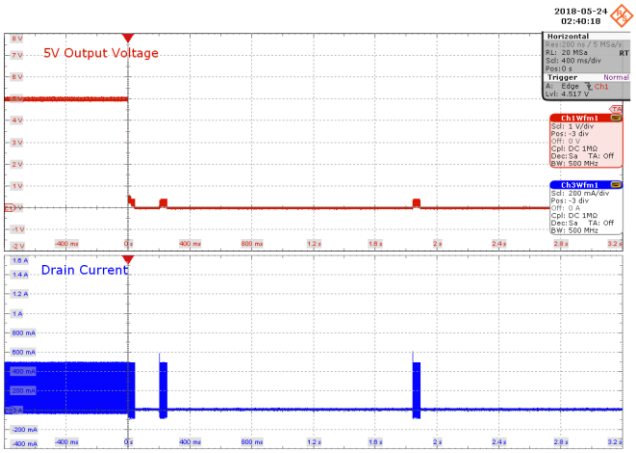

Figure 63 – 85 VAC Input.
Upper: 5 V V_{OUT}, 1 V / div., 400 ms / div.
Lower: I_{DS}, 200 mA / div.

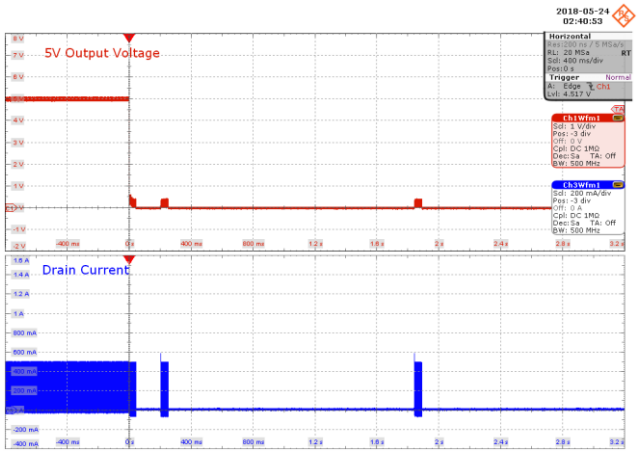

Figure 64 – 115 VAC Input.
Upper: 5 V V_{OUT}, 1 V / div., 400 ms / div.
Lower: I_{DS}, 200 mA / div.

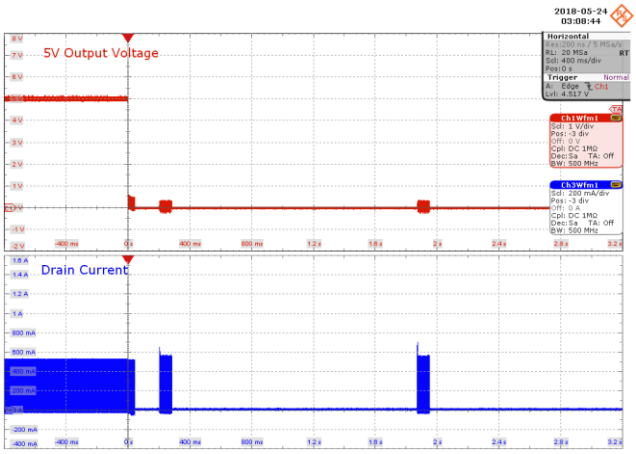

Figure 65 – 230 VAC Input.
Upper: 5 V V_{OUT}, 1 V / div., 400 ms / div.
Lower: I_{DS}, 200 mA / div.

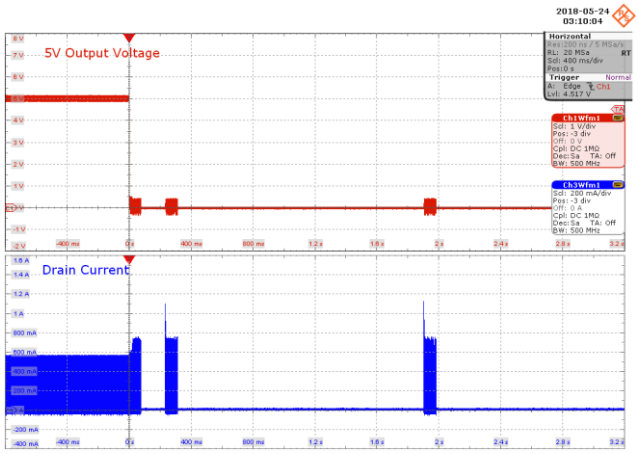

Figure 66 – 440 VAC Input.
Upper: 5 V V_{OUT}, 1 V / div., 400 ms / div.
Lower: I_{DS}, 200 mA / div.

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10.5.2 *12 V Output Short*

Test conditions: Both outputs at full load before short

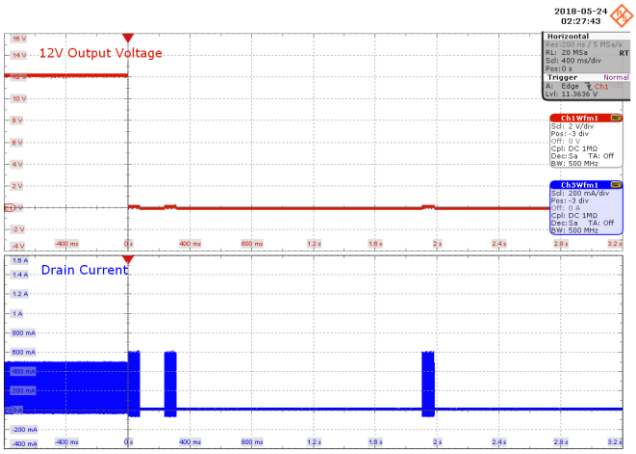

Figure 67 – 85 VAC Input.
Upper: 12 V V_{OUT}, 2 V / div., 400 ms / div.
Lower: I_{DS}, 200 mA / div.

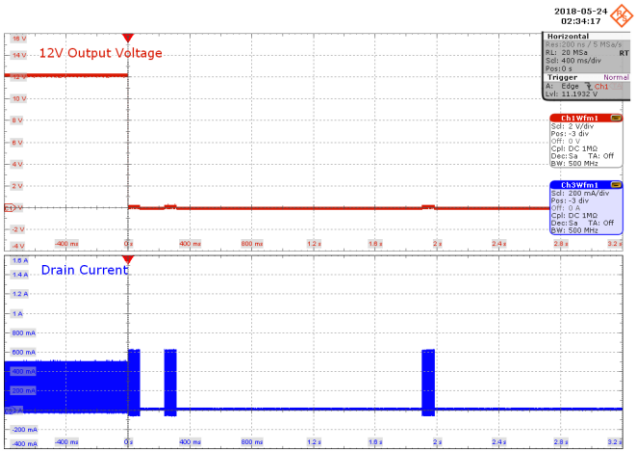

Figure 68 – 115 VAC Input.
Upper: 12 V V_{OUT}, 2 V / div., 400 ms / div.
Lower: I_{DS}, 200 mA / div.

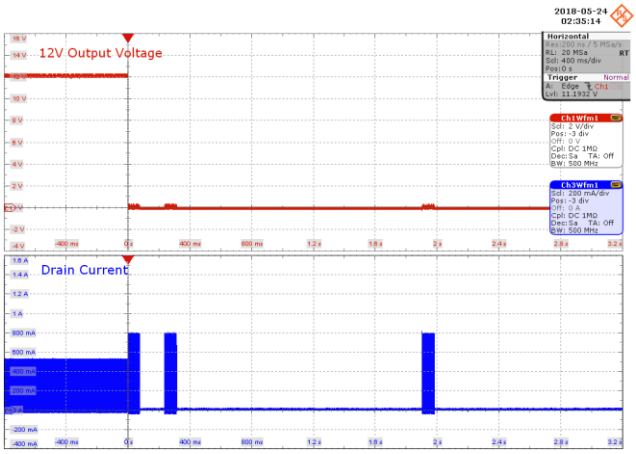

Figure 69 – 230 VAC Input.
Upper: 12 V V_{OUT}, 2 V / div., 400 ms / div.
Lower: I_{DS}, 200 mA / div.

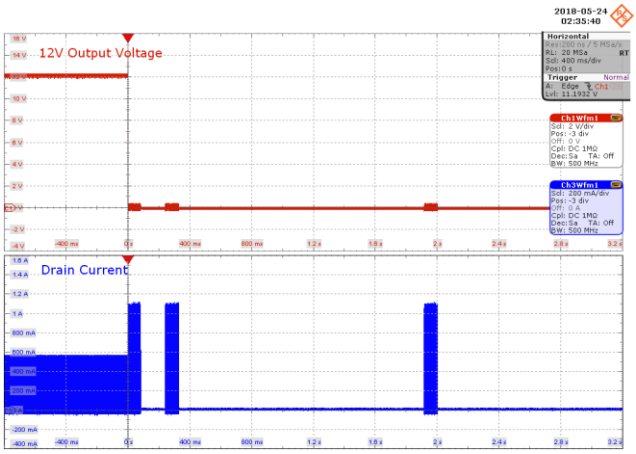

Figure 70 – 440 VAC Input.
Upper: 12 V V_{OUT}, 2 V / div., 400 ms / div.
Lower: I_{DS}, 200 mA / div.

10.5.3 *Line Overvoltage*

Test conditions: VR1 Zener diode voltage rating set to 102 V, OVP at 520 VAC_{RMS}

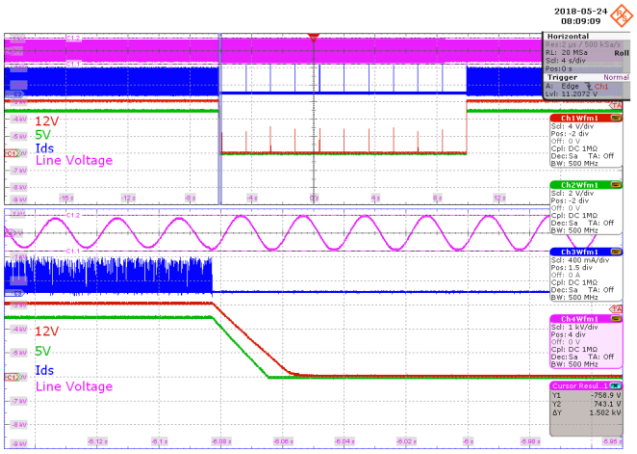

Figure 71 – Line +OV at 520 VAC_{RMS}.
Upper: 12 V V_{OUT}, 2 V / div., 400 ms / div.
Lower: I_{DS}, 200 mA / div.

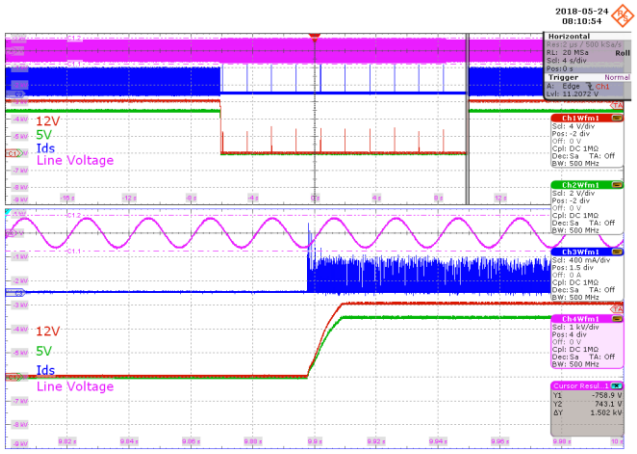

Figure 72 – Line -OV.
Upper: 12 V V_{OUT}, 2 V / div., 400 ms / div.
Lower: I_{DS}, 200 mA / div.

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11 Thermal Performance

11.1 Test Set-Up

Thermal evaluation was performed under two conditions: (1) room temperature with the circuit board enclosed inside an acrylic box and (2), 50 ºC ambient inside a thermal chamber. In both conditions, the circuit is soaked for two hours under full load conditions.

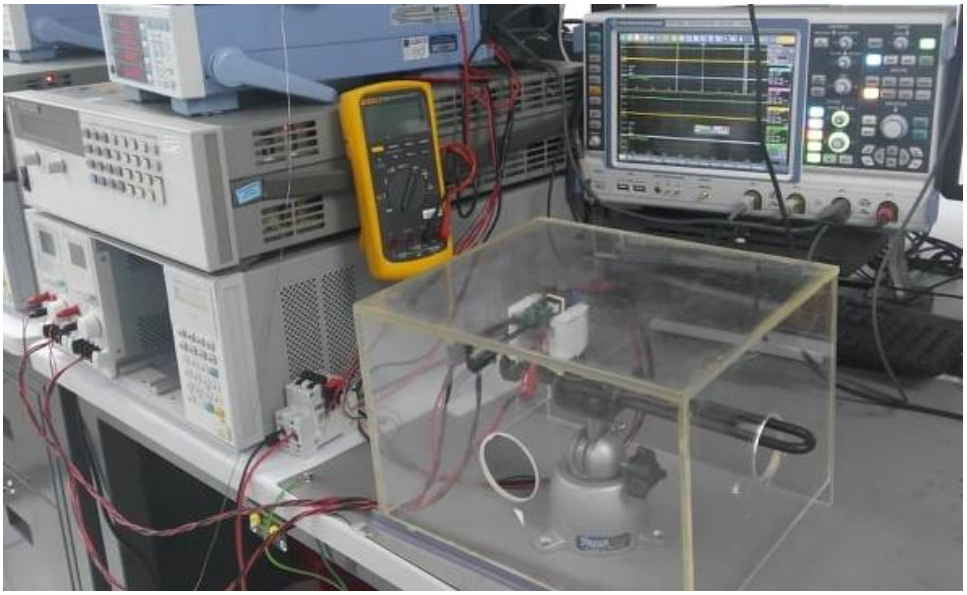

Figure 73 – Thermal Performance Set-up Using an Acrylic Box.

Figure 74 – Thermal Performance Set-up Using Thermal Chamber.

11.2 **Room Temperature**

11.2.1 *85 VAC @ Room Temperature*

Ambient (ºC)	LinkSwitch-XT2 900 V (U1)	Transformer (T1)	12 V Output Diode (T2)	Bridge Rectifier (BR1)
27	53.3	60.0	71.0	47.3

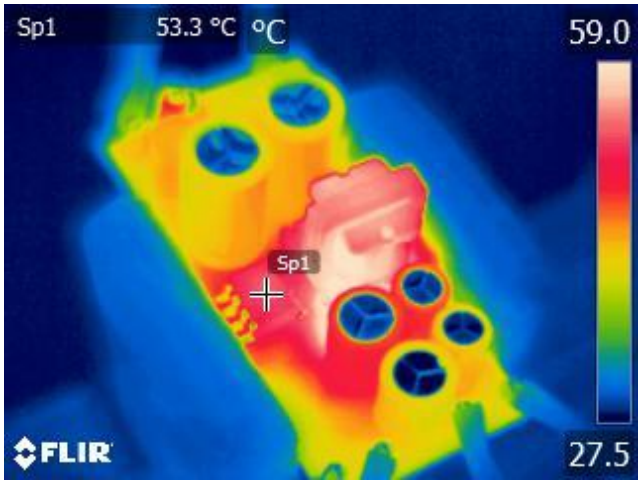

Figure 75 – Ambient = 27.5 ºC.
LNK-XT2-900, U1 = 53.3 ºC.

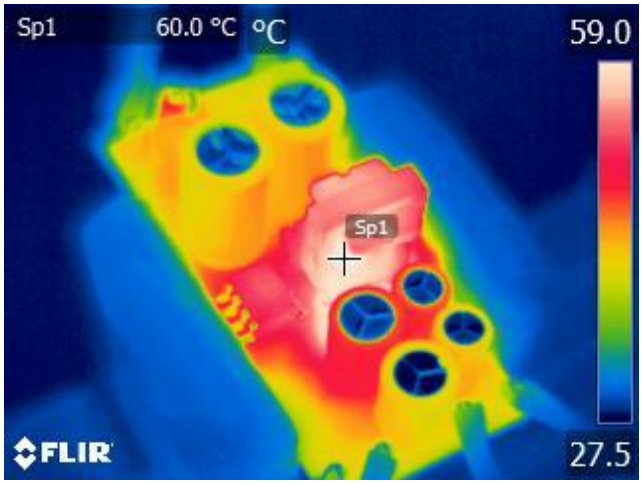

Figure 76 – Ambient = 27.5 ºC.
Transformer, T1 = 60.0 ºC.

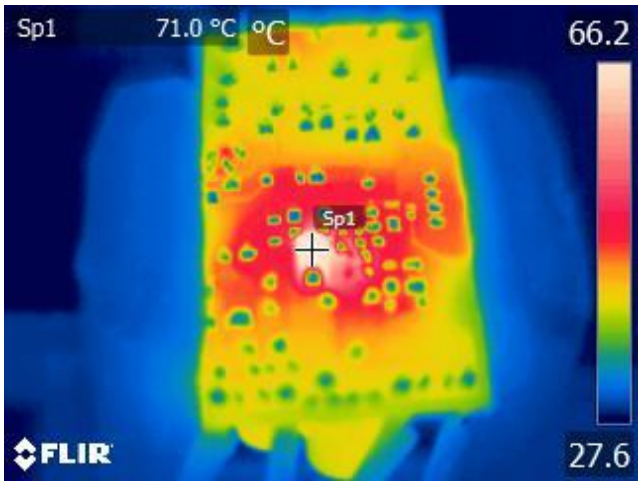

Figure 77 – Ambient = 27.6 ºC.
12 V Diode, D4 = 71.0 ºC.

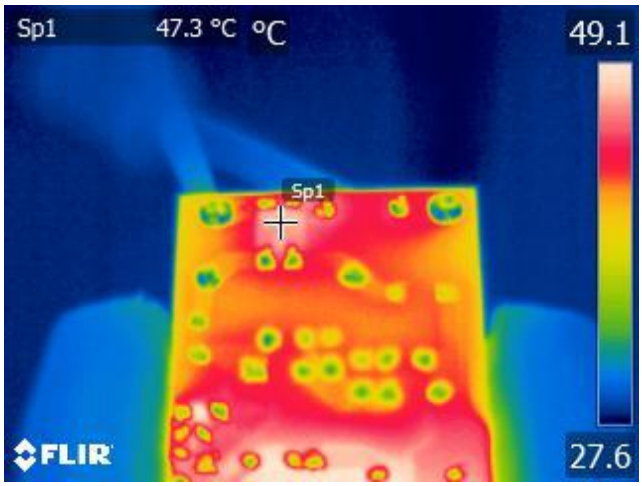

Figure 78 – Ambient = 27.6 ºC.
Bridge Rectifier, BR1 = 47.3 ºC.

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11.2.2 *440 VAC @ Room Temperature*

Ambient (ºC)	LinkSwitch-XT2 900 V (U1)	Transformer (T1)	12 V Output Diode (T2)	Bridge Rectifier (BR1)
27	54.6	63.1	78.4	37.0

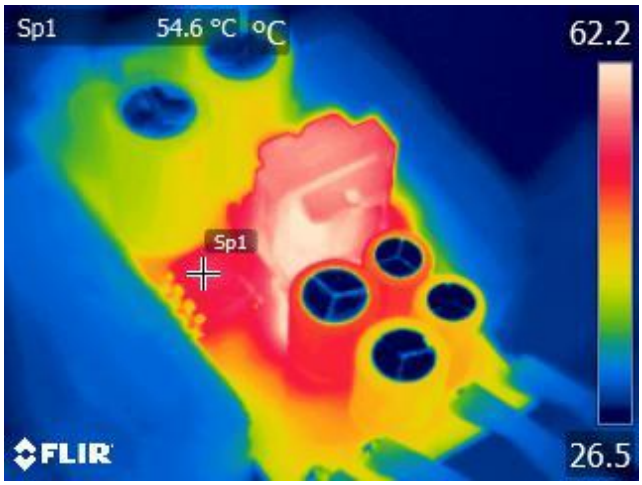

Figure 79 – Ambient = 26.5 ºC.
LNK-XT2-900, U1 = 54.6 ºC.

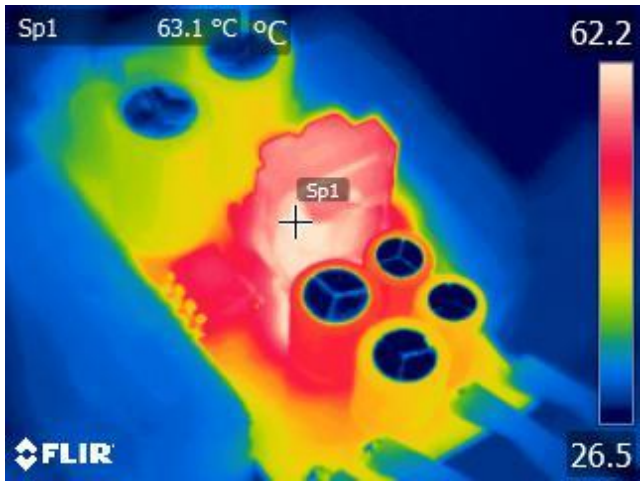

Figure 80 – Ambient = 26.5 ºC.
Transformer, T1 = 63.1 ºC.

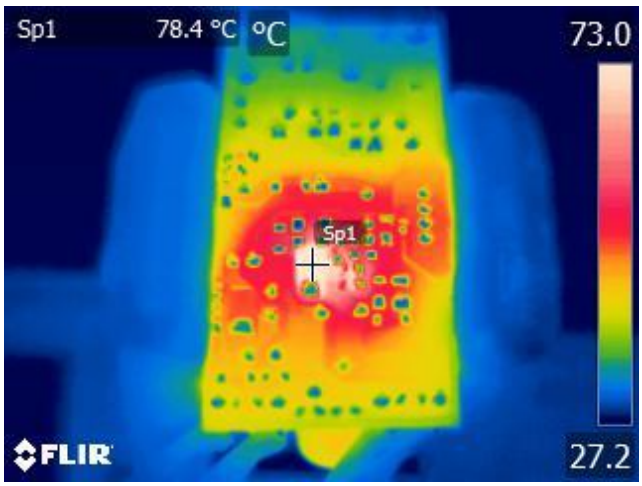

Figure 81 – Ambient = 27.2 ºC.
12 V Diode, D4 = 78.4 ºC.

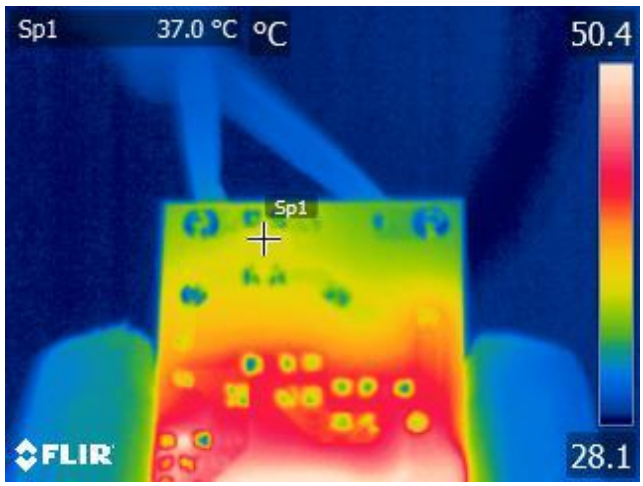

Figure 82 – Ambient = 28.1 ºC.
Bridge Rectifier, BR1 = 37.0 ºC.

11.3 **50 ºC Ambient**

11.3.1 *85 VAC @ 50 ºC*

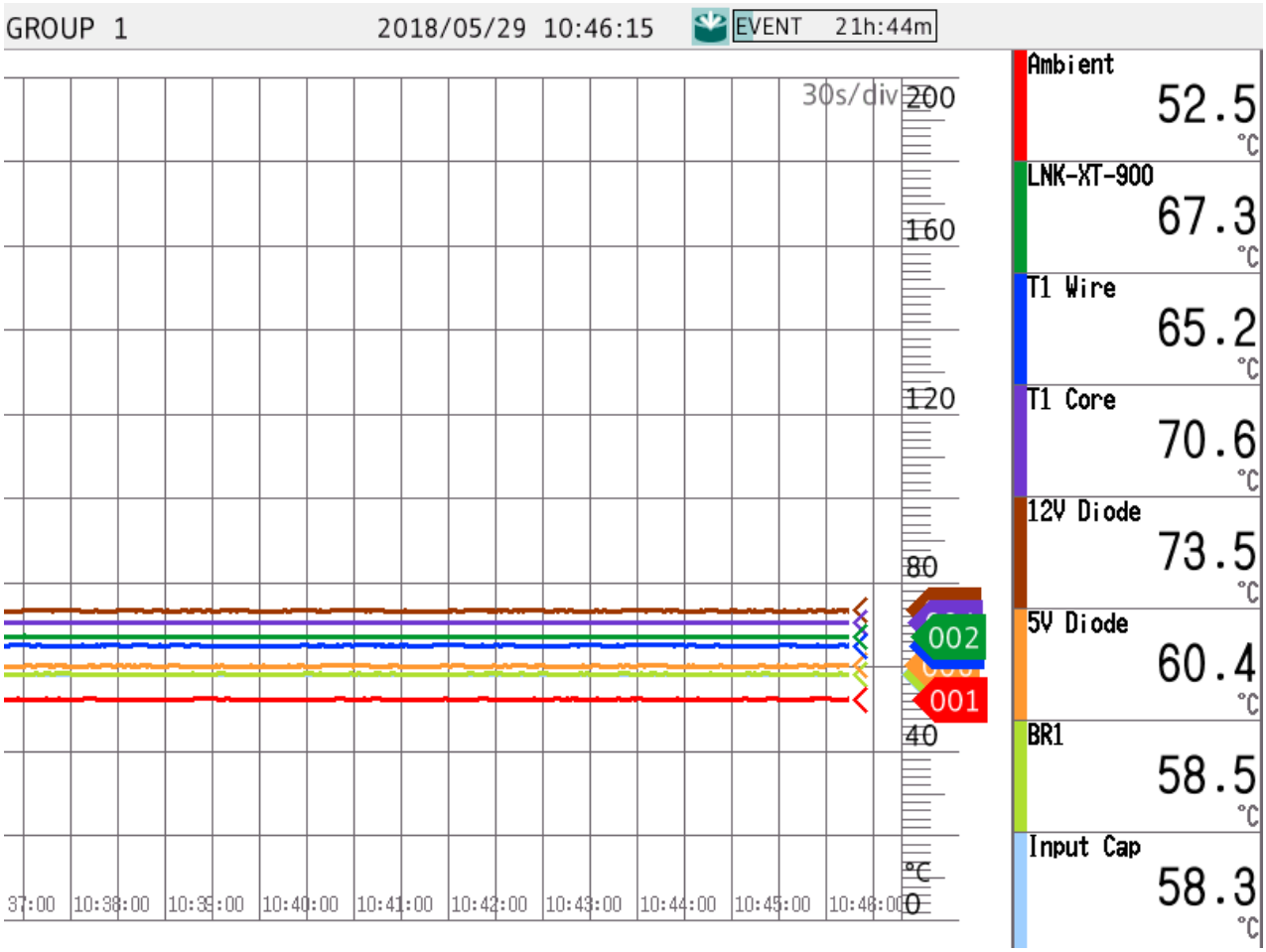

Figure 83 — Component Temperatures at 50 ºC Ambient.

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11.3.2 *440 VAC @ 50 ºC*

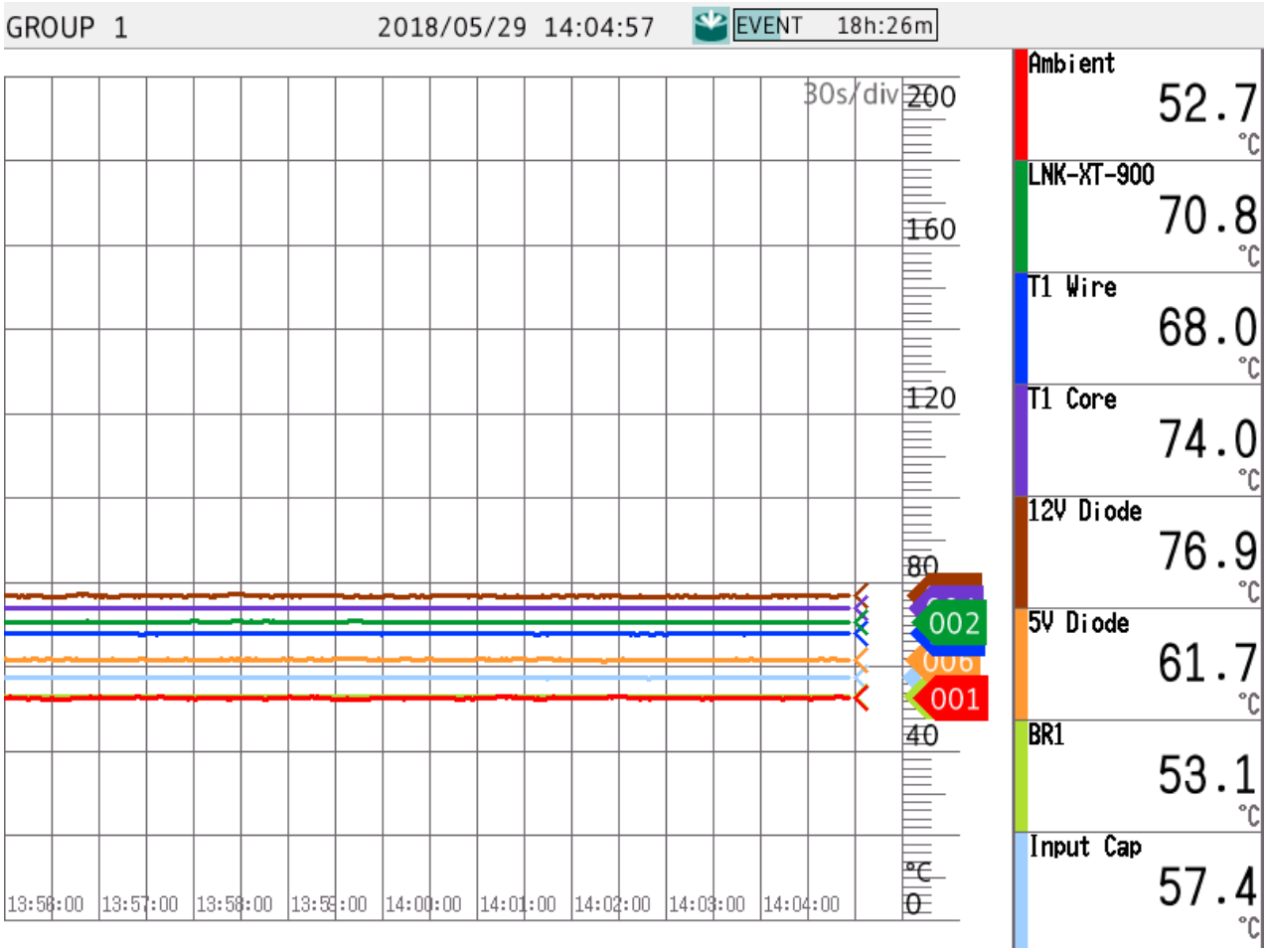

Figure 84 – Component Temperatures at 50 ºC Ambient.

12 Conducted EMI

12.1 EMI Equipment and Load

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture, model A662003.
5. Resistor load with input voltage set at 115 VAC.

12.2 Test Set-up

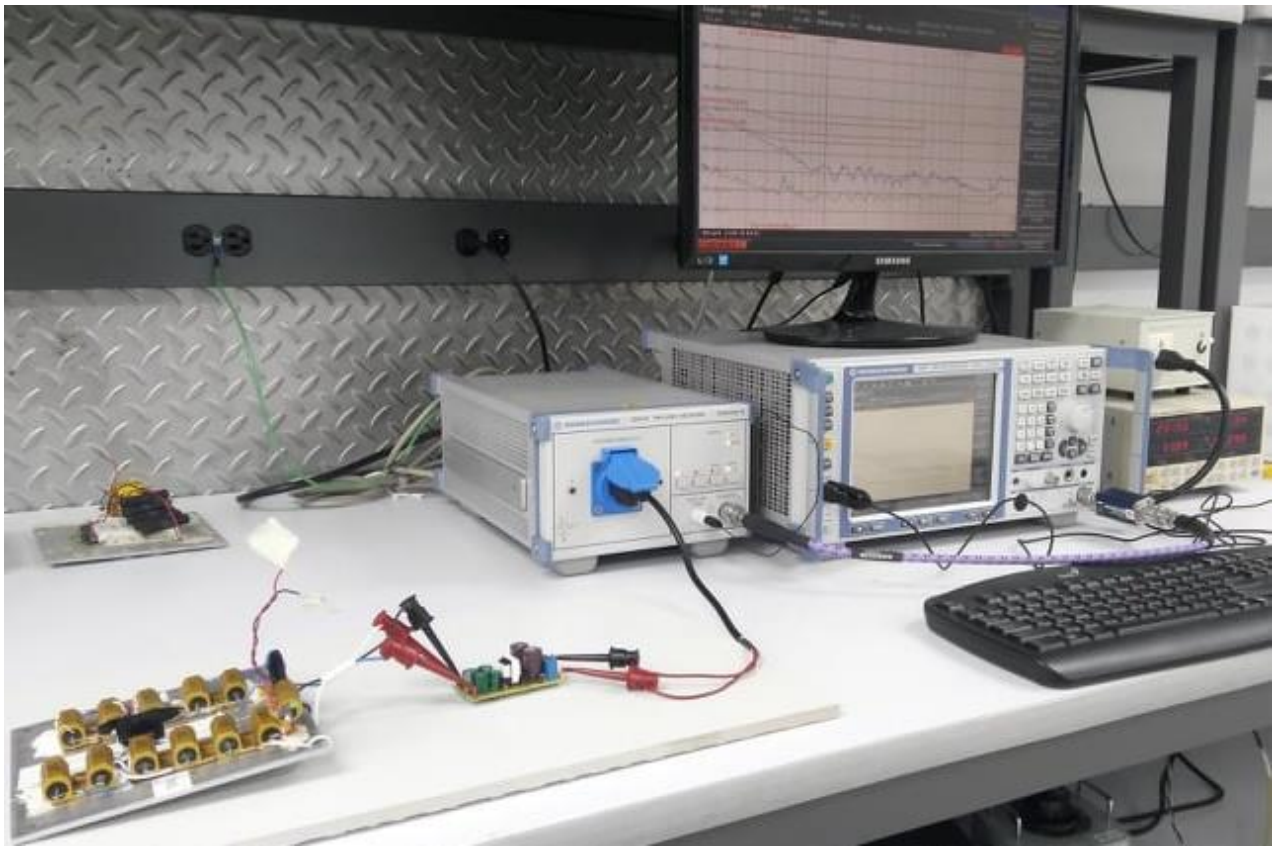

Figure 85 – Conducted EMI Test Set-up.

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12.3 **EMI Test Results**

12.3.1 *115 VAC, Floating Output*

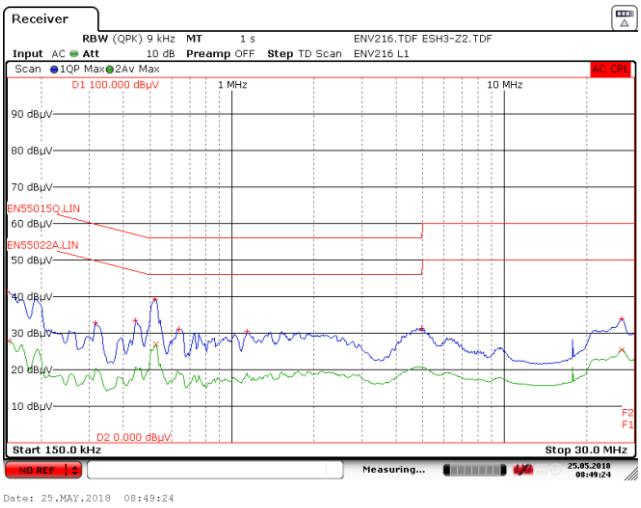

Figure 86 – Line.
Upper: Lowest Peak Delta Limit:
-16.63 dB, 523.50 kHz.
Lower: Lowest Average Delta Limit:
-19.13 dB, 525.75 kHz.

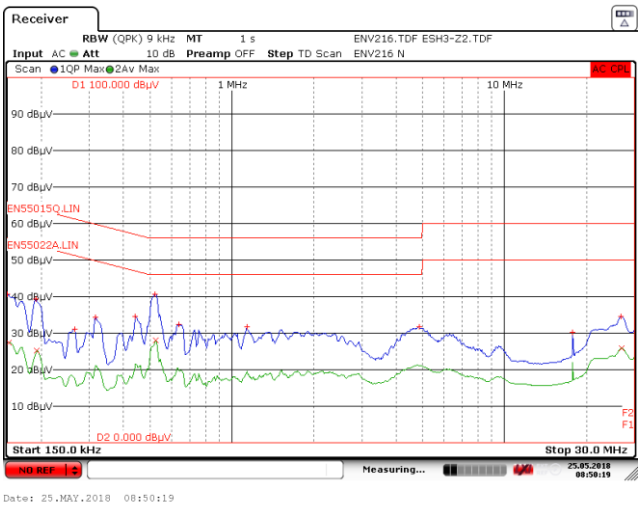

Figure 87 – Neutral.
Upper: Lowest Peak Delta Limit:
-15.29 dB, 523.50 kHz.
Lower: Lowest Average Delta Limit:
-18.03 dB, 525.75 kHz.

12.3.2 *230 VAC, Floating Output*

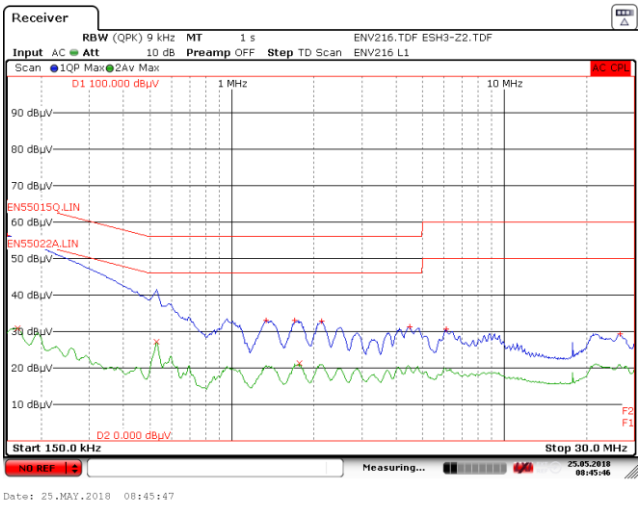

Figure 88 – Line.
Upper: Lowest Peak Delta Limit:
-9.80 dB, 150.00 kHz.
Lower: Lowest Average Delta Limit:
-18.92 dB, 530.25 kHz.

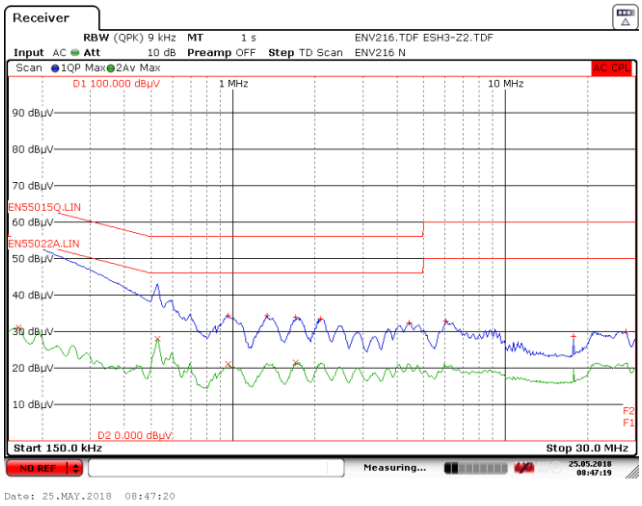

Figure 89 – Neutral.
Upper: Lowest Peak Delta Limit:
-9.93 dB, 150.00 kHz.
Lower: Lowest Average Delta Limit:
-17.99 dB, 530.25 kHz.

13 Line Surge

The unit was subject to ±2000 V, 100 kHz ring wave, and ±1000 V differential surge test using 10 strikes at each condition. A test failure is defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

13.1 Differential Surge Test

Surge Voltage (kV)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+1	0	L1 / L2	2	10	PASS
-1	0	L1 / L2	2	10	PASS
+1	90	L1 / L2	2	10	PASS
-1	90	L1 / L2	2	10	PASS
+1	180	L1 / L2	2	10	PASS
-1	180	L1 / L2	2	10	PASS
+1	270	L1 / L2	2	10	PASS
-1	270	L1 / L2	2	10	PASS

Note: In all PASS results, no damage and no auto-restart was observed.

13.2 Ring Wave Test

Ring Wave Voltage (kV)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+2	0	L1 / L2	12	10	PASS
-2	0	L1 / L2	12	10	PASS
+2	90	L1 / L2	12	10	PASS
-2	90	L1 / L2	12	10	PASS
+2	180	L1 / L2	12	10	PASS
-2	180	L1 / L2	12	10	PASS
+2	270	L1 / L2	12	10	PASS
-2	270	L1 / L2	12	10	PASS

Note: In all PASS results, no damage and no auto-restart was observed.

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14 Revision History

Date	Author	Revision	Description & Changes	Reviewed
26-Sep-18	IB & JPB	1.0	Initial Release.	Mktg & Apps
26-Oct-18	IB	1.1	Updated Section 8 Transformer Design Spreadsheet.	Mktg & Apps
30-Jun-20	KM	1.2	Updated Transformer Assembly Section. Converted to RDR	Mktg & Apps

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