

## Evaluating the **ADP7118/ADP7142** 20 V/40 V, 200 mA, Low Noise, CMOS LDOS

### FEATURES

Input voltage range for the **ADP7118**: 2.7 V to 20 V

Input voltage range for the **ADP7142**: 2.7 V to 40 V

Output current range: 0 mA to 200 mA

Output voltage accuracy:  $\pm 0.8\%$

Operating temperature range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

Adjustable option voltage set with two external resistors

$$V_{\text{OUT}} = 1.2 \text{ V} \times (1 + R1/R2)$$

### GENERAL DESCRIPTION

The **ADP7118/ADP7142** evaluation boards are used to demonstrate the functionality of the **ADP7118/ADP7142** series of linear regulators.

Simple device measurements such as line and load regulation, dropout, and ground current can be demonstrated with just a single voltage source, a voltmeter, an ammeter, and load resistors.

For more details on the **ADP7118** and **ADP7142** linear regulators, refer to the corresponding data sheets.

### EVALUATION BOARDS

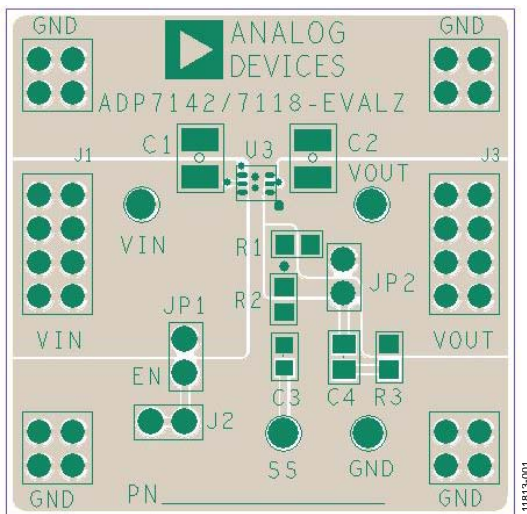


Figure 1. **ADP7118/ADP7142** LFCSP Evaluation Board

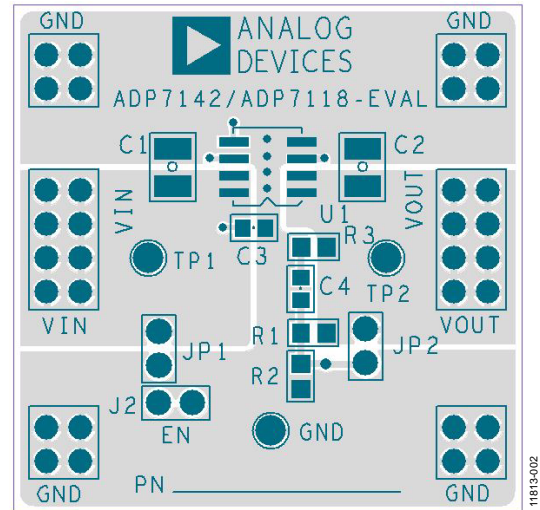


Figure 2. **ADP7118/ADP7142** TSOT Evaluation Board

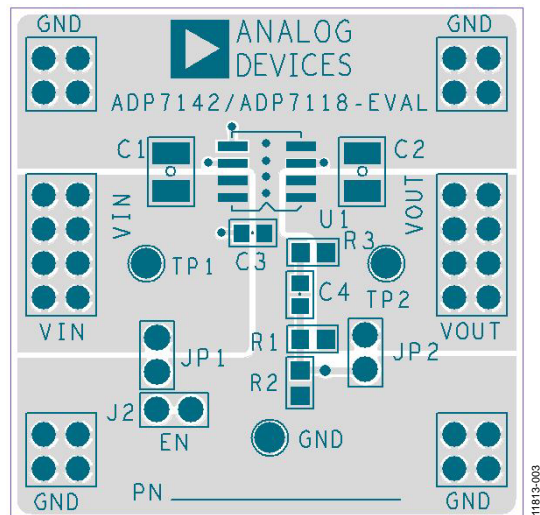


Figure 3. **ADP7118/ADP7142** SOIC Evaluation Board

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**REVISION HISTORY**

10/14—Revision 0: Initial Version

# EVALUATION BOARD HARDWARE AND SCHEMATIC

## EVALUATION BOARD CONFIGURATIONS

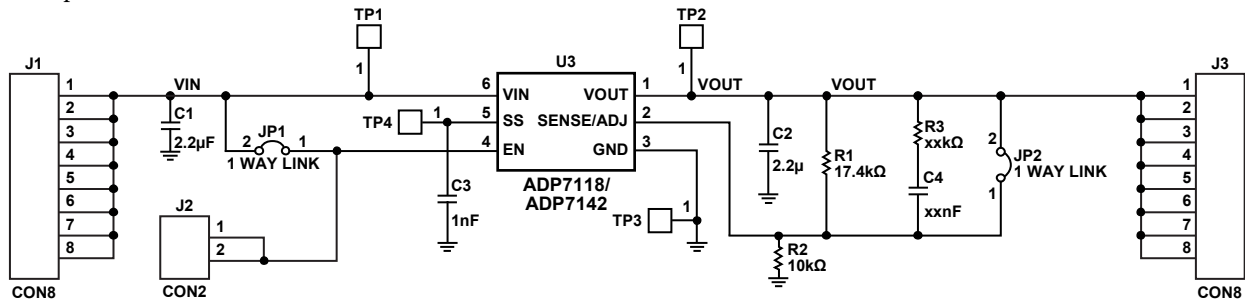
The [ADP7118/ADP7142](#) evaluation boards come supplied with different components depending on which package option is ordered. Components common to all package options are C1, C2, R1, R2, R3, JP1, and JP2. Resistor R1 and Resistor R2 are used only for the adjustable output option. The output voltage is set by

$$V_{OUT} = 1.2\text{ V} \times (1 + R1/R2)$$

Note that only the LFCSP and SOIC package options have the soft start capacitor, C3.

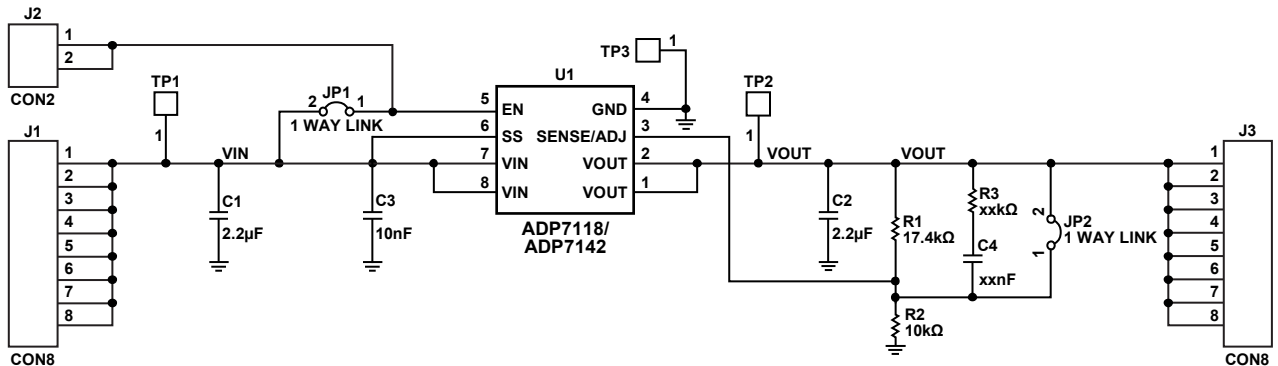
All three package options allow the use of the noise reduction network. The LFCSP and the SOIC use C4 and R3, while the TSOT uses C3 and R3.

Figure 4, Figure 5, and Figure 6 show the evaluation boards configuration schematics of the LFCSP, the SOIC, and the TSOT, respectively. The [ADP7142](#) can handle up to 40 V of input voltage, whereas the [ADP7118](#) can handle up to 20 V of input voltage.



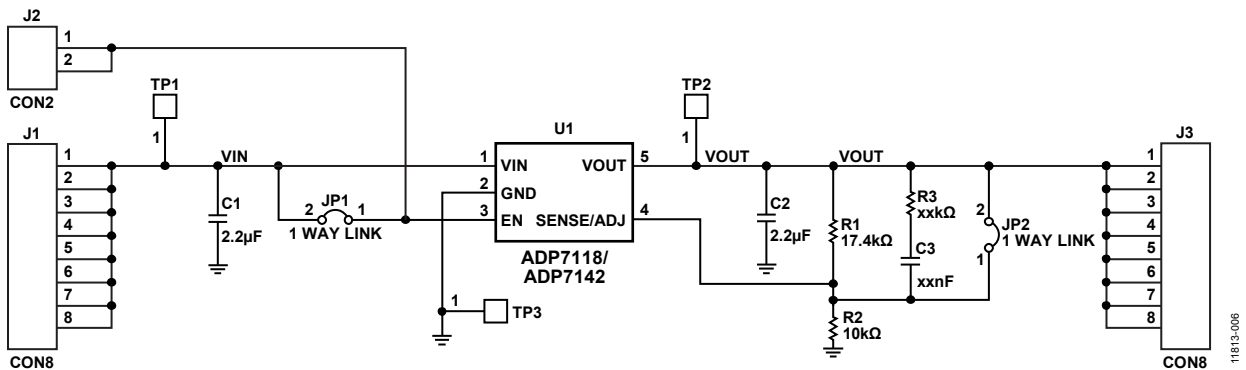
NOTES  
1. THE VALUES OF R3 AND C4 DEPEND ON THE LOW FREQUENCY ZERO OF THE NOISE REDUCTION NETWORK. SEE DATA SHEET FOR DESIGN DETAILS.

Figure 4. LFCSP Evaluation Board Schematic



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Figure 5. SOIC Evaluation Board Schematic



NOTES  
1. THE VALUES OF R3 AND C3 DEPEND ON THE LOW FREQUENCY ZERO OF THE NOISE REDUCTION NETWORK. SEE DATA SHEET FOR DESIGN DETAILS.

Figure 6. TSOT Evaluation Board Schematic

Table 1. Evaluation Board Hardware Components (LFCSP and SOIC)

Component	Function	Description
U1, U3 <sup>1</sup>	Linear regulator	ADP7118/ADP7142 are linear regulators.
C1	Input capacitor	C1 is a 2.2 $\mu$ F input bypass capacitor.
C2	Output capacitor	C2 is a 2.2 $\mu$ F output capacitor that is required for stability and transient performance.
C3	Soft start capacitor	C3 sets the soft start time to limit inrush current.
C4	Noise reduction capacitor	C4 is used with R3 for the noise reduction network.
R1	Output divider	R1 sets the output voltage to 3.3 V with R2 in the adjustable option. R2 = 17.4 k $\Omega$ .
R2	Output divider	R2 sets the output voltage to 3.3 V with R1 in the adjustable option. R1 = 10 k $\Omega$ .
R3	Noise reduction resistor	R3 is used with C4 for the noise reduction network.
JP1	Jumper	JP1 connects the EN pin to VIN for automatic startup.
JP2	Jumper	JP2 connects the SENSE/ADJ pin to output for fixed output options.

<sup>1</sup> Component varies depending on the type of evaluation board ordered.

Table 2. Evaluation Board Hardware Components (TSOT)

Component	Function	Description
U1 <sup>1</sup>	Linear regulator	ADP7118/ADP7142 are linear regulators.
C1	Input capacitor	C1 is a 2.2 $\mu$ F input bypass capacitor.
C2	Output capacitor	C2 is a 2.2 $\mu$ F output capacitor that is required for stability and transient performance.
C3	Noise reduction capacitor	C3 is used with R3 for the noise reduction network.
R1	Output divider	R1 sets the output voltage to 3.3 V with R2 in the adjustable option. R2 = 17.4 k $\Omega$ .
R2	Output divider	R2 sets the output voltage to 3.3 V with R1 in the adjustable option R1 = 10 k $\Omega$ .
R3	Noise reduction resistor	R3 is used with C3 for the noise reduction network.
JP1	Jumper	JP1 connects the EN pin to VIN for automatic startup.
JP2	Jumper	JP2 connects the SENSE/ADJ pin to output for fixed output options.

<sup>1</sup> Component varies depending on the type of evaluation board ordered.

## OUTPUT VOLTAGE MEASUREMENTS

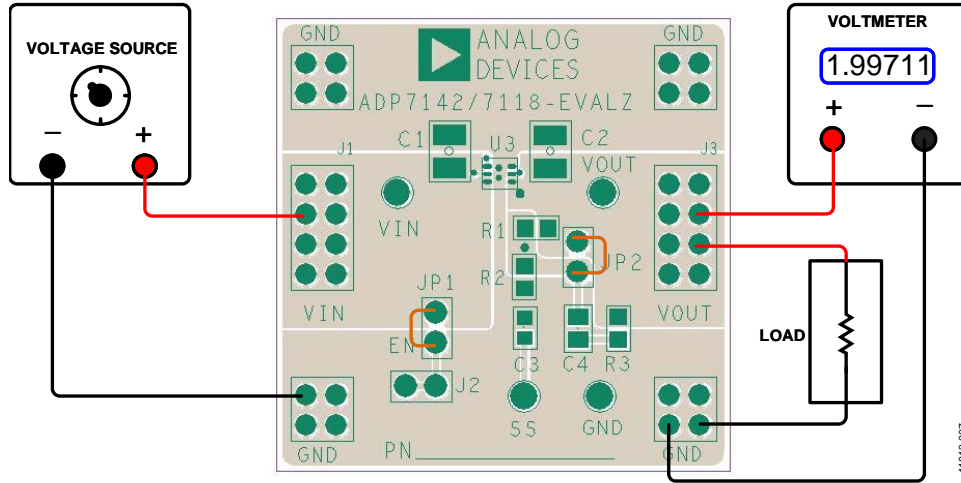


Figure 7. Output Voltage Measurement, LFCSP

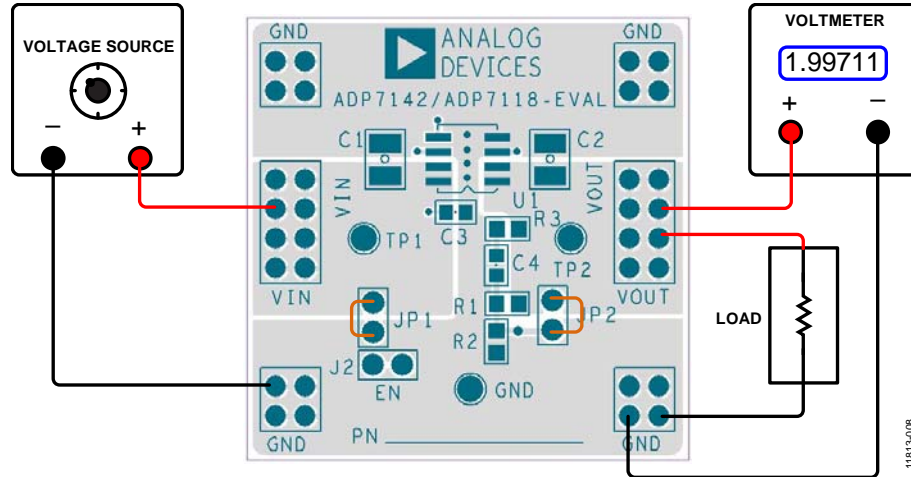


Figure 8. Output Voltage Measurement, SOIC

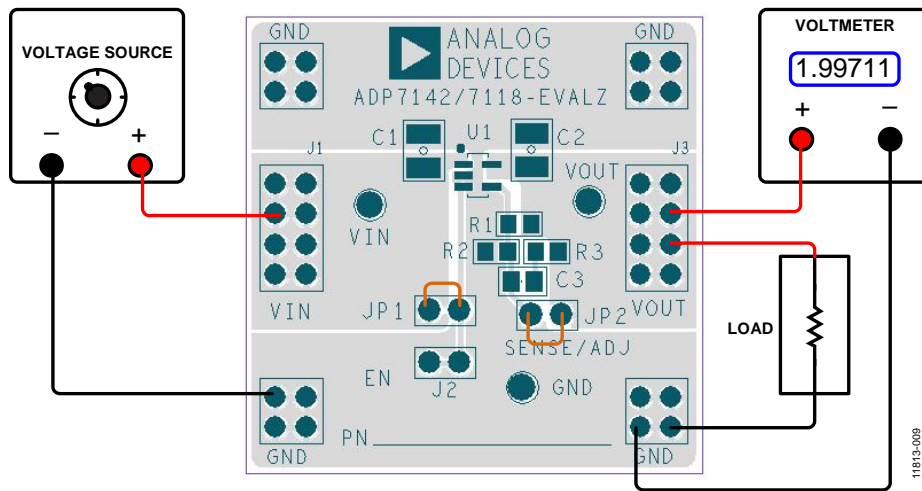


Figure 9. Output Voltage Measurement, TSOT

Figure 7, Figure 8, and Figure 9 show how the different evaluation boards can be connected to a voltage source and a voltmeter for basic output voltage accuracy measurements. A resistor can be used as the load for the regulator. Ensure that the

resistor has a power rating that can adequately handle the power expected to be dissipated across it. An electronic load can also be used as an alternative. Ensure that the voltage source can supply enough current for the expected load levels.

Use the following steps to connect the evaluation boards to a voltage source and voltmeter:

1. Connect the negative terminal (–) of the voltage source to one of the GND pads on the evaluation board.
2. Connect the positive terminal (+) of the voltage source to the VIN pad on the evaluation board.
3. Connect a load between the VOUT pad and one of the GND pads.
4. Connect the negative terminal (–) of the voltmeter to one of the GND pads.
5. Connect the positive terminal (+) on the voltmeter to the VOUT pad.

The voltage source can now be turned on. If J1 is inserted (connecting the EN pin to VIN for automatic startup), the regulator powers up.

If the load current is large, the user must connect the voltmeter as close as possible to the output capacitor to reduce the effects of IR drops.

**LINE REGULATION**

For line regulation measurements, the output of the regulator is monitored while the input of the regulator is varied. For good line regulation, the output must change as little as possible with varying input levels. To ensure that the device is not in dropout during this measurement,  $V_{IN}$  must be varied between  $V_{OUTNOM} + 1\text{ V}$  (or 2.7 V, whichever is greater) and  $V_{INMAX}$ . For example, for an ADP7142 with a 3.3 V output,  $V_{IN}$  must vary between 4.3 V and 40 V (20 V for the ADP7118). This measurement can be repeated under different load conditions. Figure 10 shows the typical line regulation performance of an ADP7142 with a 3.3 V output.

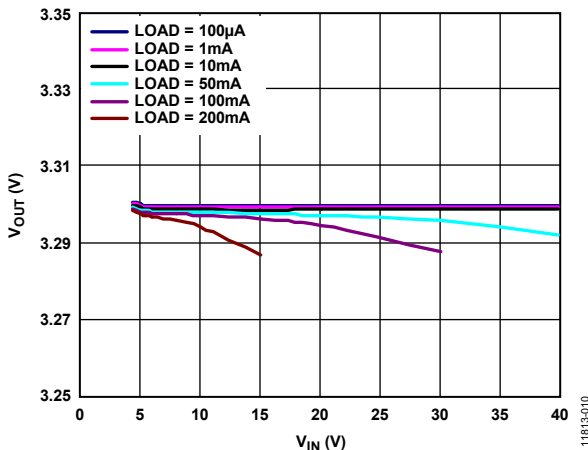


Figure 10. Output Voltage ( $V_{OUT}$ ) vs. Input Voltage ( $V_{IN}$ )

**LOAD REGULATION**

For load regulation measurements, the output of the regulator is monitored, while the load is varied. For good load regulation, the output must change as little as possible with varying loads. The input voltage must be held constant during this measurement. The load current can be varied from 0 mA to 200 mA. Figure 11 shows the typical load regulation performance of an ADP7142 with a 3.3 V output for an input voltage of 4.3 V.

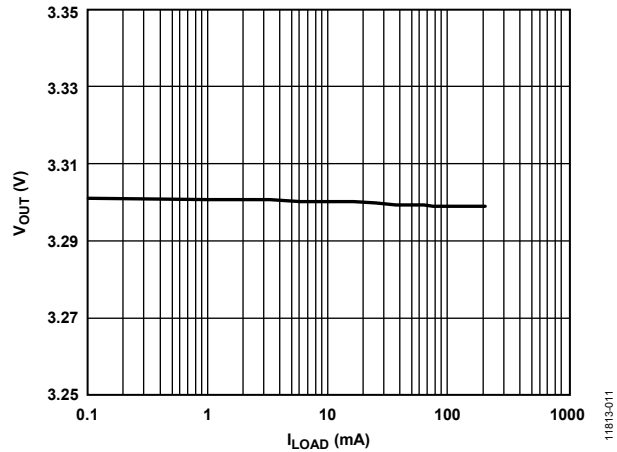


Figure 11. Output Voltage ( $V_{OUT}$ ) vs. Load Current ( $I_{LOAD}$ )

**DROPOUT VOLTAGE**

Dropout voltage can be measured using the configuration shown in Figure 7. Dropout voltage is defined as the input to output voltage differential when the input voltage is set to the nominal output voltage. Dropout voltage applies only for output voltages greater than 2.8 V. Dropout voltage increases with larger loads. For more accurate measurements, a second voltmeter can be used to monitor the input voltage across the input capacitor. The input supply voltage may need to be adjusted to account for IR drops, especially if large load currents are used. Figure 12 shows a typical curve of dropout voltage measurements with different load currents.

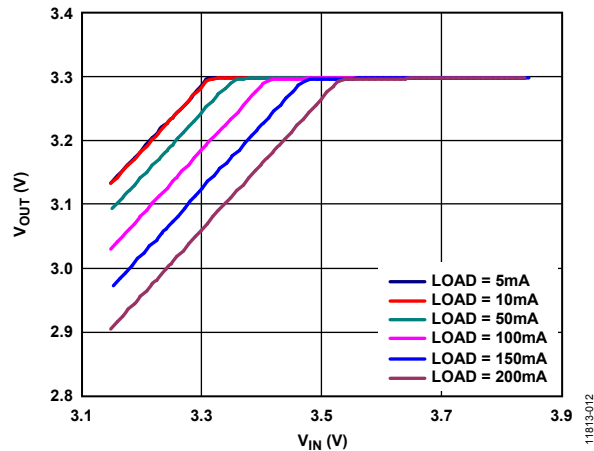


Figure 12. Output Voltage ( $V_{OUT}$ ) in Dropout vs. Load Current ( $I_{LOAD}$ )



# GROUND CURRENT MEASUREMENT

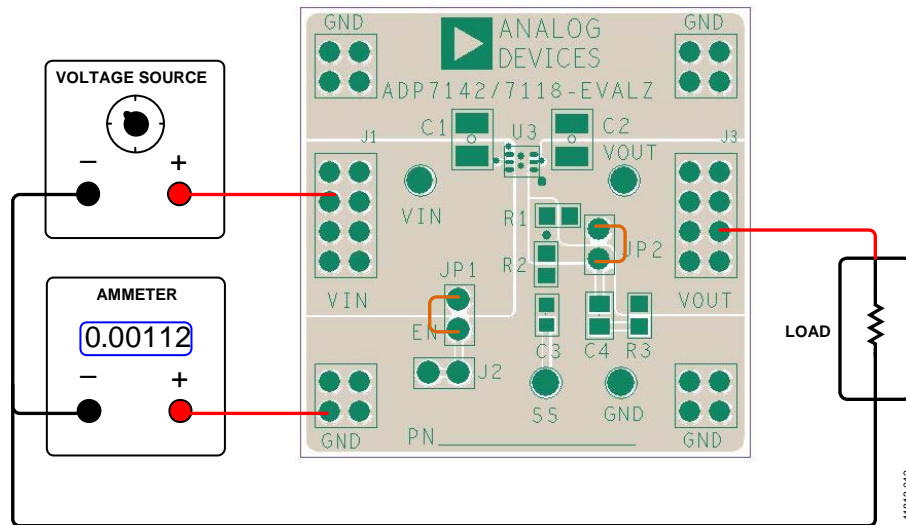


Figure 13. Ground Current Measurement, LFCSP

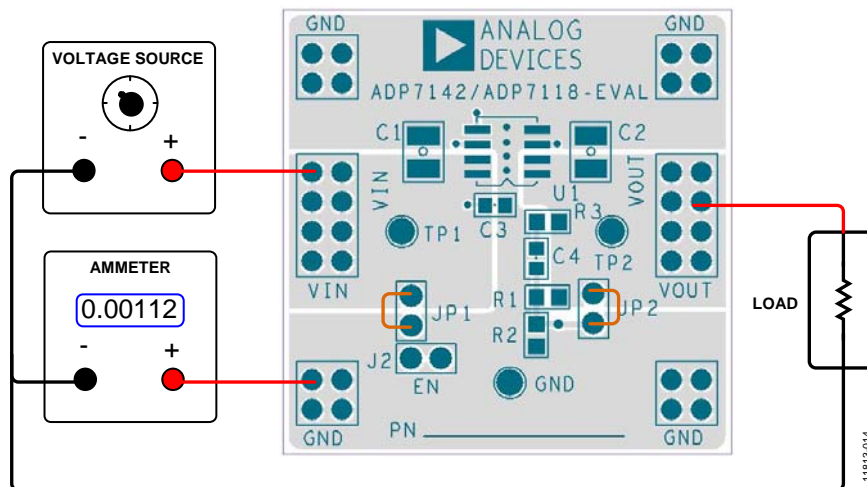


Figure 14. Ground Current Measurement, SOIC

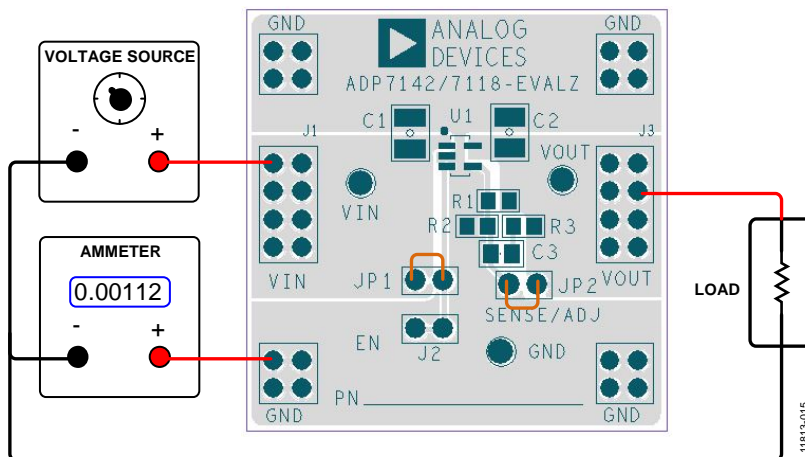


Figure 15. Ground Current Measurement, TSOT

Figure 13, Figure 14, and Figure 15 show how the evaluation boards can be connected to a voltage source and an ammeter for ground current measurements. A resistor can be used as the load for the regulator. Ensure that the resistor has a power rating that can adequately handle the power expected to be dissipated across it. An electronic load can be used as an alternative. Ensure that the voltage source used can supply enough current for the expected load levels.

Use the following steps to connect the evaluation boards to a voltage source and an ammeter:

1. Connect the positive terminal (+) of the voltage source to the VIN pad on the evaluation board.
2. Connect the positive terminal (+) of the ammeter to one of the GND pads of the evaluation board.
3. Connect the negative terminal (-) of the ammeter to the negative (-) terminal of the voltage source.
4. Connect a load between the negative (-) terminal of the voltage source and the VOUT pad of the evaluation board.

The voltage source can now be turned on. If J1 is inserted (connecting the EN pin to VIN for automatic startup), the regulator powers up.

## GROUND CURRENT CONSUMPTION

Ground current measurements can determine how much current the internal circuits of the regulator are consuming while the circuits perform the regulation function. To be efficient, the regulator needs to consume as little current as possible. The regulator typically uses the maximum current when supplying its largest load level (200 mA). Figure 16 shows the typical ground current consumption vs. load current at an input voltage of 6 V for an output voltage of 3.3 V.

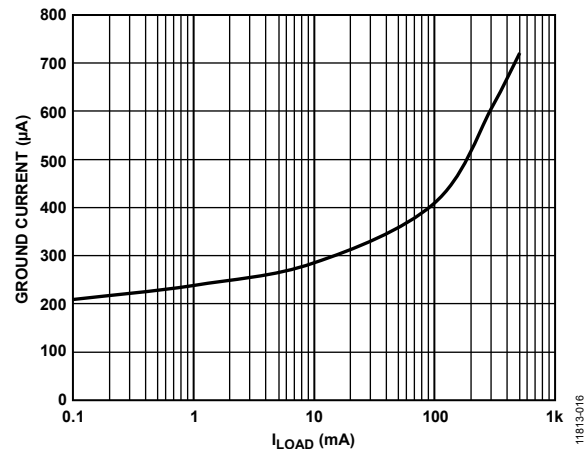


Figure 16. Ground Current vs. Load Current ( $I_{LOAD}$ )

When the device is disabled (EN = GND), the ground current drops to less than 1  $\mu$ A.



## ORDERING INFORMATION

### BILL OF MATERIALS

Table 3. SOIC and LFCSP Bill of Materials

Quantity	Reference Designator	Description	Manufacturer/Vendor	Vendor Part Number
1	U1, U3 <sup>1</sup>	ADP7118 or ADP7142	Analog Devices, Inc.	ADP7118CP or ADP7142CP
2	C1, C2	Capacitors, MLCC, 2.2 $\mu$ F, 100 V, 1210, X7R	Murata (or equivalent)	GRM32ER72A225KA35
1	C3 (not installed)	Capacitor, MLCC, 0805 case	Not applicable	Not applicable
1	C4 (not installed)	Capacitor, MLCC, 0805 case	Not applicable	Not applicable
2	JP1, JP2	Header, single, 2 pins	Sullins Connector Solutions	PEC02SAAN
1	R1	Resistor, 1%, 0805 case, 17.4 k $\Omega$	Vishay Dale or equivalent	CRCW080517K4FKEA
1	R2	Resistor, 1%, 0805 case, 10 k $\Omega$	Vishay Dale or equivalent	CRCW080510K0FKEA
1	R3 (not installed)	Resistor, 1%, 0805 case	Not applicable	Not applicable

<sup>1</sup> Component varies depending on the type of evaluation board ordered.

Table 4. TSOT Bill of Materials

Quantity	Reference Designator	Description	Manufacturer/Vendor	Vendor Part Number
1	U1 <sup>1</sup>	ADP7118 or ADP7142	Analog Devices, Inc.	ADP7118CP or ADP7142CP
2	C1, C2	Capacitors, MLCC, 2.2 $\mu$ F, 100 V, 1210, X7R	Murata (or equivalent)	GRM32ER72A225KA35
1	C3 (not installed)	Capacitor, MLCC, 0805 case	Not applicable	Not applicable
2	JP1, JP2	Header, single, 2 pins	Sullins Connector Solutions	PEC02SAAN
1	R1	Resistor, 1%, 0805 case, 17.4 k $\Omega$	Vishay Dale or equivalent	CRCW080517K4FKEA
1	R2	Resistor, 1%, 0805 case, 10 k $\Omega$	Vishay Dale or equivalent	CRCW080510K0FKEA
1	R3 (not installed)	Resistor, 1%, 0805 case	Not applicable	Not applicable

<sup>1</sup> Component varies depending on the type of evaluation board ordered.



#### ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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