# XS1-L02A-QF124 Datasheet

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It is our intention to provide you with accurate and comprehensive documentation for the hardware and software components used in this product. To subscribe to receive updates, visit http://www.xmos.com/.

# 1 Features

▶ **Dual-Tile Multicore Microcontroller with Advanced Multi-Core RISC Architecture**
  ● Up to 1000 MIPS shared between up to 16 real-time logical cores
  ● Each logical core has:
    — Guaranteed throughput of between $1/4$ and $1/8$ of tile MIPS
    — 16x32bit dedicated registers
  ● 159 high-density 16/32-bit instructions
    — All have single clock-cycle execution (except for divide)
    — 32x32→64-bit MAC instructions for DSP, arithmetic and user-definable cryptographic functions

▶ **Programmable I/O**
  ● 84 general-purpose I/O pins, configurable as input or output
  ● Port sampling rates of up to 60 MHz with respect to an external clock
  ● 64 channel ends for communication with other cores, on or off-chip

▶ **Memory**
  ● 128KB internal single-cycle SRAM (max 64KB per tile) for code and data storage
  ● 16KB internal OTP (max 8KB per tile) for application boot code

▶ **JTAG Module for On-Chip Debug**

▶ **Security Features**
  ● Programming lock disables debug and prevents read-back of memory contents
  ● AES bootloader ensures secrecy of IP held on external flash memory

▶ **Ambient Temperature Range**
  ● Commercial qualification: 0 °C to 70 °C
  ● Industrial qualification: -40 °C to 85 °C
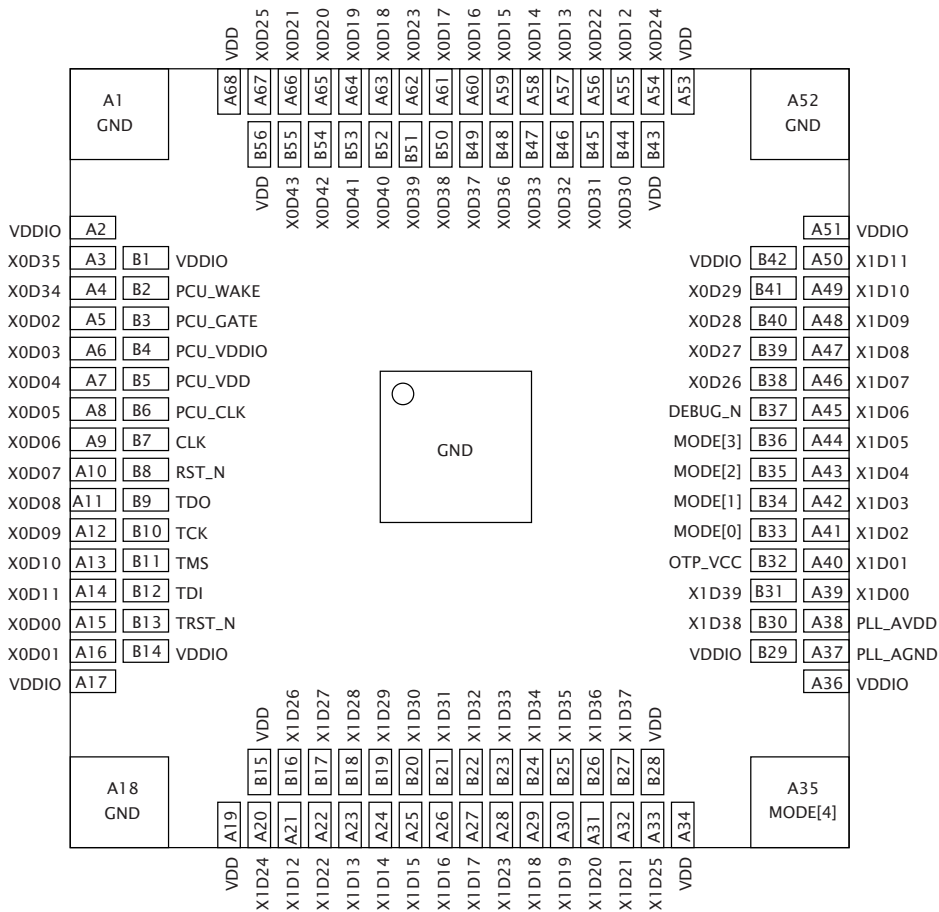
▶ **Speed Grade**
  ● 5: 500 MIPS
  ● 4: 400 MIPS

▶ **Power Consumption**
  ● Active Mode
    — 400 mA at 500 MHz (typical)
    — 320 mA at 400 MHz (typical)
  ● Standby Mode
    — 28 mA
  ● Sleep Mode
    — Programmable PCU module puts device into sleep mode
    — Wakeup on external signal or timeout

▶ **124-pin dual-row QFN package 0.5 mm pitch**

## 2  Pin Configuration

# 3 Signal Description

| Module | Signal | Function | Type | Active | Properties |
|---|---|---|---|---|---|
| | | PU=Pull Up, PD=Pull Down, ST=Schmitt Trigger Input, OT=Output Tristate, S=Switchable | | | |
| | | $R_S$=Required for SPI boot (§5.6), $R_U$=Required for USB-enabled devices (§10) | | | |
| Power | GND | Digital ground | GND | — | |
| | VDD | Digital tile power | PWR | — | |
| | VDDIO | Digital I/O power | PWR | — | |
| | PLL_AGND | Analog ground for PLL | PWR | — | |
| | PLL_AVDD | Analog PLL power | PWR | — | |
| | PCU_VDD | PCU tile power | PWR | — | |
| | PCU_VDDIO | PCU I/O supply | PWR | — | |
| | OTP_VCC | OTP power supply | PWR | — | |
| | RST_N | Global reset input | Input | Low | |
| PLL | CLK | PLL reference clock | Input | — | PD, ST |
| | MODE[4:0] | Boot mode select | Input | — | PU, ST |
| JTAG | TDI | Test data input | Input | — | PU, ST |
| | TDO | Test data output | Output | — | PD, OT |
| | TMS | Test mode select | Input | — | PU, ST |
| | TRST_N | Test reset input | Input | Low | |
| | TCK | Test clock | Input | — | PU, ST |
| | DEBUG_N | Multi-chip debug | I/O | Low | PU |
| PCU | PCU_WAKE | Wakeup reset | Input | — | PD, ST |
| | PCU_GATE | Power control gate control | Output | — | OT |
| | PCU_CLK | Clock input | Input | — | PD, ST |
| Tile 0 I/O | X0D00 | $P1A^0$ | I/O | — | $PD_S$, $R_S$ |
| | X0D01 | $XLA_{5b}^{4o}$ $P1B^0$ | I/O | — | $PD_S$, $R_S$ |
| | X0D02 | $XLA_{5b}^{3o}$ $P4A^0$ $P8A^0$ $P16A^0$ $P32A^{20}$ | I/O | — | $PD_S$, $R_U$ |
| | X0D03 | $XLA_{5b}^{2o}$ $P4A^1$ $P8A^1$ $P16A^1$ $P32A^{21}$ | I/O | — | $PD_S$, $R_U$ |
| | X0D04 | $XLA_{2b/5b}^{1o}$ $P4B^0$ $P8A^2$ $P16A^2$ $P32A^{22}$ | I/O | — | $PD_S$, $R_U$ |
| | X0D05 | $XLA_{2b/5b}^{0o}$ $P4B^1$ $P8A^3$ $P16A^3$ $P32A^{23}$ | I/O | — | $PD_S$, $R_U$ |
| | X0D06 | $XLA_{2b/5b}^{0i}$ $P4B^2$ $P8A^4$ $P16A^4$ $P32A^{24}$ | I/O | — | $PD_S$, $R_U$ |
| | X0D07 | $XLA_{2b/5b}^{1i}$ $P4B^3$ $P8A^5$ $P16A^5$ $P32A^{25}$ | I/O | — | $PD_S$, $R_U$ |
| | X0D08 | $XLA_{5b}^{2i}$ $P4A^2$ $P8A^6$ $P16A^6$ $P32A^{26}$ | I/O | — | $PD_S$, $R_U$ |
| | X0D09 | $XLA_{5b}^{3i}$ $P4A^3$ $P8A^7$ $P16A^7$ $P32A^{27}$ | I/O | — | $PD_S$, $R_U$ |
| | X0D10 | $XLA_{5b}^{4i}$ $P1C^0$ | I/O | — | $PD_S$, $R_S$ |
| | X0D11 | $P1D^0$ | I/O | — | $PD_S$, $R_S$ |
| | X0D12 | $P1E^0$ | I/O | — | $PD_S$, $R_U$ |
| | X0D13 | $XLB_{5b}^{4o}$ $P1F^0$ | I/O | — | $PD_S$, $R_U$ |
| | X0D14 | $XLB_{5b}^{3o}$ $P4C^0$ $P8B^0$ $P16A^8$ $P32A^{28}$ | I/O | — | $PD_S$, $R_U$ |
| | X0D15 | $XLB_{5b}^{2o}$ $P4C^1$ $P8B^1$ $P16A^9$ $P32A^{29}$ | I/O | — | $PD_S$, $R_U$ |
| | X0D16 | $XLB_{2b/5b}^{1o}$ $P4D^0$ $P8B^2$ $P16A^{10}$ | I/O | — | $PD_S$, $R_U$ |
| | X0D17 | $XLB_{2b/5b}^{0o}$ $P4D^1$ $P8B^3$ $P16A^{11}$ | I/O | — | $PD_S$, $R_U$ |

(continued)

| Module | Name | Function | | | | Type | Active | Properties |
|---|---|---|---|---|---|---|---|---|
| Tile 0 I/O | X0D18 | $XLB^{0i}_{2b/5b}$ | $P4D^2$ $P8B^4$ $P16A^{12}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D19 | $XLB^{1i}_{2b/5b}$ | $P4D^3$ $P8B^5$ $P16A^{13}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D20 | $XLB^{2i}_{5b}$ | $P4C^2$ $P8B^6$ $P16A^{14}$ $P32A^{30}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D21 | $XLB^{3i}_{5b}$ | $P4C^3$ $P8B^7$ $P16A^{15}$ $P32A^{31}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D22 | $XLB^{4i}_{5b}$ | $P1G^0$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D23 | $P1H^0$ | | | | I/O | — | $PD_S$, $R_U$ |
| | X0D24 | $P1I^0$ | | | | I/O | — | $PD_S$ |
| | X0D25 | $P1J^0$ | | | | I/O | — | $PD_S$ |
| | X0D26 | | $P4E^0$ $P8C^0$ $P16B^0$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D27 | | $P4E^1$ $P8C^1$ $P16B^1$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D28 | | $P4F^0$ $P8C^2$ $P16B^2$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D29 | | $P4F^1$ $P8C^3$ $P16B^3$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D30 | | $P4F^2$ $P8C^4$ $P16B^4$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D31 | | $P4F^3$ $P8C^5$ $P16B^5$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D32 | | $P4E^2$ $P8C^6$ $P16B^6$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D33 | | $P4E^3$ $P8C^7$ $P16B^7$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D34 | $P1K^0$ | | | | I/O | — | $PD_S$ |
| | X0D35 | $P1L^0$ | | | | I/O | — | $PD_S$ |
| | X0D36 | $P1M^0$ | $P8D^0$ $P16B^8$ | | | I/O | — | $PD_S$ |
| | X0D37 | $P1N^0$ | $P8D^1$ $P16B^9$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D38 | $P1O^0$ | $P8D^2$ $P16B^{10}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D39 | $P1P^0$ | $P8D^3$ $P16B^{11}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D40 | | $P8D^4$ $P16B^{12}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D41 | | $P8D^5$ $P16B^{13}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D42 | | $P8D^6$ $P16B^{14}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X0D43 | | $P8D^7$ $P16B^{15}$ | | | I/O | — | $PU_S$, $R_U$ |
| Tile 1 I/O | X1D00 | | $P1A^0$ | | | I/O | — | $PD_S$ |
| | X1D01 | $XLA^{4o}_{5b}$ | $P1B^0$ | | | I/O | — | $PD_S$ |
| | X1D02 | $XLA^{3o}_{5b}$ | $P4A^0$ $P8A^0$ $P16A^0$ $P32A^{20}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X1D03 | $XLA^{2o}_{5b}$ | $P4A^1$ $P8A^1$ $P16A^1$ $P32A^{21}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X1D04 | $XLA^{1o}_{2b/5b}$ | $P4B^0$ $P8A^2$ $P16A^2$ $P32A^{22}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X1D05 | $XLA^{0o}_{2b/5b}$ | $P4B^1$ $P8A^3$ $P16A^3$ $P32A^{23}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X1D06 | $XLA^{0i}_{2b/5b}$ | $P4B^2$ $P8A^4$ $P16A^4$ $P32A^{24}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X1D07 | $XLA^{1i}_{2b/5b}$ | $P4B^3$ $P8A^5$ $P16A^5$ $P32A^{25}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X1D08 | $XLA^{2i}_{5b}$ | $P4A^2$ $P8A^6$ $P16A^6$ $P32A^{26}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X1D09 | $XLA^{3i}_{5b}$ | $P4A^3$ $P8A^7$ $P16A^7$ $P32A^{27}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X1D10 | $XLA^{4i}_{5b}$ | $P1C^0$ | | | I/O | — | $PD_S$ |
| | X1D11 | | $P1D^0$ | | | I/O | — | $PD_S$ |
| | X1D12 | | $P1E^0$ | | | I/O | — | $PD_S$, $R_U$ |
| | X1D13 | $XLB^{4o}_{5b}$ | $P1F^0$ | | | I/O | — | $PD_S$, $R_U$ |
| | X1D14 | $XLB^{3o}_{5b}$ | $P4C^0$ $P8B^0$ $P16A^8$ $P32A^{28}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X1D15 | $XLB^{2o}_{5b}$ | $P4C^1$ $P8B^1$ $P16A^9$ $P32A^{29}$ | | | I/O | — | $PD_S$, $R_U$ |
| | X1D16 | $XLB^{1o}_{2b/5b}$ | $P4D^0$ $P8B^2$ $P16A^{10}$ | | | I/O | — | $PD_S$, $R_U$ |

(continued)

| Module | Name | Function | Type | Active | Properties |
|---|---|---|---|---|---|
| Tile 1 I/O | X1D17 | $XLB^{0o}_{2b/5b}$ $\quad$ P4D$^1$ P8B$^3$ P16A$^{11}$ | I/O | — | PD$_S$, R$_U$ |
| | X1D18 | $XLB^{0i}_{2b/5b}$ $\quad$ P4D$^2$ P8B$^4$ P16A$^{12}$ | I/O | — | PD$_S$, R$_U$ |
| | X1D19 | $XLB^{1i}_{2b/5b}$ $\quad$ P4D$^3$ P8B$^5$ P16A$^{13}$ | I/O | — | PD$_S$, R$_U$ |
| | X1D20 | $XLB^{2i}_{5b}$ $\quad$ P4C$^2$ P8B$^6$ P16A$^{14}$ P32A$^{30}$ | I/O | — | PD$_S$, R$_U$ |
| | X1D21 | $XLB^{3i}_{5b}$ $\quad$ P4C$^3$ P8B$^7$ P16A$^{15}$ P32A$^{31}$ | I/O | — | PD$_S$, R$_U$ |
| | X1D22 | $XLB^{4i}_{5b}$ $\quad$ P1G$^0$ | I/O | — | PD$_S$, R$_U$ |
| | X1D23 | P1H$^0$ | I/O | — | PD$_S$, R$_U$ |
| | X1D24 | P1I$^0$ | I/O | — | PD$_S$ |
| | X1D25 | P1J$^0$ | I/O | — | PD$_S$ |
| | X1D26 | P4E$^0$ P8C$^0$ P16B$^0$ | I/O | — | PD$_S$, R$_U$ |
| | X1D27 | P4E$^1$ P8C$^1$ P16B$^1$ | I/O | — | PD$_S$, R$_U$ |
| | X1D28 | P4F$^0$ P8C$^2$ P16B$^2$ | I/O | — | PD$_S$, R$_U$ |
| | X1D29 | P4F$^1$ P8C$^3$ P16B$^3$ | I/O | — | PD$_S$, R$_U$ |
| | X1D30 | P4F$^2$ P8C$^4$ P16B$^4$ | I/O | — | PD$_S$, R$_U$ |
| | X1D31 | P4F$^3$ P8C$^5$ P16B$^5$ | I/O | — | PD$_S$, R$_U$ |
| | X1D32 | P4E$^2$ P8C$^6$ P16B$^6$ | I/O | — | PD$_S$, R$_U$ |
| | X1D33 | P4E$^3$ P8C$^7$ P16B$^7$ | I/O | — | PD$_S$, R$_U$ |
| | X1D34 | P1K$^0$ | I/O | — | PD$_S$ |
| | X1D35 | P1L$^0$ | I/O | — | PD$_S$ |
| | X1D36 | P1M$^0$ $\quad$ P8D$^0$ P16B$^8$ | I/O | — | PD$_S$ |
| | X1D37 | P1N$^0$ $\quad$ P8D$^1$ P16B$^9$ | I/O | — | PD$_S$, R$_U$ |
| | X1D38 | P1O$^0$ $\quad$ P8D$^2$ P16B$^{10}$ | I/O | — | PD$_S$, R$_U$ |
| | X1D39 | P1P$^0$ $\quad$ P8D$^3$ P16B$^{11}$ | I/O | — | PD$_S$, R$_U$ |

# 4 Block Diagram

X0D00 X0D01 X0D02 X0D03 X0D04 X0D05 X0D06 X0D07 X0D08 X0D09 X0D10 X0D11 X0D12 X0D13 X0D14 X0D15 X0D16 X0D17 X0D18 X0D19 X0D20 X0D21 X0D22 X0D23 X0D24 X0D25 X0D26 X0D27 X0D28 X0D29 X0D30 X0D31 X0D32 X0D33 X0D34 X0D35 X0D36 X0D37 X0D38 X0D39 X0D40 X0D41 X0D42 X0D43

1A 1B 4A Port 4B Port 8A 4A XLA
1C 1D 1E 1F 4C Port 4D Port 8B 4C XLB
1G 1H 1I 1J 4E Port 4F Port 8C 4E
1K 1L 1M 1N 1O 1P Port 8D

Port 16A Port 16B

Core 0 Core 1 Core 2 Core 3 Core 4 Core 5 Core 6 Core 7

32 Channel Ends Switch

XLE XLH XLF XLG XLG XLF XLH XLE

Switch 32 Channel Ends

Core 0 Core 1 Core 2 Core 3 Core 4 Core 5 Core 6 Core 7

Port 16A Port 16B

Port 8A 4A Port 4B 4A XLA
1A 1B 1C 1D 1E 1F
Port 8B 4C Port 4D 4C XLB
1G 1H 1I 1J
Port 8C 4E Port 4F 4E
Port 8D 1K 1L 1M 1N 1O 1P

X1D00 X1D01 X1D02 X1D03 X1D08 X1D09 X1D04 X1D05 X1D06 X1D07 X1D10 X1D11 X1D12 X1D13 X1D14 X1D15 X1D20 X1D21 X1D16 X1D17 X1D18 X1D19 X1D22 X1D23 X1D24 X1D25 X1D26 X1D27 X1D32 X1D33 X1D28 X1D29 X1D30 X1D31 X1D34 X1D35 X1D36 X1D37 X1D38 X1D39

6 Clock Blocks
10 Timers
4 Locks
7 Synchronizers

64KB SRAM

64KB SRAM

6 Clock Blocks
10 Timers
4 Locks
7 Synchronizers

TDI
TCK
TMS
TRST_N
DEBUG_N

JTAG

JTAG

TDO

PLL_AVDD
PLL_AGND
CLK
RST_N
MODE[4:0]
PCU_WAKE
PCU_GATE
PCU_CLK
PCU_VDD
PCU_VDDIO
OTP_VCC
VDD
VDDIO
GND

PLL

Boot ROM

Boot ROM

PLL

PCU

Security Register

8KB OTP

Security Register

8KB OTP

X0 X1

XMOS®

# 5   Product Overview

The XMOS XS1-L02A-QF124 is a powerful device that provides a simple design process and highly-flexible solution to many applications. The device consists of two xCORE Tiles, each comprising a flexible multicore microcontroller with tightly integrated I/O and on-chip memory. The processors run mutiple tasks simultaneously using logical cores, each of which is guaranteed a slice of processing power and can execute computational code, control software and I/O interfaces. Logical cores use channels to exchange data within a tile or across tiles. The tiles are connected via an integrated switch network, which uses a proprietary physical layer protocol, and which can also be used to add additional resources to a design. The I/O pins are driven using intelligent ports that can serialize data, interpret strobe signals and wait for scheduled times or events, making the device ideal for real-time control applications.

The device can be configured using a set of software components that are rapidly customized and composed. XMOS provides source code libraries for many standard components. The device can be programmed using high-level languages such as C/C++ and XMOS-originated extensions to C, called XC, that simplify the control over concurrency, I/O and time.

The XMOS toolchain includes compilers, a simulator, debugger and static timing analyzer. The combination of real-time software, a compiler and timing analyzer enables the programmer to close timings on components of the design without a detailed understanding of the hardware characteristics.

## 5.1   Logical cores, Synchronizers and Locks

Each xCORE Tile has up to eight active logical cores, which issue instructions down a shared four-stage pipeline. Instructions from the active cores are issued round-robin. If up to four logical cores are active, each core is allocated a quarter of the processing cycles. If more than four logical cores are active, each core is allocated at least $1/n$ cycles (for $n$ cores). Figure 1 shows the guaranteed core performance depending on the number of cores used.

**Figure 1:**
Core
performance

| Speed Grade | Minimum MIPS per core (for *n* cores) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 400 MHz | 100 | 100 | 100 | 100 | 80 | 67 | 57 | 50 |
| 500 MHz | 125 | 125 | 125 | 125 | 100 | 83 | 71 | 63 |

There is no way that the performance of a logical core can be reduced below these predicted levels. Because cores may be delayed on I/O, however, their unused processing cycles can be taken by other cores. This means that for more than four logical cores, the performance of each core is often higher than the predicted minimum.

## 5.2   Channel Ends, Links and Switch

Logical cores communicate using point-to-point connections formed between two channel ends. Between tiles, channel communications are implemented over xConnect Links and routed through switches. The links operate in either 2bit/direction or 5bit/direction mode, depending on the amount of bandwidth required. Circuit switched, streaming and packet switched data can both be supported efficiently. Streams provide the fastest possible data rates between xCORE Tiles (up to 250 MBit/s), but each stream requires a single link to be reserved between switches on two tiles. All packet communications can be multiplexed onto a single link.

Information on the supported routing topologies that can be used to connect multiple devices together can be found in the XS1-L Link Performance and Design Guide, X2999.

## 5.3   Ports and Clock Blocks

Ports provide an interface between the logical cores and I/O pins. All pins of a port provide either output or input. Signals in different directions cannot be mapped onto the same port.

The operation of each port is synchronized to a clock block. A clock block can be connected to an external clock input, or it can be run from the divided reference clock. A clock block can also output its signal to a pin. On reset, each port is connected to clock block 0, which runs from the xCORE Tile reference clock.

The ports and links are multiplexed, allowing the pins to be configured for use by ports of different widths or links. If an xConnect Link is enabled, the pins of the underlying ports are disabled. If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled. Ports always operate at their specified width, even if they share pins with another port.

## 5.4   Timers

Timers are 32-bit counters that are relative to the xCORE Tile reference clock. A timer is defined to tick every 10 ns. This value is derived from the reference clock, which is configured to tick at 100 MHz by default.

## 5.5   PLL

The PLL creates a high-speed clock that is used for the switch, tile, and reference clock. The PLL multiplication value is selected through the two MODE pins, and can be changed by software to speed up the tile or use less power. The MODE pins are set as shown in Figure 2:

Figure 2 also lists the values of $OD$, $F$ and $R$, which are the registers that define the ratio of the tile frequency to the oscillator frequency:

$$F_{core} = F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \times \frac{1}{OD+1}$$

| Oscillator | MODE | | Tile | PLL Ratio | PLL settings | | |
|---|---|---|---|---|---|---|---|
| Frequency | 1 | 0 | Frequency | | $OD$ | $F$ | $R$ |
| 5-13 MHz | 0 | 0 | 130-399.75 MHz | 30.75 | 1 | 122 | 0 |
| 13-20 MHz | 1 | 1 | 260-400.00 MHz | 20 | 2 | 119 | 0 |
| 20-48 MHz | 1 | 0 | 167-400.00 MHz | 8.33 | 2 | 49 | 0 |
| 48-100 MHz | 0 | 1 | 196-400.00 MHz | 4 | 2 | 23 | 0 |

Figure 2:
PLL multiplier
values and
MODE pins

$OD$, $F$ and $R$ must be chosen so that $0 \le R \le 63$, $0 \le F \le 4095$, $0 \le OD \le 7$, and $260MHz \le F_{osc} \times \frac{F+1}{2} \times \frac{1}{R+1} \le 1.3GHz$. The $OD$, $F$, and $R$ values can be modified by writing to the digital node PLL configuration register.

The MODE pins must be held at a static value until the third rising edge of the system clock following the deassertion of the system reset.

For 500 MHz parts, once booted, the PLL must be reprogrammed to provide this tile frequency. The XMOS tools perform this operation by default.

Further details on configuring the clock can be found in the XS1-L Clock Frequency Control document, X1433.

## 5.6 Boot ROM

The xCORE Tile boot procedure is illustrated in Figure 3. In normal usage, MODE[4:2] controls the boot source according to the table in Figure 4. If bit 5 of the security register (*see* §5.7.1) is set, the device boots from OTP.



Figure 3:
Boot
procedure
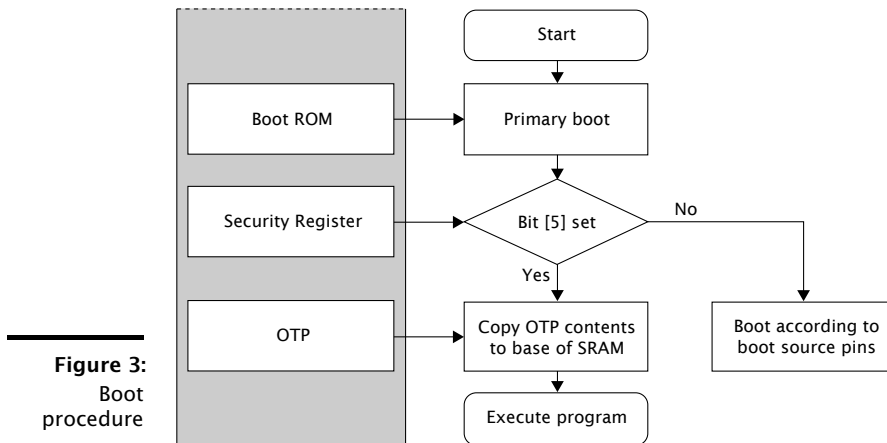
| MODE[4] | MODE[3] | MODE[2] | Boot Source |
|---------|---------|---------|-------------|
| X | 0 | 0 | None: Device waits to be booted via JTAG |
| X | 0 | 1 | Reserved |
| 0 | 1 | 0 | X0 boots from link B, X1 from channel end 0 via X0 |
| 0 | 1 | 1 | X0 boots from SPI, X1 from channel end 0 via X0 |

Figure 4:
Boot source
pins

For MODE[4]=0, MODE[3]=1, MODE[2]=1 (X0 boots from SPI, X1 from channel end 0 via X0):

| Pin[A] | Signal | Description |
|--------|--------|-------------|
| X0D00 | MISO | Master In Slave Out |
| X0D01 | SS | Slave Select |
| X0D10 | SCLK | Clock |
| X0D11 | MOSI | Master Out Slave In |

| MODE[4] | MODE[3] | MODE[2] | Boot Source |
|---------|---------|---------|-------------|
| 1 | 1 | 0 | X0 and X1 independently enable link B and internal links (E, F, G, H), and boot from channel end 0 |
| 1 | 1 | 1 | Both tiles boot from SPI independently |

A  The pins used for SPI boot are hardcoded in the boot ROM and cannot be changed. An SPI boot program can be burned into OTP and used at any time.

## 5.7   OTP

Each xCORE Tile integrates 8 KB one-time programmable (OTP) memory along with a security register that configures system wide security features. The OTP holds data in 2k rows x 32-bit configuration which can be used to implement secure bootloaders and store encryption keys. Data for the security register is loaded from the OTP on power up. All additional data in OTP is copied from the OTP to SRAM and executed first on the processor.

### 5.7.1   Security Register

The security register enables the following security features:

▶ **Secure Boot**: The xCORE Tile is forced to boot from address 0 of the OTP, allowing the xCORE Tile boot ROM to be bypassed (*see* §5.6). This feature can be used to implement a secure bootloader which loads an encrypted image from external flash, decrypts and CRC checks it with the processor, and discontinues the boot process if the decryption or CRC check fails. XMOS provides a default secure bootloader that can be written to the OTP along with secret decryption keys.

▶ **Disable JTAG**: The JTAG interface is disabled, making it impossible for the tile state or memory content to be accessed via the JTAG interface.

▶ **Disable Link access**: Other tiles are forbidden access to the processor state via the system switch.

Disabling both JTAG and Link access transforms an xCORE Tile into a "secure island" with other tiles free for non-secure user application code.

▶ **Disable Global Debug access**: Disables access to the DEBUG_N pin.

▶ **OTP Master and Sector Lock**: Further access to the OTP is prevented by setting the master lock. Locks can also be applied to each of the four OTP sectors individually.

These security features provide a strong level of protection and are sufficient for providing strong IP security.

## 5.8   SRAM

Each xCORE Tile integrates a single 64 KB SRAM bank for both instructions and data. All internal memory is 32 bits wide, and instructions are either 16-bit or 32-bit. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one tile clock cycle. There is no dedicated external memory interface, although data memory can be expanded through appropriate use of the ports.

## 5.9   JTAG

The JTAG module can be used for loading programs, boundary scan testing, in-circuit source-level debugging and programming the OTP memory.
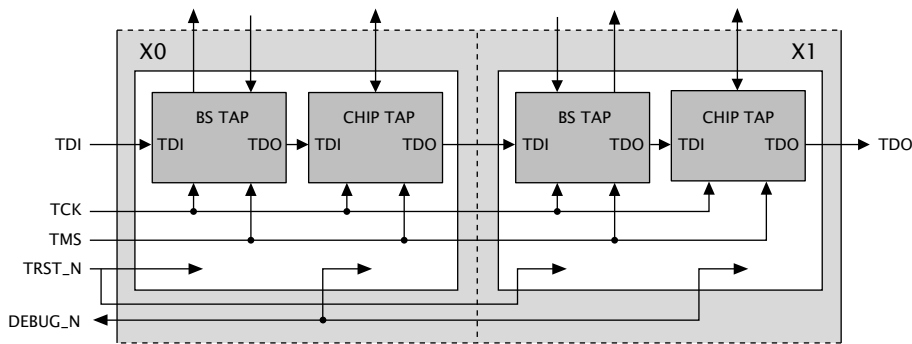
**Figure 5:**
JTAG chain
structure

The JTAG chain structure is illustrated in Figure 5. Directly after reset, two TAP controllers are present in the JTAG chain for each xCORE Tile: the boundary scan TAP and the chip TAP. The boundary scan TAP is a standard 1149.1 compliant TAP that can be used for boundary scan of the I/O pins. The chip TAP provides access into the xCORE Tile, switch and OTP for loading code and debugging.

The TRST_N pin must be asserted low during and after power up for 100 ns. If JTAG is not required, the TRST_N pin can be tied to ground to hold the JTAG module in reset.

The DEBUG_N pin is used to synchronize the debugging of multiple xCORE Tiles. This pin can operate in both output and input mode. In output mode and when configured to do so, DEBUG_N is driven low by the device when the processor hits a debug break point. Prior to this point the pin will be tri-stated. In input mode and when configured to do so, driving this pin low will put the xCORE Tile into debug mode. Software can set the behavior of the xCORE Tile based on this pin.

This pin should have an external pull up of 4K7-47K Ω or left not connected in single core applications.

The JTAG device identification register can be read by using the IDCODE instruction. Its contents are specified in Figure 6.

| Bit31 | | | | Device Identification Register | | | | | | | | | | | | | | | | | | | | | | | | | | | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Version | | | | Part Number | | | | | | | | | | | | | | | | Manufacturer Identity | | | | | | | | | | | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | | 0 | | 0 | | 0 | | 2 | | 6 | | 3 | | 3 | | | | | | | | | | | | | | | | | |

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified in Figure 7. The OTP User ID field is read from bits [22:31] of the security register on xCORE Tile 0 (all zero on unprogrammed devices).

| Bit31 | | | | Usercode Register | | | | | | | | | | | | | | | | | | | | | | | | | | | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OTP User ID | | | | | | | | | | Unused | | | | | | Silicon Revision | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | | 0 | | 0 | | 2 | | 8 | | 0 | | 0 | | 0 | | | | | | | | | | | | | | | | | |

## 5.10 PCU

The PCU can be used to isolate the core voltage of the device and reapply it under a controlled condition known as *sleep mode*. In sleep mode, all data in the SRAM is lost. The device recovers into functional mode under the control of an external PCU_WAKE signal or an internal timer.

If the PCU is not required, PCU_WAKE should be left unconnected, PCU_GATE should be left unconnected and PCU_CLK must be tied to CLK.

## 5.11 Power Supplies

The device has the following types of power supply pins:

▶ VDD pins for the xCORE Tile tile

▶ VDDIO pins for the I/O lines

▶ PLL_AVDD pins for the PLL

▶ PCU_VDD and PCU_VDDIO pins for the PCU

▶ OTP_VCC pins for the OTP

Several pins of each type are provided to minimize the effect of inductance within the package, all of which must be connected. The power supplies must be brought up monotonically and input voltages must not exceed specification at any time.

The VDD supply must ramp from 0 V to its final value within 10 ms to ensure correct startup.

The VDDIO supply must ramp to its final value before VDD reaches 0.4 V.

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The PLL_AVDD supply should be separated from the other noisier supplies on the board. The PLL requires a very clean power supply, and a low pass filter (for example, a 2.2 Ω resistor and 100 nF multi-layer ceramic capacitor) is recommended on this pin.

The PCU_VDD supply must be connected to the VDD supply.

The PCU_VDDIO supply must be connected to the VDDIO supply.

The OTP_VCC supply should be connected to the VDDIO supply.

The following ground pins are provided:

▶ PLL_AGND for PLL_AVDD

▶ GND for all other supplies

All ground pins must be connected directly to the board ground.

The VDD and VDDIO supplies should be decoupled close to the chip by several 100 nF low inductance multi-layer ceramic capacitors between the supplies and GND (for example, 4x100nF 0402 low inductance MLCCs per supply rail). The ground side of the decoupling capacitors should have as short a path back to the GND pins as possible. A bulk decoupling capacitor of at least 10 uF should be placed on each of these supplies.

RST_N is an active-low asynchronous-assertion global reset signal. Following a reset, the PLL re-establishes lock after which the device boots up according to the boot mode (*see* §5.6). RST_N and must be asserted low during and after power up for 100 ns.

# 6  DC and Switching Characteristics

## 6.1  Operating Conditions

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|--------|-----------|-----|-----|-----|-------|-------|
| VDD | Tile DC supply voltage | 0.95 | 1.00 | 1.05 | V | |
| VDDIO | I/O supply voltage | 3.00 | 3.30 | 3.60 | V | |
| PLL_AVDD | PLL analog supply | 0.95 | 1.00 | 1.05 | V | |
| PCU_VDD | PCU tile DC supply voltage | 0.95 | 1.00 | 1.05 | V | |
| PCU_VDDIO | PCU I/O DC supply voltage | 3.00 | 3.30 | 3.60 | V | |
| OTP_VCC | OTP supply voltage | 3.00 | 3.30 | 3.60 | V | |
| Cl | xCORE Tile I/O load capacitance | | | 25 | pF | |
| Ta | Ambient operating temperature (Commercial) | 0 | | 70 | ℃ | |
| | Ambient operating temperature (Industrial) | -40 | | 85 | ℃ | |
| Tj | Junction temperature | | | 125 | ℃ | |
| Tstg | Storage temperature | -65 | | 150 | ℃ | |

## 6.2  DC Characteristics

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|--------|-----------|-----|-----|-----|-------|-------|
| V(IH) | Input high voltage | 2.00 | | 3.60 | V | A |
| V(IL) | Input low voltage | -0.30 | | 0.70 | V | A |
| V(OH) | Output high voltage | 2.70 | | | V | B, C |
| V(OL) | Output low voltage | | | 0.60 | V | B, C |
| R(PU) | Pull-up resistance | | 35K | | Ω | D |
| R(PD) | Pull-down resistance | | 35K | | Ω | D |

A  All pins except power supply pins.

B  Ports 1A, 1D, 1E, 1H, 1I, 1J, 1K and 1L are nominal 8 mA drivers, the remainder of the general-purpose I/Os are 4 mA.

C  Measured with 4 mA drivers sourcing 4 mA, 8 mA drivers sourcing 8 mA.

D  Used to guarantee logic state for an I/O when high impedance. The internal pull-ups/pull-downs should not be used to pull external circuitry.

## 6.3  ESD Stress Voltage

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|--------|-----------|-----|-----|-----|-------|-------|
| HBM | Human body model | -2.00 | | 2.00 | KV | |
| MM | Machine model | -200 | | 200 | V | |

## 6.4 Reset Timing

**Figure 11:**
Reset timing

| Symbol | Parameters | MIN | TYP | MAX | UNITS | Notes |
|--------|-----------|-----|-----|-----|-------|-------|
| T(RST) | Reset pulse width | 5 | | | us | |
| T(INIT) | Initialization time | | | 150 | µs | A |

A  Shows the time taken to start booting after RST_N has gone high.

## 6.5 Power Consumption

**Figure 12:**
xCORE Tile
currents

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|--------|-----------|-----|-----|-----|-------|-------|
| I(DDCQ) | Quiescent VDD current | | 28 | | mA | A, B, C |
| PD | Tile power dissipation | | 450 | | µW/MIPS | A, D, E, F |
| IDD | Active VDD current (Speed Grade 4) | | 320 | 600 | mA | A, G |
| | Active VDD current (Speed Grade 5) | | 400 | 600 | mA | A, H |
| I(ADDPLL) | PLL_AVDD current | | | 14 | mA | I |

A  Use for budgetary purposes only.
B  Assumes typical tile and I/O voltages with no switching activity.
C  Includes PLL current.
D  Assumes typical tile and I/O voltages with nominal switching activity.
E  Assumes 1 MHz = 1 MIPS.
F  PD(TYP) value is the usage power consumption under typical operating conditions.
G  Measurement conditions: VDD = 1.0 V, VDDIO = 3.3 V, 25 °C, 400 MHz, average device resource usage.
H  Measurement conditions: VDD = 1.0 V, VDDIO = 3.3 V, 25 °C, 500 MHz, average device resource usage.
I  PLL_AVDD = 1.0 V

The tile power consumption of the device is highly application dependent and should be used for budgetary purposes only.

More detailed power analysis can be found in the XS1-L Power Consumption document, X2999.

## 6.6   Clock

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|--------|-----------|-----|-----|-----|-------|-------|
| f | Frequency | 4.22 | 20 | 100 | MHz | |
| SR | Slew rate | 0.10 | | | V/ns | |
| TJ(LT) | Long term jitter (pk-pk) | | | 2 | % | A |
| f(MAX) | Processor clock frequency (Speed Grade 4) | | | 400 | MHz | B |
| | Processor clock frequency (Speed Grade 5) | | | 500 | MHz | B |

A  Percentage of CLK period.
B  Assumes typical tile and I/O voltages with nominal activity.

Further details can be found in the XS1-L Clock Frequency Control document, X1433.

## 6.7   xCORE Tile I/O AC Characteristics

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|--------|-----------|-----|-----|-----|-------|-------|
| T(XOVALID) | Input data valid window | 8 | | | ns | |
| T(XOINVALID) | Output data invalid window | 9 | | | ns | |
| T(XIFMAX) | Rate at which data can be sampled with respect to an external clock | | | 60 | MHz | |

The input valid window parameter relates to the capability of the device to capture data input to the chip with respect to an external clock source. It is calculated as the sum of the input setup time and input hold time with respect to the external clock as measured at the pins. The output invalid window specifies the time for which an output is invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the device provides functionality to delay the incoming clock with respect to the incoming data.

Information on interfacing to high-speed synchronous interfaces can be found in the XS1 Port I/O Timing document, X5821.

## 6.8   xConnect Link Performance

| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|--------|-----------|-----|-----|-----|-------|-------|
| B(2blinkP) | 2b link bandwidth (packetized) | | | 87 | MBit/s | A, B |
| B(5blinkP) | 5b link bandwidth (packetized) | | | 217 | MBit/s | A, B |
| B(2blinkS) | 2b link bandwidth (streaming) | | | 100 | MBit/s | B |
| B(5blinkS) | 5b link bandwidth (streaming) | | | 250 | MBit/s | B |

A  Assumes 32-byte packet in 3-byte header mode. Actual performance depends on size of the header and payload.
B  7.5 ns symbol time.

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The asynchronous nature of links means that the relative phasing of CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

## 6.9   JTAG Timing

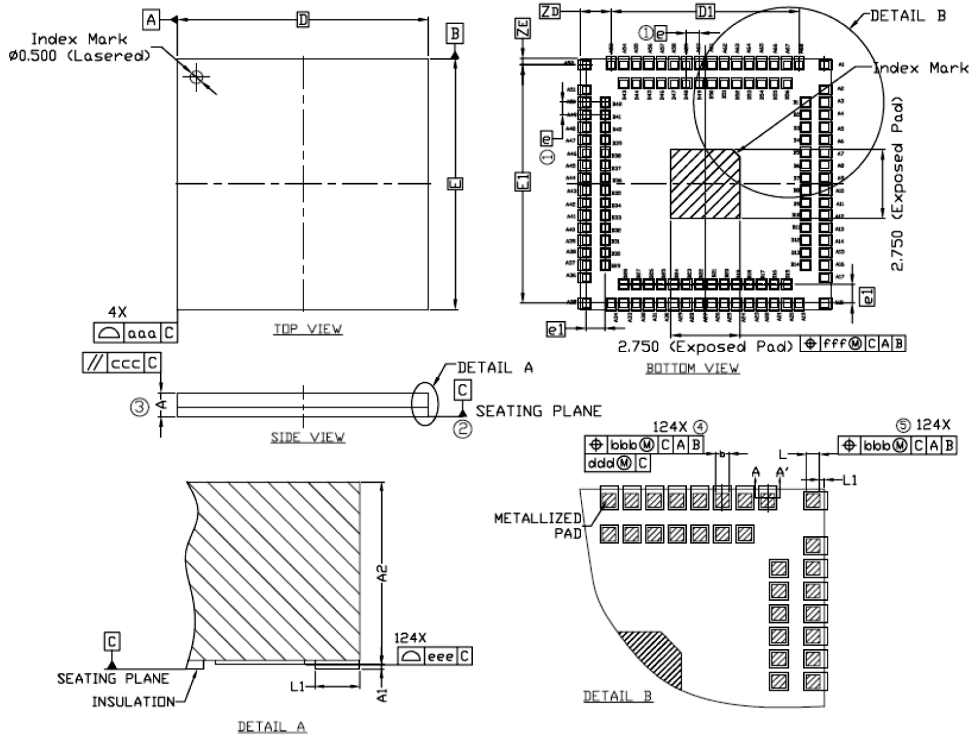| Symbol | Parameter | MIN | TYP | MAX | UNITS | Notes |
|--------|-----------|-----|-----|-----|-------|-------|
| f(TCK_D) | TCK frequency (debug) | | | 18 | MHz | |
| f(TCK_B) | TCK frequency (boundary scan) | | | 10 | MHz | |
| T(SETUP) | TDO to TCK setup time | 5 | | | ns | A |
| T(HOLD) | TDO to TCK hold time | 5 | | | ns | A |
| T(DELAY) | TCK to output delay | | | 15 | ns | B |

A  Timing applies to TMS and TDI inputs.

B  Timing applies to TDO output from negative edge of TCK.

All JTAG operations are synchronous to TCK apart from the global asynchronous reset TRST_N.
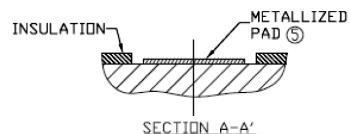
# 7 Package Information



| Symbol | Dimension in mm | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 0.99 | 1.05 | 1.11 |
| A1 | − | − | 0.05 |
| A2 | − | − | 1.06 |
| b | 0.25 | 0.30 | 0.35 |
| D | 10.00 BSC | | |
| E | 10.00 BSC | | |
| D1 | 7.50 BSC | | |
| E1 | 9.50 BSC | | |
| e | 0.50 BSC | | |
| e1 | 0.75 BSC | | |
| L | 0.25 | 0.30 | 0.35 |
| L1 | 0.10 BSC | | |
| ZD | 1.25 BSC | | |
| ZE | 0.25 BSC | | |

DIMENSIONAL REFERENCES

| Ref | TOLERANCE OF FROM AND POSITION |
|---|---|
| aaa | 0.10 |
| bbb | 0.10 |
| ccc | 0.10 |
| ddd | 0.08 |
| eee | 0.08 |
| fff | 0.10 |

Note:
1. 'eT' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
2. DATUM 'C' IS THE MOUNTING SURFACE, WITH WHICH THE PACKAGE IS IN CONTACT.
3. DIMENSION 'A' INCLUDES PACKAGE WARPAGE.
4. DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.
5. METALLIZED PADS ARE Cu PAD WITH IT'S EXPOSED SURFACE PLATED WITH Ni & Au.

## 7.1 Part Marking



Manufacturing date code

Qualification/Speed grade (optional)

USMMYYFN QS

LLLLLL.LL

Lot code
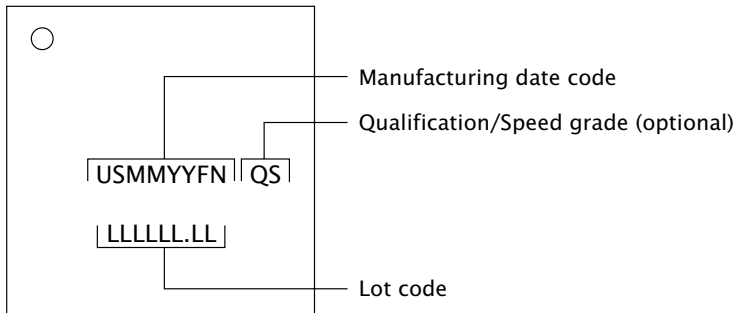
**Figure 17:**
Part marking
scheme

# 8 Ordering Information

| Product Code | Marking | Qualification | Speed Grade |
|---|---|---|---|
| XS1-L02A-QF124-C4 | USMMYYL2 | Commercial | 400 MHz |
| XS1-L02A-QF124-C5 | USMMYYL2 C5 | Commercial | 500 MHz |
| XS1-L02A-QF124-I4 | USMMYYL2 I4 | Industrial | 400 MHz |
| XS1-L02A-QF124-I5 | USMMYYL2 I5 | Industrial | 500 MHz |

**Figure 18:**
Orderable
part numbers

# 9 Development Tools

XMOS provides a comprehensive suite of development tools. Source files, timing scripts and a board design file are input to the compiler toolchain which produces a binary executable. This executable file can be simulated, loaded onto the device and debugged over JTAG, programmed into flash memory on the board or written to OTP memory on the device. The tools can also encrypt the flash image and write the decrpytion key securely to OTP memory.

The tools can be driven from either a graphical development environment or the command line and are supported on Windows, Linux and MacOS X. The tools are available at no cost from xmos.com/downloads. Information on using the tools is provided in a separate user guide, X1013.

# 10 Addendum: XMOS USB Interface

XMOS provides a low-level USB interface for connecting the device to a USB transceiver using the UTMI+ Low Pin Interface (ULPI). The ULPI signals must be connected to the pins named in Figure 19. Note also that some ports on the same tile are used internally and are not available for use when the USB driver is active (they are available otherwise).

| Pin | Signal |
|-----|--------|
| X*n*D02 | |
| X*n*D03 | |
| X*n*D04 | |
| X*n*D05 | Unavailable when USB active |
| X*n*D06 | |
| X*n*D07 | |
| X*n*D08 | |
| X*n*D09 | |

| Pin | Signal |
|-----|--------|
| X*n*D12 | ULPI_STP |
| X*n*D13 | ULPI_NXT |
| X*n*D14 | ULPI_DATA[0] |
| X*n*D15 | ULPI_DATA[1] |
| X*n*D16 | ULPI_DATA[2] |
| X*n*D17 | ULPI_DATA[3] |
| X*n*D18 | ULPI_DATA[4] |
| X*n*D19 | ULPI_DATA[5] |
| X*n*D20 | ULPI_DATA[6] |
| X*n*D21 | ULPI_DATA[7] |
| X*n*D22 | ULPI_DIR |
| X*n*D23 | ULPI_CLK |

| Pin | Signal |
|-----|--------|
| X*n*D26 | |
| X*n*D27 | |
| X*n*D28 | |
| X*n*D29 | Unavailable when USB active |
| X*n*D30 | |
| X*n*D31 | |
| X*n*D32 | |
| X*n*D33 | |

| Pin | Signal |
|-----|--------|
| X*n*D37 | |
| X*n*D38 | |
| X*n*D39 | |
| X*n*D40 | Unavailable when USB active |
| X*n*D41 | |
| X*n*D42 | |
| X*n*D43 | |

**Figure 19:**
ULPI signals provided by the XMOS USB driver

# 11 Device Errata

This section describes minor operational differences from the data sheet and recommended workarounds. As device and documentation issues become known, this section will be updated the document revised.

To guarantee a logic low is seen on the pins RST_N, DEBUG_N, MODE[4:0], TRST_N, TMS, TCK and TDI, the driving circuit should present an impedance of less than $100\,\Omega$ to ground. Usually this is not a problem for CMOS drivers driving single inputs. If one or more of these inputs are placed in parallel, however, additional logic buffers may be required to guarantee correct operation.

For static inputs tied high or low, the relevant input pin should be tied directly to GND or VDDIO.

## 12   Associated Design Documentation

| Document Title | Information | Document Number |
|---|---|---|
| XS1-L Hardware Design Checklist | Board design checklist | X6277 |
| Device Package User Guide | Land pattern, solder paste, ground recommendations | X4979 |
| Estimating Power Consumption For XS1-L Devices | Power consumption | X4271 |
| Programming XC on XMOS Devices | Timers, ports, clocks, cores and channels | X9577 |
| XMOS Tools User Guide | Compilers, assembler and linker/mapper<br><br>Timing analyzer and debugger<br><br>Flash and OTP programming utilities | X1013 |

▶ Example schematic diagrams detailing minimal system configurations are available from http://www.xmos.com/support/silicon.

## 13   Related Documentation

| Document Title | Information | Document Number |
|---|---|---|
| The XMOS XS1 Architecture | ISA manual | X7879 |
| XS1 Port I/O Timing | Port timings | X5821 |
| XS1-L System Specification | Link, switch and system information | X2725 |
| XS1-L Link Performance and Design Guidelines | Link timings | X2999 |
| XS1-L Clock Frequency Control | Advanced clock control | X1433 |
| XS1-L Active Power Conservation | Low-power mode during idle | X5512 |

# 14   Revision History

The page numbers in this section refer to this document.

**Rev. X1189L–10/12**
  1. Renamed XCore to xCORE Tile, and Thread to Core.
  2. Instruction description updated - page 2.
  3. Updated PL section - page 9.

**Rev. X1189K–05/12-B**
  1. Block diagram updated: pins listed sequentially, 4-bit ports updated - page 7.

**Rev. X1189J–05/12**
  1. Input voltage use for 1-bit ports updated footnote on page 15.
  2. Pull up/down information updated for JTAG/MODE pins on page 4.
  3. Updated use of TRST_N on page 12.
  4. Clarified tables of pins used by USB Interface on page 20.
  5. OTP section updated and moved before SRAM on page 12.

**Rev. X1189I–03/12**
  1. Removed "Volatile" from Memory description on page 2.

**Rev. X1189H–05/11**
  1. Changed XMOS Link references to XLA format in Signal Description on page 4.

**Rev. X1189G–01/11**
  1. Replaced "Port Pin Table" with "Signal Description" on page 4.
  2. Updated "ULPI" on page 20 with set of disabled signals.
  3. Removed "Device Configuration".
  4. Added "Associated Design Documentation" on page 22.
  5. Renamed OTP_VDDIO to OTP_VCC.
  6. Renamed DEBUG to DEBUG_N.
  7. Updated Figure 12 on page 16 by adding max value for IDD.
  8. Removed *Preliminary* designation for all characterization data.

**Rev. X1189F–06/10**
  1. Updated "Errata" on page 21 to correct pin A35.
  2. Updated "USB ULPI Mode" on page 20 to correct pin A23.

**Rev. X1189E–05/10**
  1. Added "USB ULPI Mode" on page 20.
  2. Added C5, I4 and I5 parts.

**Rev. X1189D–03/10**

1. Added "Power Supply Sequencing".
2. Added Figure 4 on page 11.
3. Changed from 'Preliminary' to 'Release'.
4. Editorial updates.

**Rev. X1189C–01/10-B**

1. Added "Precedence" on page 9.
2. Added "Power Control Unit" on page 13.
3. Added "SPI Interface' on page 11.

**Rev. X1189B–01/10**

1. Added "Package Marking" on page 20.
2. Updated "Miscellaneous Control Signals".
3. Added ring position to pin table.

**Rev. X1189A–12/09**

1. Initial revision.

**XMOS**®