

1ch 4 A High Speed Low-side Gate Driver

BD2310G

General Description

BD2310G is 1ch Low-side Gate Driver, which can drive external Nch-FET and IGBT at high speed. BD2310G can supply output current 4 A at small package SSOP5.

This driver has the VREF pin for external input logic supply voltage and this range is 2.0 V to 5.5 V. As a protection function, the driver includes an Undervoltage Lockout (UVLO) between VCC and GND.

Key Specifications

- Output Voltage Range: 4.5 V to 18 V
- Input Logic Voltage Range: 2.0 V to 5.5 V
- Output Current I_{O+}/I_{O-} : 4 A / 4 A (Typ)
- Turn-on / Turn-off Delay Time: 15 ns / 15 ns (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package

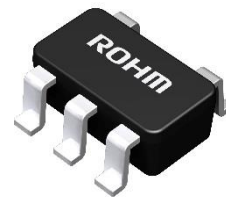
SSOP5

W (Typ) x D (Typ) x H (Max)

2.9 mm x 2.8 mm x 1.25 mm

Features

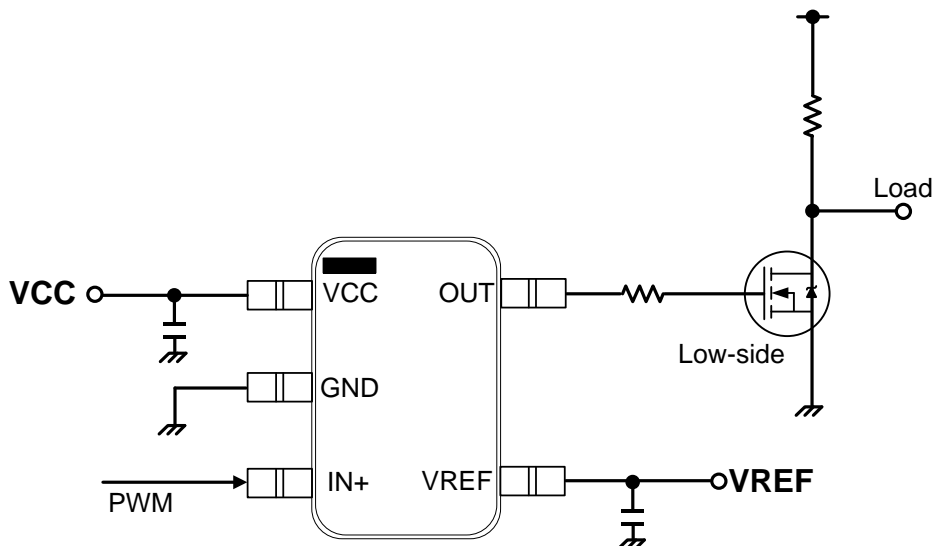
- Gate Drive Voltage Range 4.5 V to 18 V
- Built-in Undervoltage Lockout (UVLO) between VCC and GND
- Input Logic Voltage Range 2.0 V to 5.5 V
- In-phase Output with Input signal
- Small Package SSOP5



Applications

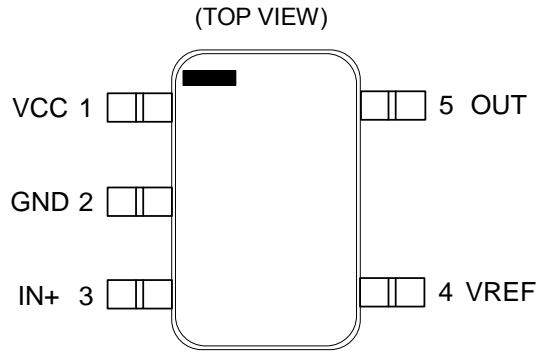
- MOSFET / IGBT Driver Applications
- DC / DC Converters
- Motor Control

Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

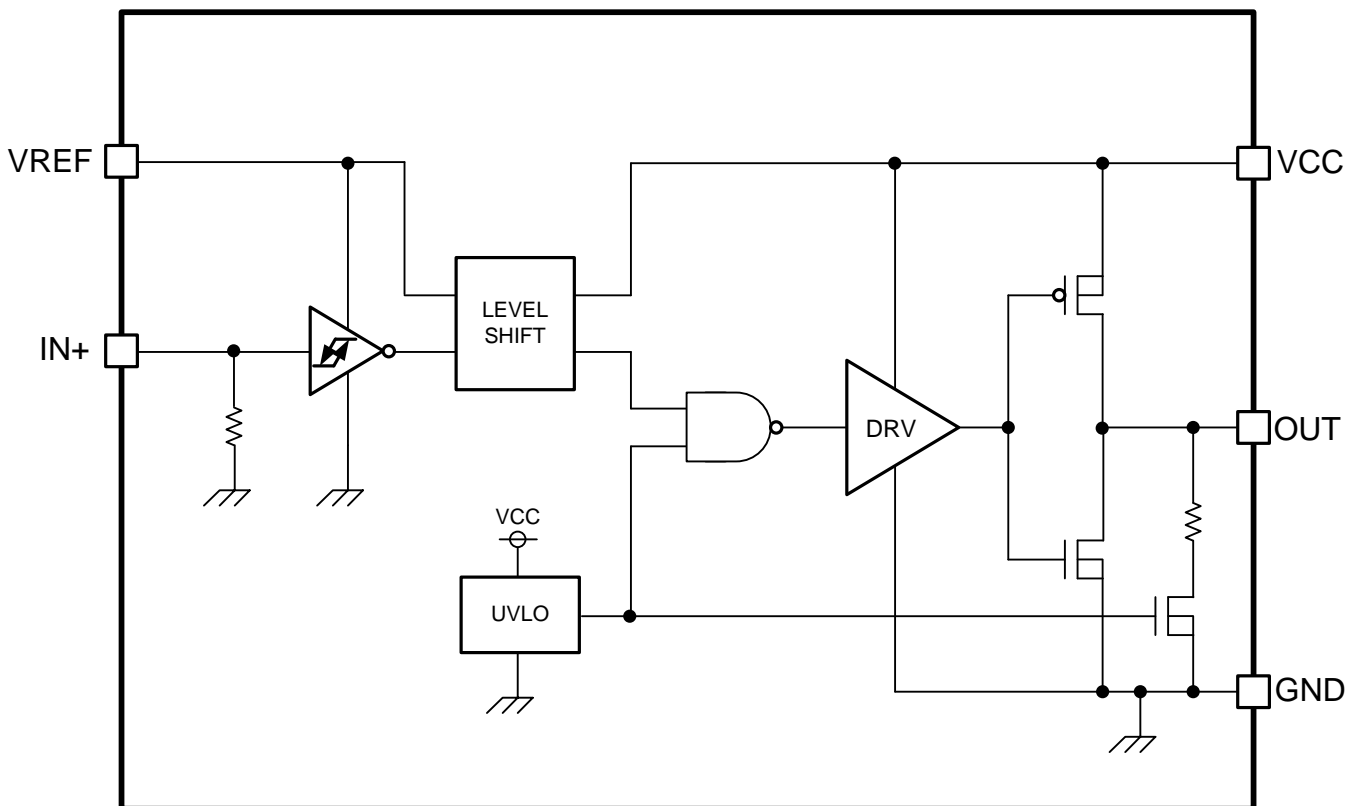
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	VCC	Supply voltage
2	GND	Ground
3	IN+	Logic input
4	VREF	Logic supply voltage
5	OUT	Gate drive output

Block Diagram



Absolute Maximum Rating (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	VCC	-0.3 to +20	V
Logic Input Voltage	V _{IN}	-0.3 to V _{REF} + 0.3	V
Logic Supply Voltage	V _{REF}	-0.3 to +6.0	V
Output Voltage	V _{OUT}	-0.3 to VCC + 0.3	V
Maximum Junction Temperature	T _{Jmax}	150	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance (Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 3)	2s2p ^(Note 4)	
SSOP5				
Junction to Ambient	θ_{JA}	376.5	185.4	°C/W
Junction to Top Characterization Parameter ^(Note 2)	Ψ_{JT}	40	30	°C/W

(Note 1) Based on JESD51-2A (Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size			
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt			
Top					
Copper Pattern	Thickness				
Footprints and Traces	70 μ m				
Layer Number of Measurement Board	Material	Board Size			
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt			
Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μ m	74.2 mm x 74.2 mm	35 μ m	74.2 mm x 74.2 mm	70 μ m

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	12	18	V
Logic Input Voltage	V _{IN}	0	-	V _{REF}	V
Logic Supply Voltage	V _{REF}	2.0	3.3	5.5	V
Output Voltage	V _{OUT}	0	-	VCC	V
Operating Temperature	Topr	-40	+25	+125	°C

Electrical Characteristics (Unless otherwise specified VCC = 12 V, V_{REF} = 3.3 V, Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions	
Circuit Current							
VCC Static Supply Current	I _{CC}	-	35	70	μA	V _{IN} = 0 V	
VREF Static Supply Current	I _{REF}	-	4.5	9.0	μA	V _{IN} = 0 V	
Undervoltage Lockout (UVLO)							
Detect Threshold Voltage	V _{UV-}	2.9	3.6	4.3	V		
Reset Threshold Voltage	V _{UV+}	3.1	3.8	4.5	V		
Hysteresis Voltage	V _{UV_HYS}	-	0.2	-	V		
Input							
Logic "0" Threshold Voltage	V _{IN_L}	0.2V _{REF}	0.3V _{REF}	-	V		
Logic "1" Threshold Voltage	V _{IN_H}	-	0.5V _{REF}	0.6V _{REF}	V		
"0" Input Circuit Current	I _{IN_L}	-	-	1	μA	V _{IN} = 0 V	
"1" Input Circuit Current	I _{IN_H}	-	33	50	μA	V _{IN} = V _{REF}	
Output							
Output Short Circuit Pulsed Current	OUT-VCC	I _{O+}	-	4	-	A	V _{OUT} = 0 V Pulse Width ≤ 1 μs
	OUT-GND	I _{O-}	-	4	-	A	V _{OUT} = VCC Pulse Width ≤ 1 μs
Turn-on Propagation Delay	t _{ON}	-	15	30	ns		
Turn-off Propagation Delay	t _{OFF}	-	15	30	ns		
Rise Time	t _R	-	10	20	ns	CL = 1000 pF	
Fall Time	t _F	-	10	20	ns	CL = 1000 pF	
Minimum Input Pulse Width	t _{INMIN}	-	-	50	ns		

Typical Performance Curves

(Unless otherwise specified VCC = 12 V, VREF = 3.3 V, Ta = 25 °C)

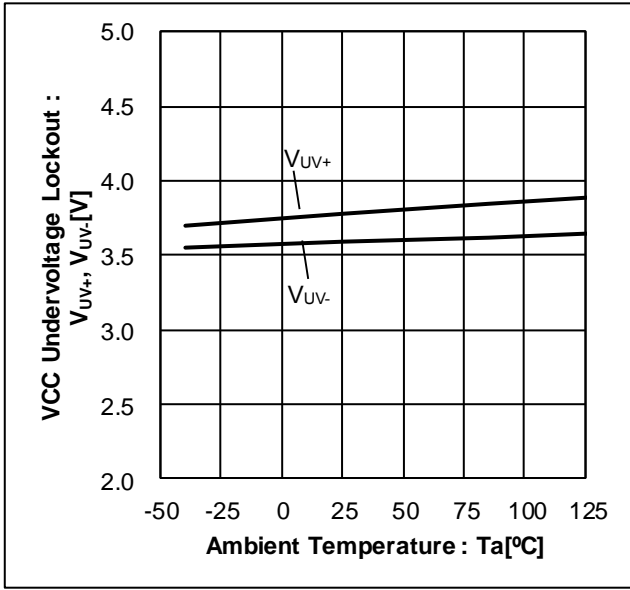


Figure 1. VCC Undervoltage Lockout vs Ambient Temperature

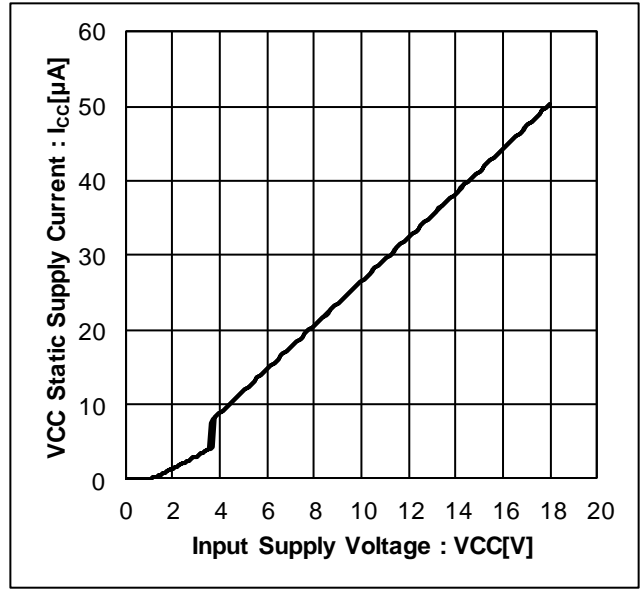


Figure 2. VCC Static Supply Current vs Input Supply Voltage

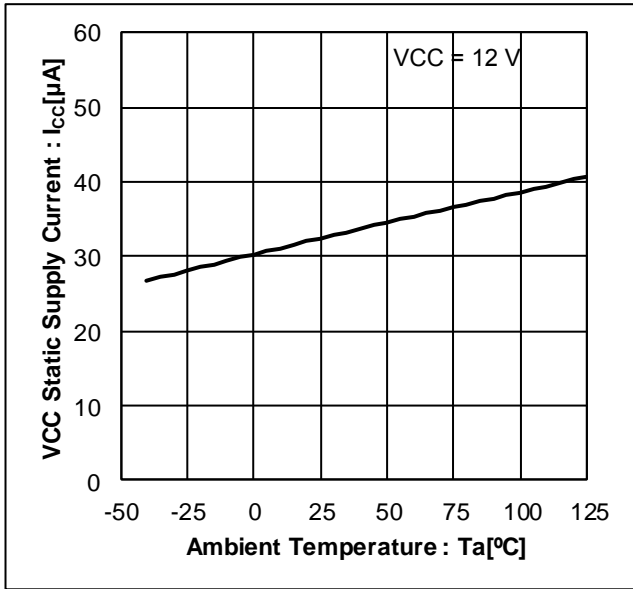


Figure 3. VCC Static Supply Current vs Ambient Temperature (VCC = 12 V)

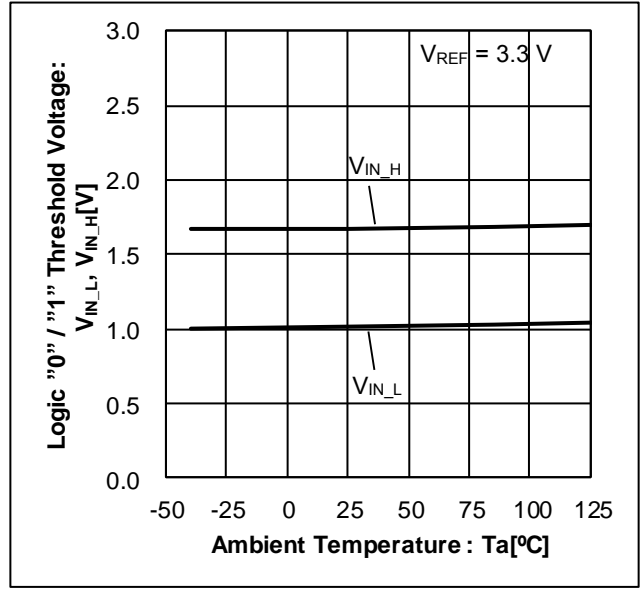


Figure 4. Logic "0" / "1" Threshold Voltage vs Ambient Temperature

Typical Performance Curves – continued

(Unless otherwise specified VCC = 12 V, VREF = 3.3 V, Ta = 25 °C)

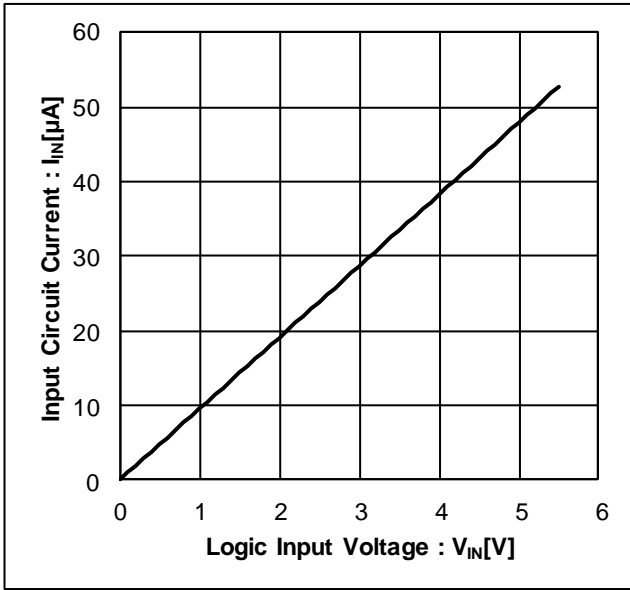


Figure 5. Input Circuit Current vs Logic Input Voltage

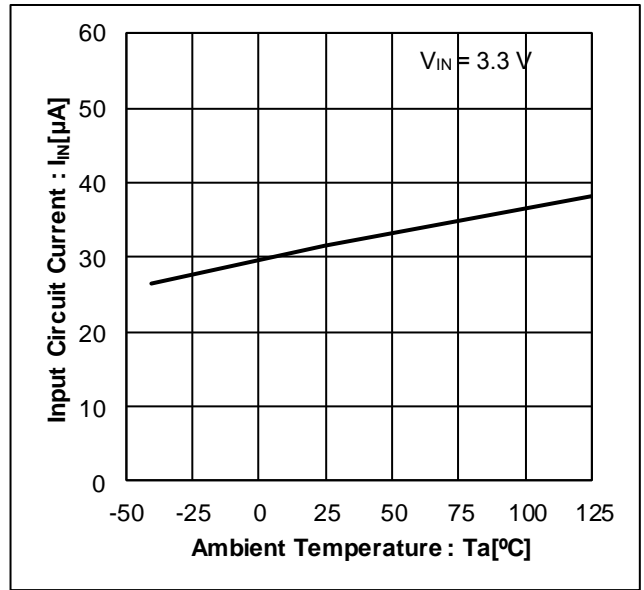


Figure 6. Input Circuit Current vs Ambient Temperature (V_{IN} = 3.3 V)

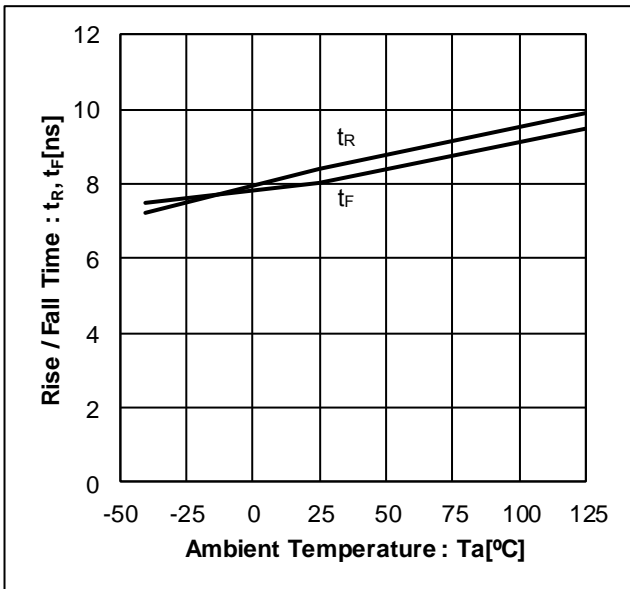


Figure 7. Rise / Fall Time vs Ambient Temperature

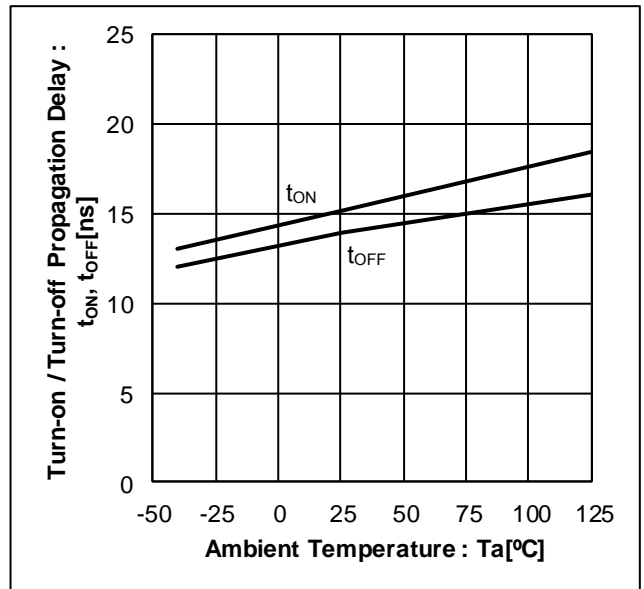


Figure 8. Turn-on / Turn-off Propagation Delay vs Ambient Temperature

Timing Chart

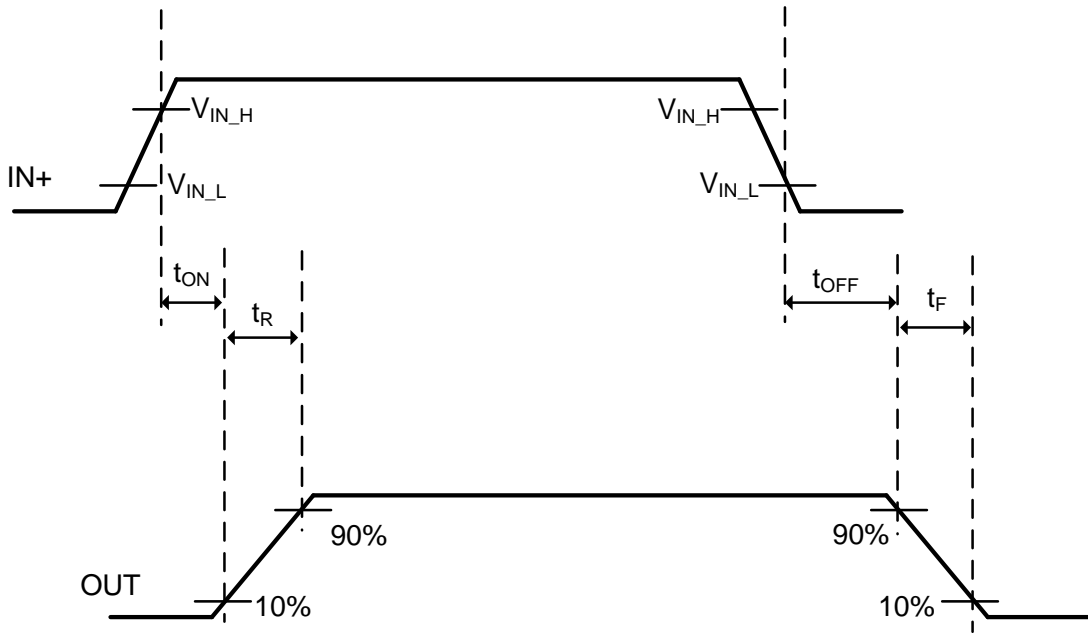


Figure 9. Timing Chart

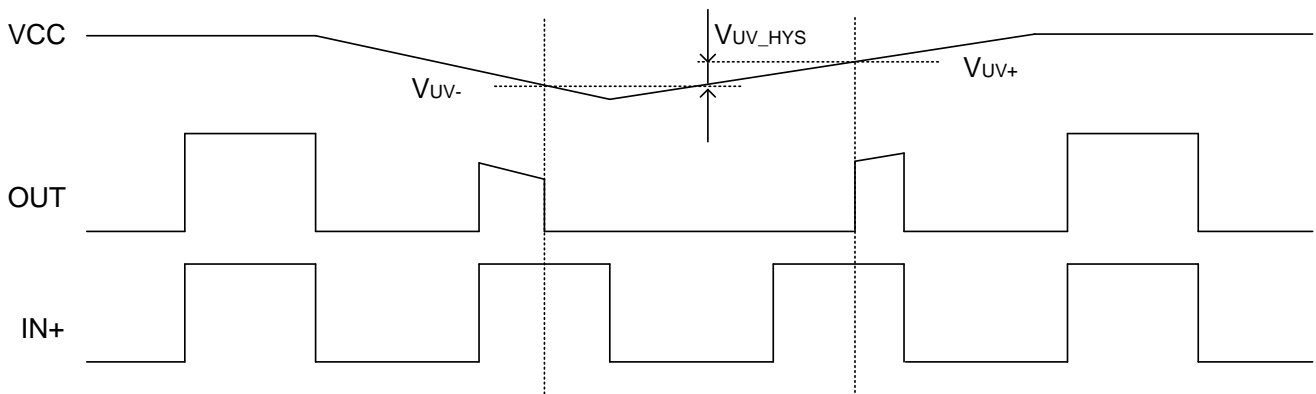


Figure 10. UVLO Timing Chart

Static Logic Function Table

VCC	VREF	IN+	OUT
$\leq V_{UV+}$	X ^(Note 5)	X ^(Note 5)	L
$\geq 4.5\text{ V}$	$< 2\text{ V}$ ^(Note 6)	X ^(Note 5)	L ^(Note 6)
$\geq 4.5\text{ V}$	$\geq 2\text{ V}$	L	L
$\geq 4.5\text{ V}$	$\geq 2\text{ V}$	H	H

(Note 5) X is not depend on the value.

(Note 6) VREF has the threshold between 0 V to 2 V. It does not definitely become OUT = L below 2 V.

Application Components Selection Method

(1) Gate Resistor

The gate resistor $R_{G(ON/OFF)}$ is selected to the switching speed of the power device. The switching time (t_{SW}) is defined as the time spent to reach the end of the plateau voltage, so the turn-on gate resistor $R_{G(ON)}$ can be calculated using the following formulas.

$$I_G = \frac{Q_{gs} + Q_{gd}}{t_{SW}} \quad [1]$$

$$R_{TOTAL(ON)} = R_{PON} + R_{G(ON)} = \frac{V_{CC} - V_{GS(TH)}}{I_G} \quad [2]$$

$$t_{SW} = \frac{Q_{gs} + Q_{gd}}{I_G} = \frac{(Q_{gs} + Q_{gd})(R_{PON} + R_{G(ON)})}{(V_{CC} - V_{GS(TH)})} \quad [3]$$

Where:

I_G is the gate current of the power device.

Q_{gs} is the charge between gate and source of the power device.

Q_{gd} is the charge between gate and drain of the power device.

$V_{GS(TH)}$ is the threshold voltage of the power device.

The turn-on gate resistance can be changed to control output slew rate (dV_D/dt). The slew rate of the power device is determined by the following equation.

$$\frac{dV_D}{dt} = \frac{I_G}{C_{rSS}} \quad [4]$$

where:

C_{rSS} is the feedback capacitance.

The gate resistance is determined as follows by substituting equation [4] into equation [2].

$$R_{TOTAL(ON)} = R_{PON} + R_{G(ON)} = \frac{V_{CC} - V_{GS(TH)}}{C_{rSS} \times \frac{dV_D}{dt}} \quad [5]$$

$$R_{G(ON)} = \frac{V_{CC} - V_{GS(TH)}}{C_{rSS} \times \frac{dV_D}{dt}} - R_{PON} \quad [6]$$

When other power devices are turned on, current flows in the power device which is off through C_{gd} . At this point, the gate resistance ($R_{G(OFF)}$) should be set so that the gate voltage does not exceed the threshold of the power device and turn on the power device itself.

$$V_{GS(TH)} \geq (R_{NOFF} + R_{G(OFF)}) \times I_G = (R_{NOFF} + R_{G(OFF)}) \times C_{gd} \times \frac{dV_D}{dt} \quad [7]$$

$$R_{G(OFF)} \leq \frac{V_{GS(TH)}}{C_{gd} \times \frac{dV_D}{dt}} - R_{NOFF} \quad [8]$$

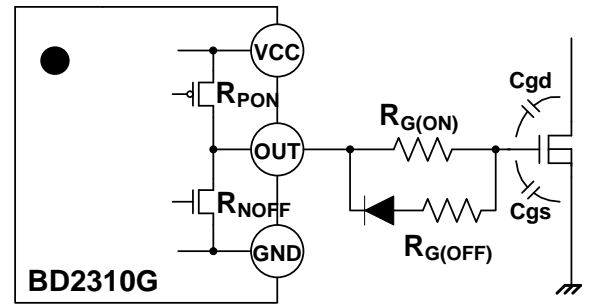


Figure 11. Gate Driver Equivalent Circuit

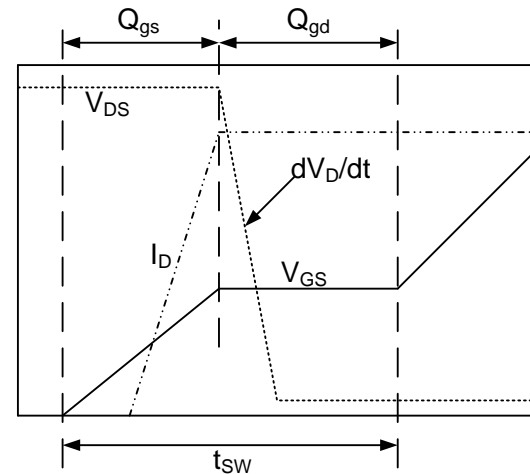


Figure 12. Gate Charge Transfer Characteristics

Application Components Selection Method – continued

(2) Input Capacitor

A low-ESR ceramic capacitor should be used near the VCC pin and the VREF pin to reduce input ripple voltage. In considering of the DC bias characteristic, it is recommended 0.5 μF or more between VCC and GND, 8 nF or more between VREF and GND.

PCB Layout

The voltage of VCC pin may be risen by the parasitic inductance of the PCB and the bonding wire in the IC.

The mechanism by which VCC voltage rises is Figure 13.

(1) When the signal with short pulse width is input as an input signal, it is turned off in the state that Pch-FET of the final stage is turned on and flows current.

(2) When Pch-FET is turned off while current is flowing, VCC voltage is risen by the parasitic inductance.

When VCC voltage is risen and over absolute maximum ratings, it can damage the IC.

To reduce the rising of VCC voltage, please locate a ceramic capacitor which is low-ESR near the VCC pin and the GND pin, and connect it so that parasitic inductance L_{VCC} and L_{GND} in the PCB becomes small. It is recommended 3 nH or less each L_{VCC} and L_{GND} .

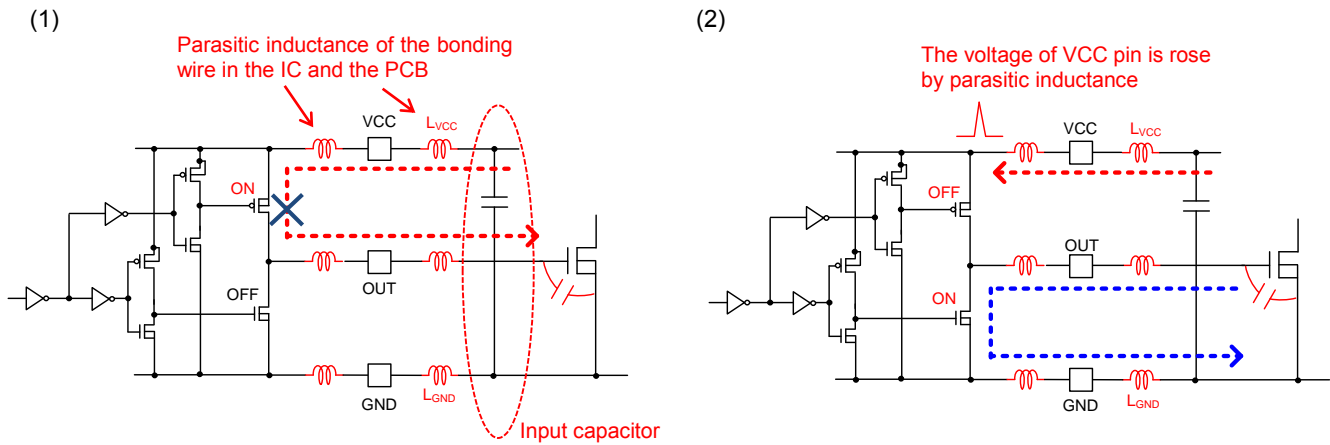
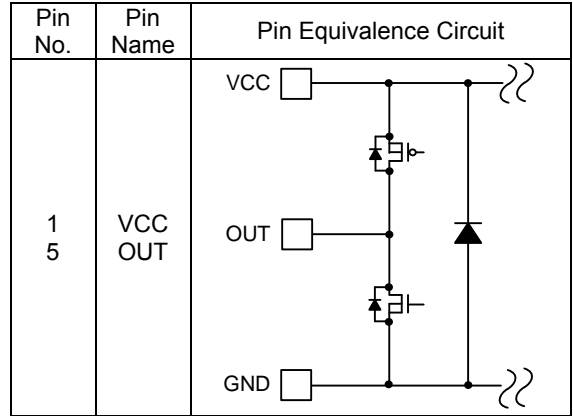
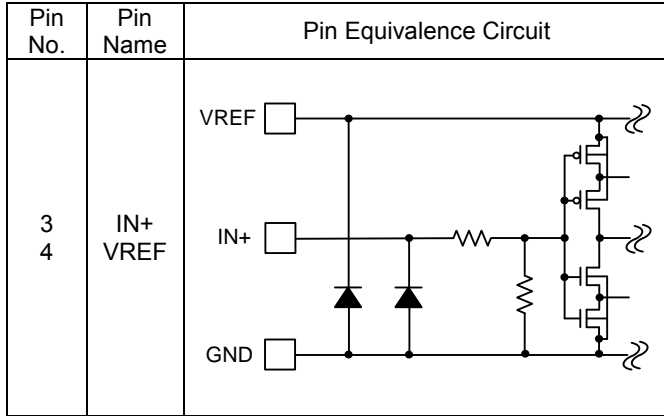


Figure 13. Mechanism of Overshoot

I/O Equivalence Circuits



Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

- When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.
- When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

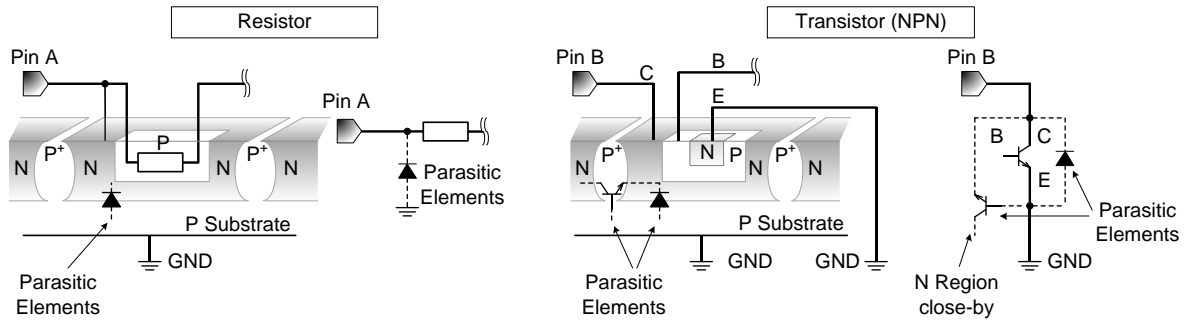
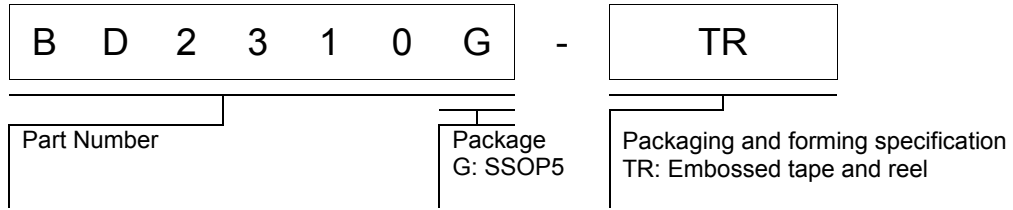


Figure 18. Example of Monolithic IC Structure

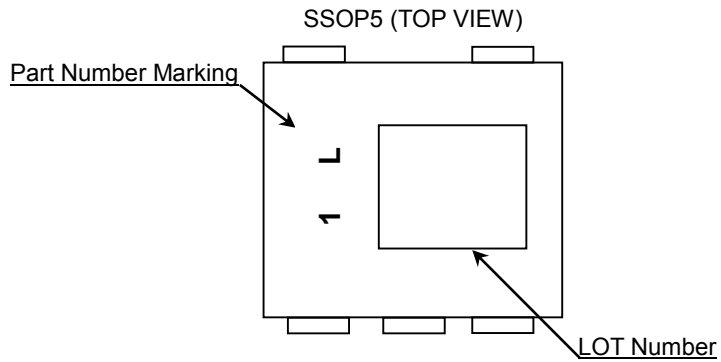
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

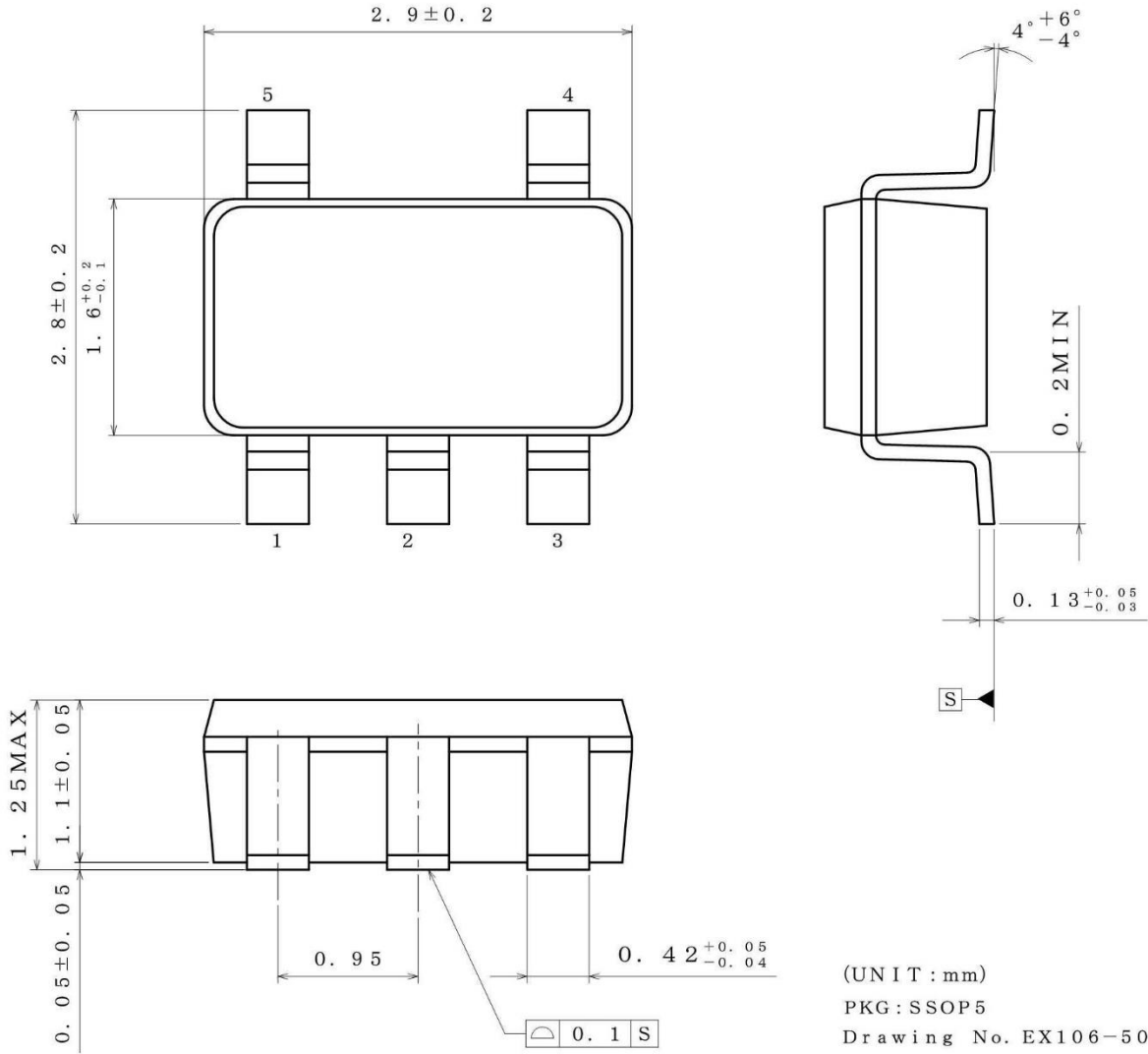


Marking Diagram



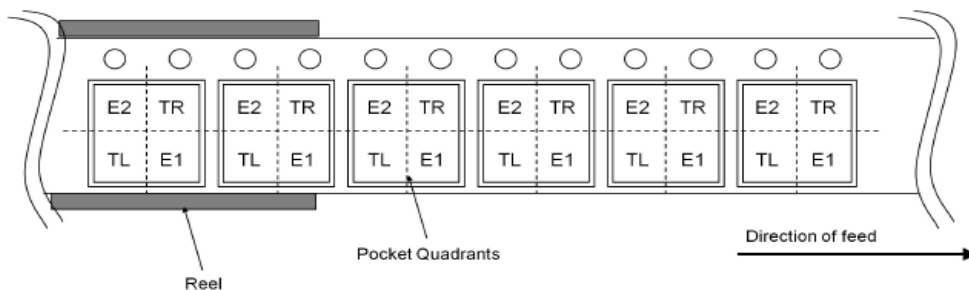
Physical Dimension and Packing Information

Package Name	SSOP5
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< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1 pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
26.Mar.2020	001	New Release

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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