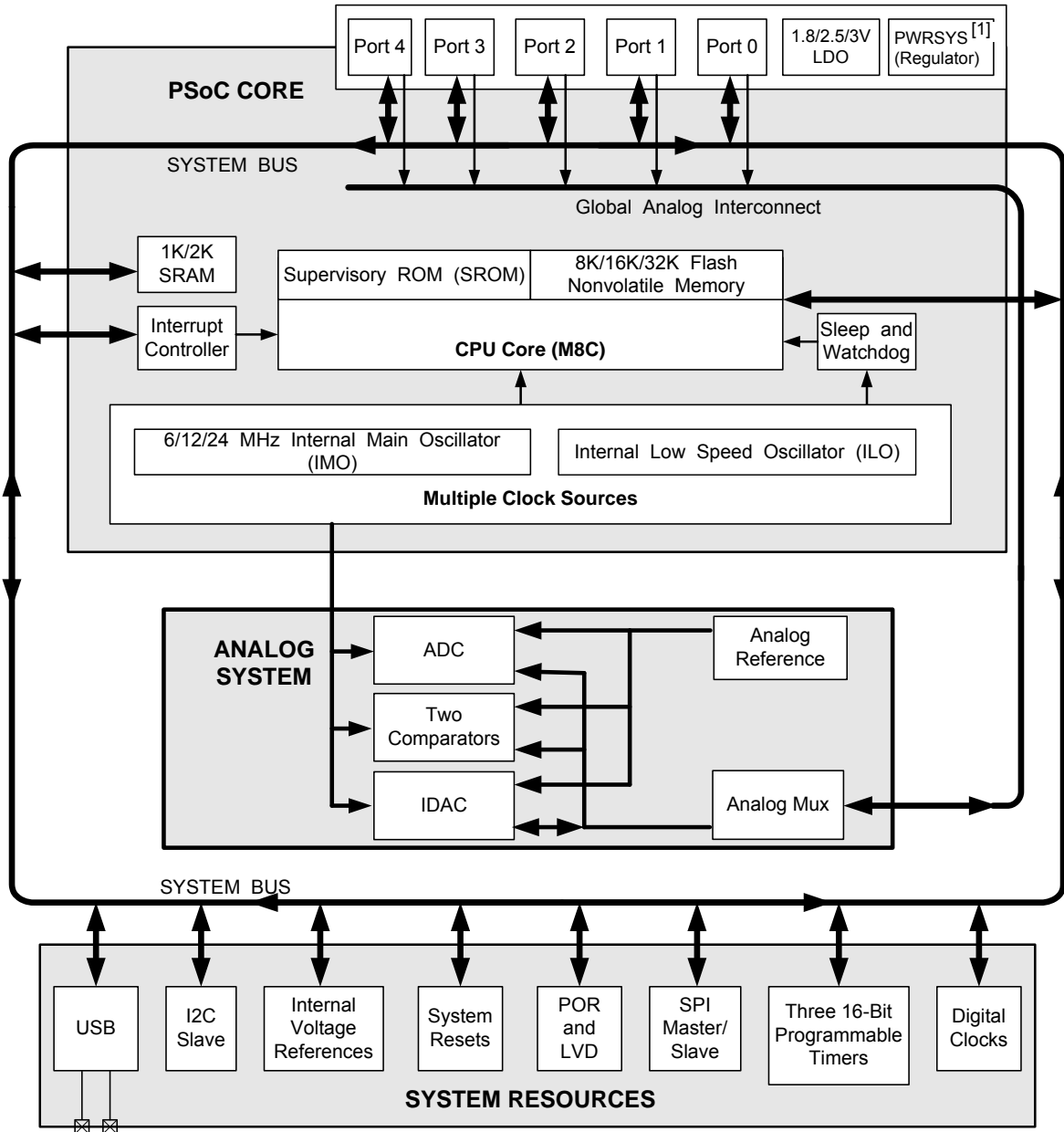


## Features

- Powerful Harvard-architecture processor
  - M8C CPU with a max speed of 24 MHz
- Operating Range: 1.71 V to 5.5 V
  - Standby Mode 1.1  $\mu$ A (Typ)
  - Deep Sleep 0.1  $\mu$ A (Typ)
- Operating Temperature range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Flexible on-chip memory
  - 8 KB flash, 1 KB SRAM
  - 16 KB flash, 2 KB SRAM
  - 32 KB flash, 2 KB SRAM
  - Read while Write with EEPROM emulation
  - 50,000 flash erase/write cycles
  - In-system programming simplifies manufacturing process
- Four Clock Sources
  - Internal main oscillator (IMO): 6/12/24 MHz
  - Internal low-speed oscillator (ILO) at 32 kHz for watchdog and sleep timers
  - External 32 KHz Crystal Oscillator
  - External Clock Input
- Programmable pin configurations
  - Up to 36 general purpose dual mode GPIO (Analog inputs and Digital I/O supported)
  - High sink current of 25 mA per GPIO
    - Max sink current 120 mA for all GPIOs
  - Source Current
    - 5 mA on ports 0 and 1
    - 1 mA on ports 2,3 and 4
  - Configurable internal pull-up, high-Z and open drain modes
  - Selectable, regulated digital I/O on port 1
  - Configurable input threshold on port 1
- Versatile Analog functions
  - Internal Low-Dropout voltage regulator for high power supply rejection ratio (PSRR)
- Full-Speed USB
  - 12 Mbps USB 2.0 compliant
  - Eight unidirectional endpoints
  - One bidirectional endpoint
  - Dedicated 512 byte SRAM
  - No external crystal required
- Additional system resources
  - I2C Slave:
    - Selectable to 50 kHz, 100 kHz, or 400 kHz
  - Configurable up to 12 MHz SPI master and slave
  - Three 16-bit timers
  - Watchdog and sleep timers
  - Integrated supervisory circuit
  - 10-bit incremental analog-to-digital converter (ADC) with internal voltage reference
  - Two general-purpose Comparators
    - 3 Voltage References (0.8 V, 1 V, 1.2 V)
    - Any pin to either comparator inputs
    - Low-power operation at 10  $\mu$ A
  - One 8-bit IDAC with full scale range of 512  $\mu$ A
  - One 8-bit Software PWM
- Development Platform
  - PSoC Designer™ IDE
- GPIOs and Package options
  - 13 GPIOs - QFN 16
  - 28 GPIOs - QFN 32
  - 34 GPIOs - QFN 48
  - 36 GPIOs - QFN 48

### Logic Block Diagram



**Note**

1. Internal voltage regulator for internal circuitry.

## More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right PSoC device for your design, and quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article “[How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292](#)”.

- **Overview:** PSoC Portfolio, PSoC Roadmap
- **Product Selectors:** PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP. In addition, PSoC Designer includes a device selection tool.
- **Application Notes and Code Examples:** Cover a broad range of topics, from basic to advanced level. Many of the application notes include code examples.
- **Technical Reference Manuals (TRM):** The TRM provides complete detailed descriptions of the internal architecture of the PSoC 1 devices.

### Development Kits:

- **CY3215A-DK In-Circuit Emulation Lite Development Kit** includes an in-circuit emulator (ICE). While the ICE-Cube is primarily used to debug PSoC 1 devices, it can also program PSoC 1 devices using ISSP.
- **CY3210-PSOCEVAL1 Kit** enables you to evaluate and experiment Cypress’s PSoC 1 programmable system-on-chip design methodology and architecture.

The **MiniProg1** and **MiniProg3** device provides an interface for flash programming.

## PSoC Designer

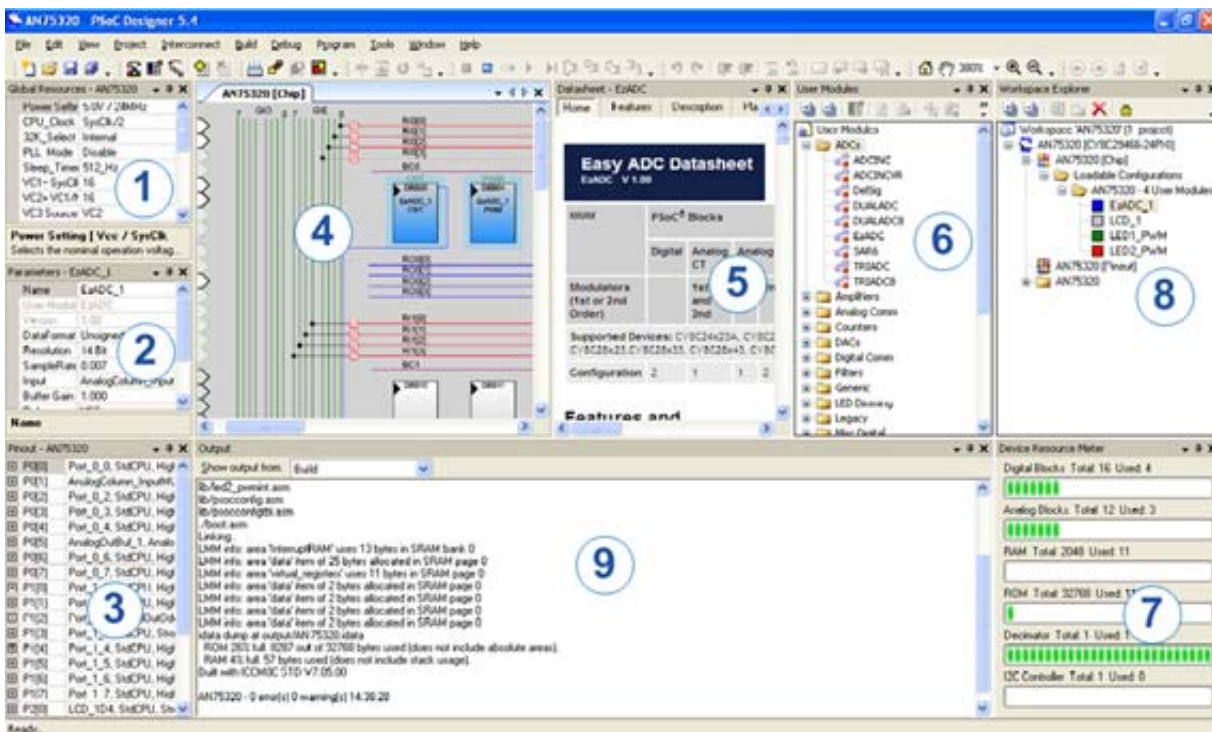
**PSoC Designer** is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. **Figure 1** shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources** – all device hardware settings.
2. **Parameters** – the parameters of the currently selected User Modules.
3. **Pinout** – information related to device pins.
4. **Chip-Level Editor** – a diagram of the resources available on the selected chip.

5. **Datasheet** – the datasheet for the currently selected UM
6. **User Modules** – all available User Modules for the selected device.
7. **Device Resource Meter** – device resource usage for the current project configuration.
8. **Workspace** – a tree level diagram of files associated with the project.
9. **Output** – output from project build and debug operations.

**Note:** For detailed information on PSoC Designer, go to **PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide**.

**Figure 1. PSoC Designer Layout**



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## PSoC® Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the [Logic Block Diagram on page 2](#), consists of three main areas:

- The Core
- Analog System
- System Resources (including a full-speed USB port).

A common, versatile bus allows connection between I/O and the analog system.

Depending on the PSoC package, up to 36 GPIO are included in the CY8C24x93 PSoC device. The GPIO provides access to the MCU and analog mux.

### PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

### Analog system

The analog system is composed of an ADC, two comparators and an IDAC. It has an internal 0.8 V, 1 V or 1.2 V analog reference. All the pins can be configured to connect to the analog system.

#### ADC

The ADC in the CY8C24x93 device is an incremental analog-to-digital converter with a range of 8 to 10 bits supporting signed and unsigned data formats. The input to the ADC can be from any pin.

#### IDAC

The IDAC can provide current source up to 512  $\mu$ A to any GPIO pin. In the CY8C24x93 family of devices 4 ranges of current source can be implemented that can vary in 255 steps, and are connected to analog mux bus.

**Table 1. IDAC Ranges**

Range	Full Scale Range in $\mu$ A
1x	64
2x	128
4x	256
8x	512

#### Comparator

The CY8C24x93 family has two high-speed, low-power comparators. The comparators have three voltage references, 0.8 V, 1.0 V and 1.2 V. Comparator inputs can be connected from any pin through the analog mux bus. The comparator output can be read in firmware for processing or routed out via specific pins (P1\_0 or P1\_4).

The output of the two comparators can be combined with 2-input logic functions. The combinatorial output can be optionally combined with a latched value and routed to a pin output or to the interrupt controller. The input multiplexers and the comparator are controller through the CMP User Module.

#### Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin and can be internally connected to the ADC, Comparators or the IDAC.

Other multiplexer applications include:

- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

### Additional System Resources

System resources provide additional capability, such as configurable USB and I2C slave, SPI master/slave communication interface, three 16-bit programmable timers, software 8-bit PWM, low voltage detect, power on reset, and various system resets supported by the M8C.

The merits of each system resource are listed here:

- The I<sup>2</sup>C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on-reset (POR) circuit eliminates the need for a system supervisor.
- A register-controlled bypass mode allows the user to disable the LDO regulator.
- An 8-bit Software PWM is provided for applications like buzzer control or lighting control. A 16-bit Timer acts as the input clock to the PWM. The ISR increments a software counter (8-bit), checks for PWM compare condition and toggles a GPIO accordingly. PWM Output is available on all GPIOs.



## Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the [Technical Reference Manual](#) for the PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at [www.cypress.com/psoc](http://www.cypress.com/psoc).

### Silicon Errata

Errata documents known issues with silicon including errata trigger conditions, scope of impact, available workarounds and silicon revision applicability.

### Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

## Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via [www.cypress.com](http://www.cypress.com), covers a wide variety of topics and skill levels to assist you in your designs.

### CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

### Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

### Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

## Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I<sup>2</sup>C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

## PSoC Designer Software Subsystems

### *Design Entry*

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

### *Code Generation Tools*

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

**Assemblers.** The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

### *Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

### *Online Help System*

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

### *In-Circuit Emulator*

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.



## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

10. Select [user modules](#).
11. Configure user modules.
12. Organize and connect.
13. Generate, verify, and debug.

### Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules”. User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the

internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

### Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

### Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

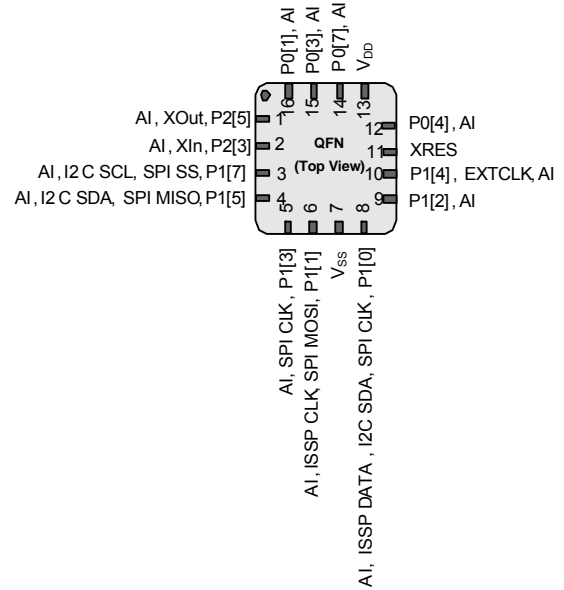
## Pinouts

### 16-pin QFN (13 GPIOs) [2]

**Table 2. Pin Definitions – CY8C24093 [3]**

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	IOHR	I	P1[7]	I <sup>2</sup> C SCL, SPI SS
4	IOHR	I	P1[5]	I <sup>2</sup> C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	ISSP CLK <sup>[4]</sup> , I <sup>2</sup> C SCL, SPI MOSI
7	Power		V <sub>SS</sub>	Ground connection
8	IOHR	I	P1[0]	ISSP DATA <sup>[4]</sup> , I <sup>2</sup> C SDA, SPI CLK <sup>[5]</sup>
9	IOHR	I	P1[2]	
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down
12	IOH	I	P0[4]	
13	Power		V <sub>DD</sub>	Supply voltage
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	
16	IOH	I	P0[1]	

**Figure 2. CY8C24093 Device**



**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

#### Notes

- No center pad.
- 13 GPIOs.
- On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I<sup>2</sup>C bus. Use alternate pins if you encounter issues.
- Alternate SPI clock.

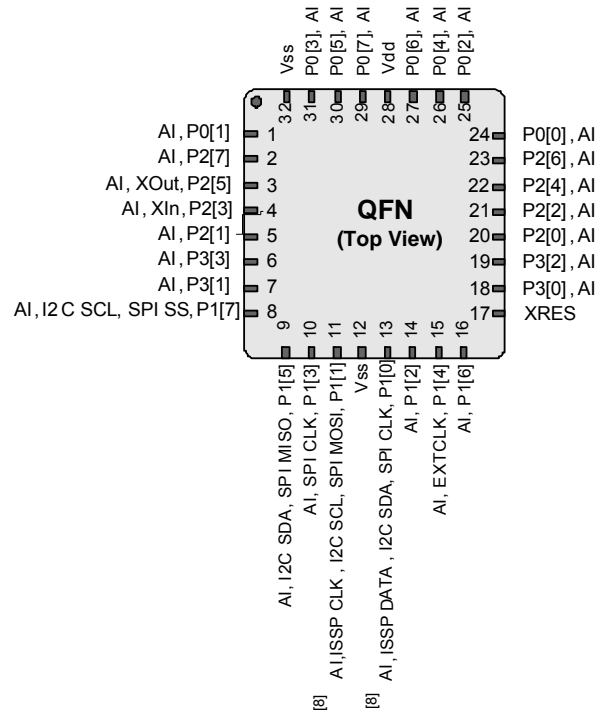
**32-pin QFN (28 GPIOs) [6]**

**Table 3. Pin Definitions – CY8C24193 [7]**

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I <sup>2</sup> C SCL, SPI SS
9	IOHR	I	P1[5]	I <sup>2</sup> C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK <sup>[8]</sup> , I <sup>2</sup> C SCL, SPI MOSI.
12	Power		V <sub>SS</sub>	Ground connection.
13	IOHR	I	P1[0]	ISSP DATA <sup>[8]</sup> , I <sup>2</sup> C SDA, SPI CLK <sup>[9]</sup>
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		V <sub>DD</sub>	Supply voltage
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	
32	Power		V <sub>SS</sub>	Ground connection
CP	Power		V <sub>SS</sub>	Center pad must be connected to ground

**LEGEND** A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

**Figure 3. CY8C24193**



**Notes**

- 28 GPIOs.
- The center pad (CP) on the QFN package must be connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- Alternate SPI clock.

32-pin QFN (28 GPIOs) [10]

Table 4. Pin Definitions – CY8C24293 [11]

Pin No.	Digital	Analog	Name	Description
1	IOH	I	P0[1]	
2	I/O	I	P2[5]	Crystal output (XOut)
3	I/O	I	P2[3]	Crystal input (XIn)
4	I/O	I	P2[1]	
5	I/O	I	P4[3]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I <sup>2</sup> C SCL, SPI SS
9	IOHR	I	P1[5]	I <sup>2</sup> C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK [12], I <sup>2</sup> C SCL, SPI MOSI.
12	Power		V <sub>SS</sub>	Ground connection
13	IOHR	I	P1[0]	ISSP DATA [12], I <sup>2</sup> C SDA, SPI CLK [13]
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P4[0]	
21	I/O	I	P4[2]	
22	I/O	I	P2[0]	
23	I/O	I	P2[2]	
24	I/O	I	P2[4]	
25	IOH	I	P0[0]	
26	IOH	I	P0[2]	
27	IOH	I	P0[4]	
28	IOH	I	P0[6]	
29	Power		V <sub>DD</sub>	
30	IOH	I	P0[7]	
31	IOH	I	P0[3]	
32	Power		V <sub>SS</sub>	Ground connection
CP	Power		V <sub>SS</sub>	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes

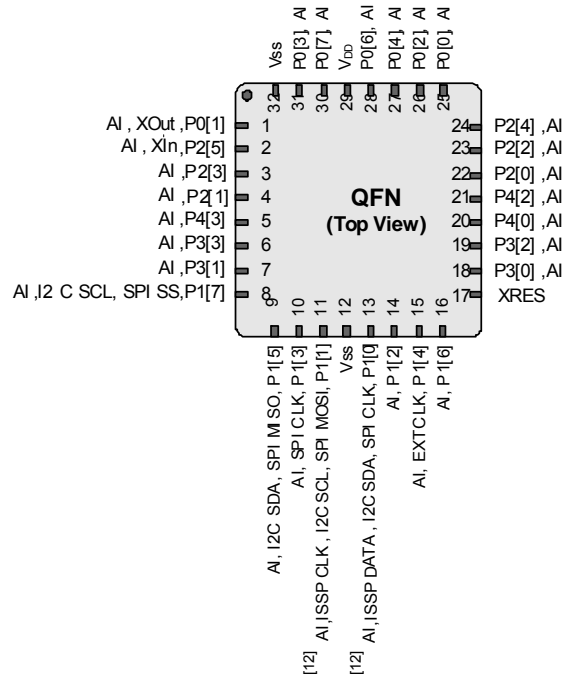
10. 28 GPIOs.

11. The center pad (CP) on the QFN package must be connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.

12. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.

13. Alternate SPI clock.

Figure 4. CY8C24293 Device



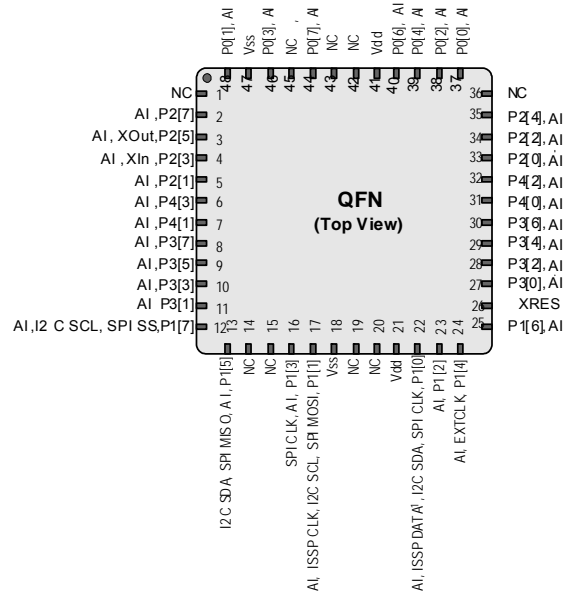
48-pin QFN (34 GPIOs) [14]

Table 5. Pin Definitions – CY8C24393, CY8C24693 [15, 16]

Pin No.	Digital	Analog	Name	Description			
1			NC	No connection			
2	I/O	I	P2[7]				
3	I/O	I	P2[5]	Crystal output (XOut)			
4	I/O	I	P2[3]	Crystal input (XIn)			
5	I/O	I	P2[1]				
6	I/O	I	P4[3]				
7	I/O	I	P4[1]				
8	I/O	I	P3[7]				
9	I/O	I	P3[5]				
10	I/O	I	P3[3]				
11	I/O	I	P3[1]				
12	IOHR	I	P1[7]	I <sup>2</sup> C SCL, SPI SS			
13	IOHR	I	P1[5]	I <sup>2</sup> C SDA, SPI MISO			
14			NC	No connection			
15			NC	No connection			
16	IOHR	I	P1[3]	SPI CLK			
17	IOHR	I	P1[1]	ISSP CLK <sup>[17]</sup> , I <sup>2</sup> C SCL, SPI MOSI			
18	Power		V <sub>SS</sub>	Ground connection			
19			NC	No connection			
20			NC	No connection			
21	Power		V <sub>DD</sub>	Supply voltage			
22	IOHR	I	P1[0]	ISSP DATA <sup>[17]</sup> , I <sup>2</sup> C SDA, SPI CLK <sup>[18]</sup>			
23	IOHR	I	P1[2]				
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)			
25	IOHR	I	P1[6]				
26	Input		XRES	Active high external reset with internal pull-down			
27	I/O	I	P3[0]				
28	I/O	I	P3[2]				
29	I/O	I	P3[4]				
30	I/O	I	P3[6]				
31	I/O	I	P4[0]				
32	I/O	I	P4[2]				
33	I/O	I	P2[0]				
34	I/O	I	P2[2]				
35	I/O	I	P2[4]				
			Pin No.	Digital	Analog	Name	Description
			36			NC	No connection
			37	IOH	I	P0[0]	
			38	IOH	I	P0[2]	
			39	IOH	I	P0[4]	
			40	IOH	I	P0[6]	
			41	Power		V <sub>DD</sub>	Supply voltage
			42			NC	No connection
			43			NC	No connection
			44	IOH	I	P0[7]	
			45			NC	No connection
			46	IOH	I	P0[3]	
			47	Power		V <sub>SS</sub>	Ground connection
			48	IOH	I	P0[1]	
			CP	Power		V <sub>SS</sub>	Center pad must be connected to ground

LEGENDA = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Figure 5. CY8C24393, CY8C24693 Device



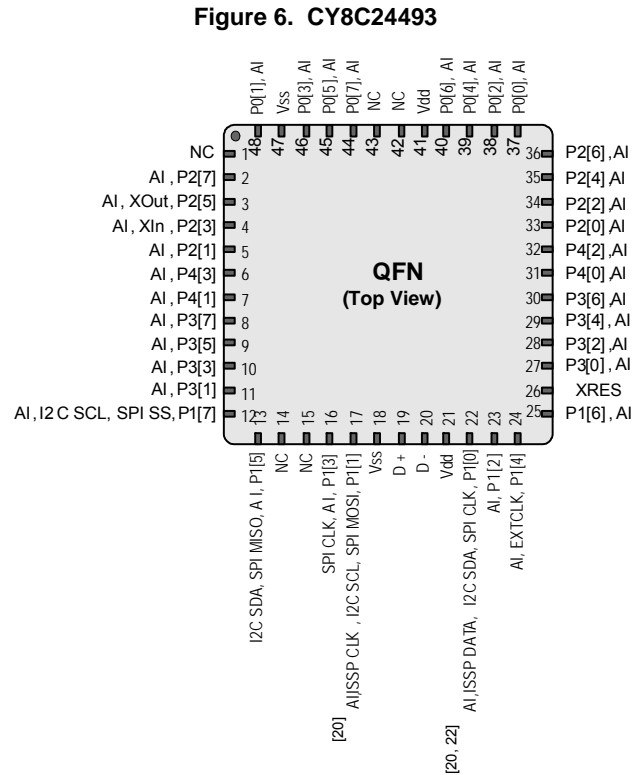
Notes

- 14. 38 GPIOs.
- 15. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.
- 16. The center pad (CP) on the QFN package must be connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- 17. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- 18. Alternate SPI clock.

48-pin QFN (36 GPIOs (With USB)) [19]

Table 6. Pin Definitions – CY8C24493 [20, 21]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I <sup>2</sup> C SCL, SPI SS
13	IOHR	I	P1[5]	I <sup>2</sup> C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK <sup>[20]</sup> , I <sup>2</sup> C SCL, SPI MOSI
18	Power		V <sub>SS</sub>	Ground connection
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		V <sub>DD</sub>	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA <sup>[20]</sup> , I <sup>2</sup> C SDA, SPI CLK <sup>[22]</sup>
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	



Pin No.	Digital	Analog	Name	Description
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V <sub>DD</sub>	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	
47	Power		V <sub>SS</sub>	Ground connection
48	IOH	I	P0[1]	
CP	Power		V <sub>SS</sub>	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Notes

- 19. 36 GPIOs.
- 20. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- 21. The center pad (CP) on the QFN package must be connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- 22. Alternate SPI clock.



48-pin QFN (OCD) (36 GPIOs) [23]

The 48-pin QFN part is for the CY8C240093 On-Chip Debug (OCD). Note that this part is only used for in-circuit debugging.

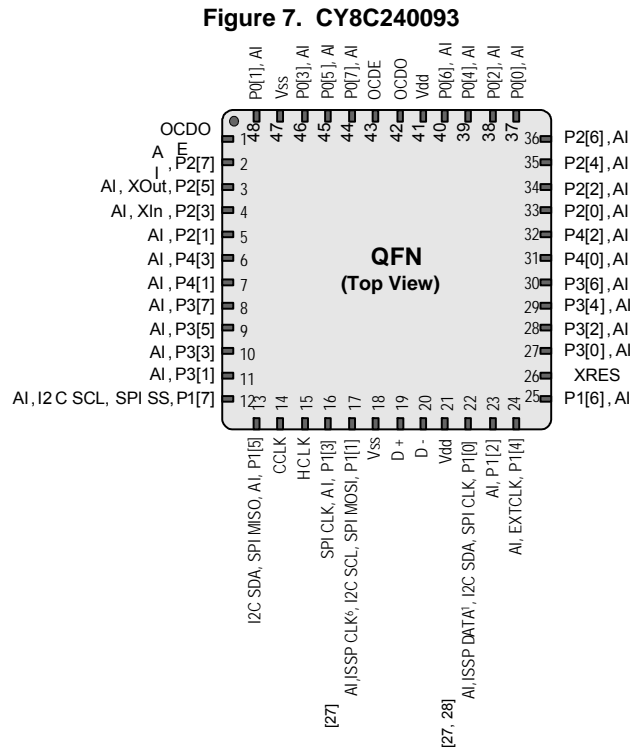
Table 7. Pin Definitions – CY8C240093 [24, 25]

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1 <sup>[26]</sup>			OCDOE	OCD mode direction pin					
2	I/O	I	P2[7]						
3	I/O	I	P2[5]	Crystal output (XOut)					
4	I/O	I	P2[3]	Crystal input (XIn)					
5	I/O	I	P2[1]						
6	I/O	I	P4[3]						
7	I/O	I	P4[1]						
8	I/O	I	P3[7]						
9	I/O	I	P3[5]						
10	I/O	I	P3[3]						
11	I/O	I	P3[1]						
12	IOHR	I	P1[7]	I <sup>2</sup> C SCL, SPI SS					
13	IOHR	I	P1[5]	I <sup>2</sup> C SDA, SPI MISO					
14 <sup>[26]</sup>			CCLK	OCD CPU clock output					
15 <sup>[26]</sup>			HCLK	OCD high speed clock output					
16	IOHR	I	P1[3]	SPI CLK.					
17	IOHR	I	P1[1]	ISSP CLK <sup>[27]</sup> , I <sup>2</sup> C SCL, SPI MOSI					
18	Power		V <sub>SS</sub>	Ground connection					
19	I/O		D+	USB D+					
20	I/O		D-	USB D-					
21	Power		V <sub>DD</sub>	Supply voltage					
22	IOHR	I	P1[0]	ISSP DATA <sup>[27]</sup> , I <sup>2</sup> C SDA, SPI CLK <sup>[28]</sup>					
23	IOHR	I	P1[2]						
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)	37	IOH	I	P0[0]	
25	IOHR	I	P1[6]		38	IOH	I	P0[2]	
26	Input		XRES	Active high external reset with internal pull-down	39	IOH	I	P0[4]	
27	I/O	I	P3[0]		40	IOH	I	P0[6]	
28	I/O	I	P3[2]		41	Power		V <sub>DD</sub>	Supply voltage
29	I/O	I	P3[4]		42 <sup>[26]</sup>			OCDO	OCD even data I/O
30	I/O	I	P3[6]		43 <sup>[26]</sup>			OCDE	OCD odd data output
31	I/O	I	P4[0]		44	IOH	I	P0[7]	
32	I/O	I	P4[2]		45	IOH	I	P0[5]	
33	I/O	I	P2[0]		46	IOH	I	P0[3]	
34	I/O	I	P2[2]		47	Power		V <sub>SS</sub>	Ground connection
35	I/O	I	P2[4]		48	IOH	I	P0[1]	
36	I/O	I	P2[6]		CP	Power		V <sub>SS</sub>	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

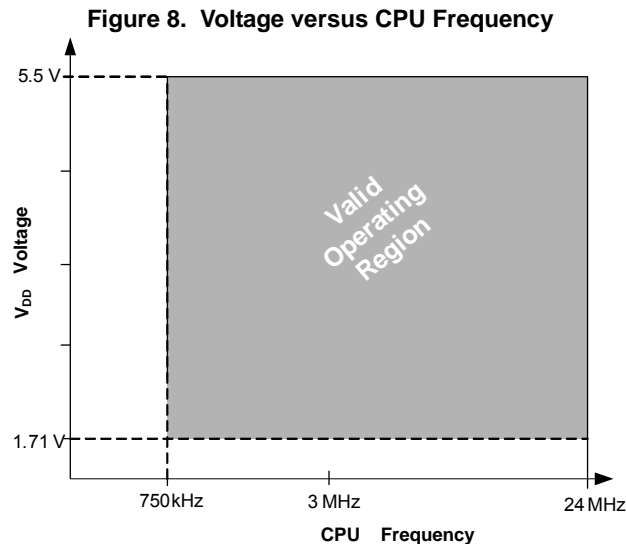
Notes

- 23. 36 GPIOs.
- 24. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.
- 25. The center pad (CP) on the QFN package must be connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- 26. This pin (associated with OCD part only) is required for connecting the device to ICE-Cube In-Circuit Emulator for firmware debugging purpose. To know more about the usage of ICE-Cube, refer to [CY3215-DK PSoC® IN-CIRCUIT EMULATOR KIT GUIDE](#).
- 27. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
- 28. Alternate SPI clock.



## Electrical Specifications (CY8C24193/493)

This section presents the DC and AC electrical specifications of the CY8C24193/493 PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at <http://www.cypress.com/psoc>.



### Absolute Maximum Ratings (CY8C24193/493)

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 8. Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>STG</sub>	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	-55	+25	+125	°C
V <sub>DD</sub>	Supply voltage relative to V <sub>SS</sub>	-	-0.5	-	+6.0	V
V <sub>IO</sub>	DC input voltage	-	V <sub>SS</sub> - 0.5	-	V <sub>DD</sub> + 0.5	V
V <sub>IOZ</sub>	DC voltage applied to tristate	-	V <sub>SS</sub> - 0.5	-	V <sub>DD</sub> + 0.5	V
I <sub>MIO</sub>	Maximum current into any port pin	-	-25	-	+50	mA
ESD	Electro static discharge voltage	Human body model ESD	2000	-	-	V
LU	Latch up current	In accordance with JESD78 standard	-	-	200	mA

### Operating Temperature (CY8C24193/493)

**Table 9. Operating Temperature**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>A</sub>	Ambient temperature	-	-40	-	+85	°C
T <sub>C</sub>	Commercial temperature range	-	0	-	70	°C
T <sub>J</sub>	Operational die temperature	The temperature rise from ambient to junction is package specific. See the <a href="#">Thermal Impedances on page 49</a> . The user must limit the power consumption to comply with this requirement.	-40	-	+100	°C

**DC Chip-Level Specifications (CY8C24193/493)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 10. DC Chip-Level Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DD}$ [29, 43]	Supply voltage	See table <a href="#">DC POR and LVD Specifications (CY8C24093/293/393/693)</a> on page 37	1.71	–	5.50	V
$I_{DD24}$	Supply current, IMO = 24 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz.	–	2.88	4.00	mA
$I_{DD12}$	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz.	–	1.71	2.60	mA
$I_{DD6}$	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz.	–	1.16	1.80	mA
$I_{SB0}$	Deep sleep current	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	1.1	μA
$I_{SB1}$	Standby current with POR, LVD and sleep timer	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	μA
$I_{SB12C}$	Standby current with I <sup>2</sup> C enabled	Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz	–	1.64	–	μA

**Notes**

29. When  $V_{DD}$  remains in the range from 1.71 V to 1.9 V for more than 50 μs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 μs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the  $SR_{POWER\_UP}$  parameter.
30. If powering down in standby sleep mode, to properly detect and recover from a  $V_{DD}$  brown out condition any of the following actions must be taken:
  - a. Bring the device out of sleep before powering down.
  - b. Assure that  $V_{DD}$  falls below 100 mV before powering back up.
  - c. Set the No Buzz bit in the OSC\_CR0 register to keep the voltage monitoring circuit powered during sleep.
  - d. Increase the buzz rate to assure that the falling edge of  $V_{DD}$  is captured. The rate is configured through the PSSDC bits in the SLP\_CFG register. For the referenced registers, refer to the [Technical Reference Manual](#). In deep sleep/standby sleep mode, additional low power voltage monitoring circuitry allows  $V_{DD}$  brown out conditions to be detected and resets the device when  $V_{DD}$  goes lower than 1.1 V at edge rates slower than 1 V/ms.

**DC GPIO Specifications (CY8C24193/493)**

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 1.71 V to 2.4 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 11. 3.0 V to 5.5 V DC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>PU</sub>	Pull-up resistor	–	4	5.60	8	kΩ
V <sub>OH1</sub>	High output voltage Port 2 or 3 pins	I <sub>OH</sub> ≤ 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH2</sub>	High output voltage Port 2 or 3 Pins	I <sub>OH</sub> = 1 mA, maximum of 20 mA source current in all I/Os	V <sub>DD</sub> – 0.90	–	–	V
V <sub>OH3</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH4</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I <sub>OH</sub> = 5 mA, maximum of 20 mA source current in all I/Os	V <sub>DD</sub> – 0.90	–	–	V
V <sub>OH5</sub>	High output voltage Port 1 Pins with LDO Regulator Enabled for 3 V out	I <sub>OH</sub> < 10 μA, V <sub>DD</sub> > 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
V <sub>OH6</sub>	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I <sub>OH</sub> = 5 mA, V <sub>DD</sub> > 3.1 V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V <sub>OH7</sub>	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I <sub>OH</sub> < 10 μA, V <sub>DD</sub> > 2.7 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V <sub>OH8</sub>	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I <sub>OH</sub> = 2 mA, V <sub>DD</sub> > 2.7 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V <sub>OH9</sub>	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I <sub>OH</sub> < 10 μA, V <sub>DD</sub> > 2.7 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
V <sub>OH10</sub>	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I <sub>OH</sub> = 1 mA, V <sub>DD</sub> > 2.7 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V <sub>OL</sub>	Low output voltage	I <sub>OL</sub> = 25 mA, V <sub>DD</sub> > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V <sub>IL</sub>	Input low voltage	–	–	–	0.80	V
V <sub>IH</sub>	Input high voltage	–	2.00	–	–	V
V <sub>H</sub>	Input hysteresis voltage	–	–	80	–	mV
I <sub>IL</sub>	Input leakage (Absolute Value)	–	–	0.00 1	1	μA
C <sub>PIN</sub>	Pin capacitance	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
V <sub>ILLVT3.3</sub>	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
V <sub>IHLVT3.3</sub>	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.4	–	–	V
V <sub>ILLVT5.5</sub>	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
V <sub>IHLVT5.5</sub>	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.7	–	–	V

**Table 12. 2.4 V to 3.0 V DC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>PU</sub>	Pull-up resistor	–	4	5.60	8	kΩ
V <sub>OH1</sub>	High output voltage Port 2 or 3 pins	I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> - 0.20	–	–	V
V <sub>OH2</sub>	High output voltage Port 2 or 3 Pins	I <sub>OH</sub> = 0.2 mA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> - 0.40	–	–	V
V <sub>OH3</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> - 0.20	–	–	V
V <sub>OH4</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I <sub>OH</sub> = 2 mA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> - 0.50	–	–	V
V <sub>OH5A</sub>	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I <sub>OH</sub> < 10 μA, V <sub>DD</sub> > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V <sub>OH6A</sub>	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I <sub>OH</sub> = 1 mA, V <sub>DD</sub> > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V <sub>OL</sub>	Low output voltage	I <sub>OL</sub> = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V <sub>IL</sub>	Input low voltage	–	–	–	0.72	V
V <sub>IH</sub>	Input high voltage	–	1.40	–	–	V
V <sub>H</sub>	Input hysteresis voltage	–	–	80	–	mV
I <sub>IL</sub>	Input leakage (absolute value)	–	–	1	1000	nA
C <sub>PIN</sub>	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
V <sub>ILLVT2.5</sub>	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.7	V	–	
V <sub>IHLVT2.5</sub>	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.2		–	V

**Table 13. 1.71 V to 2.4 V DC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>PU</sub>	Pull-up resistor	–	4	5.60	8	kΩ
V <sub>OH1</sub>	High output voltage Port 2 or 3 pins	I <sub>OH</sub> = 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH2</sub>	High output voltage Port 2 or 3 pins	I <sub>OH</sub> = 0.5 mA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.50	–	–	V
V <sub>OH3</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I <sub>OH</sub> = 100 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH4</sub>	High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I <sub>OH</sub> = 2 mA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.50	–	–	V
V <sub>OL</sub>	Low output voltage	I <sub>OL</sub> = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V
V <sub>IL</sub>	Input low voltage	–	–	–	0.30 × V <sub>DD</sub>	V
V <sub>IH</sub>	Input high voltage	–	0.65 × V <sub>DD</sub>	–	–	V
V <sub>H</sub>	Input hysteresis voltage	–	–	80	–	mV
I <sub>IL</sub>	Input leakage (absolute value)	–	–	1	1000	nA
C <sub>PIN</sub>	Capacitive load on pins	Package and pin dependent temp = 25 °C	0.50	1.70	7	pF

**Table 14. GPIO Current Sink and Source Specifications**

Supply Voltage	Mode	Port 1 per I/O (max)	Port 2/3/4 per I/O (max)	Total Current Even Pins (max)	Total Current Odd Pins (max)	Units
1.71 – 2.4	Sink	5	5	20	30	mA
	Source	2	0.5	10 <sup>[31]</sup>		mA
2.4 – 3.0	Sink	10	10	30	30	mA
	Source	2	0.2	10 <sup>[31]</sup>		mA
3.0 – 5.0	Sink	25	25	60	60	mA
	Source	5	1	20 <sup>[31]</sup>		mA

**Note**

31. Total current (odd + even ports)



**DC Analog Mux Bus Specifications (CY8C24193/493)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 15. DC Analog Mux Bus Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>SW</sub>	Switch resistance to common analog bus	–	–	–	800	Ω
R <sub>GND</sub>	Resistance of initialization switch to V <sub>SS</sub>	–	–	–	800	Ω

The maximum pin voltage for measuring R<sub>SW</sub> and R<sub>GND</sub> is 1.8 V

**DC Low Power Comparator Specifications (CY8C24193/493)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 16. DC Comparator Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>LPC</sub>	Low power comparator (LPC) common mode	Maximum voltage limited to V <sub>DD</sub>	0.2	–	1.8	V
I <sub>LPC</sub>	LPC supply current	–	–	10	80	μA
V <sub>OSLPC</sub>	LPC voltage offset	–	–	2.5	30	mV

**Comparator User Module Electrical Specifications (CY8C24193/493)**

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: –40 °C ≤ TA ≤ 85 °C, 1.71 V ≤ V<sub>DD</sub> ≤ 5.5 V.

**Table 17. Comparator User Module Electrical Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>COMP</sub>	Comparator response time	50 mV overdrive	–	70	100	ns
Offset		Valid from 0.2 V to 1.5 V	–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	μA
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input range		–	0.2		1.5	V

**ADC Electrical Specifications (CY8C24193/493)**
**Table 18. ADC User Module Electrical Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
<b>Input</b>						
V <sub>IN</sub>	Input voltage range	–	0	–	VREFADC	V
C <sub>IIN</sub>	Input capacitance	–	–	–	5	pF
R <sub>IN</sub>	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	1/(500fF × data clock)	1/(400fF × data clock)	1/(300fF × data clock)	Ω
<b>Reference</b>						
V <sub>REFADC</sub>	ADC reference voltage	–	1.14	–	1.26	V
<b>Conversion Rate</b>						
F <sub>CLK</sub>	Data clock	Source is chip's internal main oscillator. See <a href="#">AC Chip-Level Specifications on page 25</a> for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2 <sup>^</sup> Resolution/Data Clock)	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. sample rate = 0.001/ (2 <sup>^</sup> resolution/data clock)	–	5.85	–	ksps
<b>DC Accuracy</b>						
RES	Resolution	Can be set to 8, 9, or 10 bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E <sub>OFFSET</sub>	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E <sub>GAIN</sub>	Gain error	For any resolution	–5	–	+5	%FSR
<b>Power</b>						
I <sub>ADC</sub>	Operating current	–	–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR (V <sub>DD</sub> > 3.0 V)	–	24	–	dB
		PSRR (V <sub>DD</sub> < 3.0 V)	–	30	–	dB

**DC POR and LVD Specifications (CY8C24193/493)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 19. DC POR and LVD Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>POR0</sub>	1.66 V selected in PSoC Designer	V <sub>DD</sub> must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V <sub>POR1</sub>	2.36 V selected in PSoC Designer		–	2.36	2.41	
V <sub>POR2</sub>	2.60 V selected in PSoC Designer		–	2.60	2.66	
V <sub>POR3</sub>	2.82 V selected in PSoC Designer		–	2.82	2.95	
V <sub>LVD0</sub>	2.45 V selected in PSoC Designer	–	2.40	2.45	2.51	V
V <sub>LVD1</sub>	2.71 V selected in PSoC Designer		2.64 <sup>[46]</sup>	2.71	2.78	
V <sub>LVD2</sub>	2.92 V selected in PSoC Designer		2.85 <sup>[47]</sup>	2.92	2.99	
V <sub>LVD3</sub>	3.02 V selected in PSoC Designer		2.95 <sup>[48]</sup>	3.02	3.09	
V <sub>LVD4</sub>	3.13 V selected in PSoC Designer		3.06	3.13	3.20	
V <sub>LVD5</sub>	1.90 V selected in PSoC Designer		1.84	1.90	2.32	
V <sub>LVD6</sub>	1.80 V selected in PSoC Designer		1.75 <sup>[49]</sup>	1.80	1.84	
V <sub>LVD7</sub>	4.73 V selected in PSoC Designer		4.62	4.73	4.83	

**DC Programming Specifications (CY8C24193/493)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 20. DC Programming Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>DDIWRITE</sub>	Supply voltage for flash write operations	–	1.71	–	5.25	V
I <sub>DDP</sub>	Supply current during programming or verify	–	–	5	25	mA
V <sub>ILP</sub>	Input low voltage during programming or verify	See appropriate DC GPIO Specifications (CY8C24093/293/393/693) on page 33	–	–	V <sub>IL</sub>	V
V <sub>IHP</sub>	Input high voltage during programming or verify	See appropriate DC GPIO Specifications (CY8C24093/293/393/693) on page 33	V <sub>IH</sub>	–	–	V
I <sub>ILP</sub>	Input current when Applying V <sub>ILP</sub> to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I <sub>IHP</sub>	Input current when applying V <sub>IHP</sub> to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V <sub>OLP</sub>	Output low voltage during programming or verify		–	–	V <sub>SS</sub> + 0.75	V
V <sub>OHP</sub>	Output high voltage during programming or verify	See appropriate DC GPIO Specifications (CY8C24093/293/393/693) on page 33. For V <sub>DD</sub> > 3V use V <sub>OH4</sub> in Table 36 on page 33.	V <sub>OH</sub>	–	V <sub>DD</sub>	V
Flash <sub>ENPB</sub>	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
Flash <sub>DR</sub>	Flash data retention	Following maximum Flash write cycles; ambient temperature of 55 °C	20	–	–	Years

**Notes**

32. Always greater than 50 mV above V<sub>PPOR1</sub> voltage for falling supply.
33. Always greater than 50 mV above V<sub>PPOR2</sub> voltage for falling supply.
34. Always greater than 50 mV above V<sub>PPOR3</sub> voltage for falling supply.
35. Always greater than 50 mV above V<sub>PPOR0</sub> voltage for falling supply.

### DC I<sup>2</sup>C Specifications (CY8C24193/493)

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 1.71 V to 2.4 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 21. DC I<sup>2</sup>C Specifications<sup>[36]</sup>**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>IL12C</sub>	Input low level	$3.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	$0.25 \times V_{DD}$	V
		$2.5\text{ V} \leq V_{DD} \leq 3.0\text{ V}$	–	–	$0.3 \times V_{DD}$	V
		$1.71\text{ V} \leq V_{DD} \leq 2.4\text{ V}$	–	–	$0.3 \times V_{DD}$	V
V <sub>IH12C</sub>	Input high level	$1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$0.65 \times V_{DD}$	–	$V_{DD} + 0.7\text{ V}$ <sup>[37]</sup>	V

### Shield Driver DC Specifications (CY8C24193/493)

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 1.71 V to 2.4 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 22. Shield Driver DC Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>Ref</sub>	Reference buffer output	$1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.942	–	1.106	V
V <sub>RefHi</sub>	Reference buffer output	$1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.104	–	1.296	V

### DC IDAC Specifications (CY8C24193/493)

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 23. DC IDAC Specifications (8-bit IDAC)**

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–1	–	1	LSB	
IDAC_DNL	Integral nonlinearity	–2	–	2	LSB	
IDAC_Current	Range = 4x	138	–	169	μA	DAC setting = 127 dec
	Range = 8x	138	–	169	μA	DAC setting = 64 dec

**Table 24. DC IDAC Specifications (7-bit IDAC)**

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–1	–	1	LSB	
IDAC_DNL	Integral nonlinearity	–2	–	2	LSB	
IDAC_Current	Range = 4x	137	–	168	μA	DAC setting = 127 dec
	Range = 8x	138	–	169	μA	DAC setting = 64 dec

#### Notes

36. Pull-up resistors on I2C interface cannot be connected to a supply voltage that is more than 0.7 V higher than the CY8C24x93 power supply. See the CY8C24x93 Silicon Errata document for more details.

37. Please refer to Item # 6 of the CY8C24x93 Family.

**AC Chip-Level Specifications (CY8C24193/493)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 25. AC Chip-Level Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>IMO24</sub>	IMO frequency at 24 MHz Setting	–	22.8	24	25.2	MHz
F <sub>IMO12</sub>	IMO frequency at 12 MHz setting	–	11.4	12	12.6	MHz
F <sub>IMO6</sub>	IMO frequency at 6 MHz setting	–	5.7	6.0	6.3	MHz
F <sub>CPU</sub>	CPU frequency	–	0.75	–	25.20	MHz
F <sub>32K1</sub>	ILO frequency	–	15	32	50	kHz
F <sub>32K_U</sub>	ILO untrimmed frequency	–	13	32	82	kHz
DC <sub>IMO</sub>	Duty cycle of IMO	–	40	50	60	%
DC <sub>ILO</sub>	ILO duty cycle	–	40	50	60	%
SR <sub>POWER_UP</sub>	Power supply slew rate	V <sub>DD</sub> slew rate during power-up	–	–	250	V/ms
t <sub>XRST</sub>	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
t <sub>XRST2</sub>	External reset pulse width after power-up <sup>[50]</sup>	Applies after part has booted	10	–	–	μs
t <sub>JIT_IMO</sub> <sup>[39]</sup>	6 MHz IMO cycle-to-cycle jitter (RMS)	–	–	0.7	6.7	ns
	6 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32	–	–	4.3	29.3	ns
	6 MHz IMO period jitter (RMS)	–	–	0.7	3.3	ns
	12 MHz IMO cycle-to-cycle jitter (RMS)	–	–	0.5	5.2	ns
	12 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32	–	–	2.3	5.6	ns
	12 MHz IMO period jitter (RMS)	–	–	0.4	2.6	ns
	24 MHz IMO cycle-to-cycle jitter (RMS)	–	–	1.0	8.7	ns
	24 MHz IMO long term N cycle-to-cycle jitter (RMS); N = 32	–	–	1.4	6.0	ns
	24 MHz IMO period jitter (RMS)	–	–	0.6	4.0	ns

**Note**

38. The minimum required XRES pulse length is longer when programming the device (see Table 55 on page 42).

39. See the Cypress Jitter Specifications application note, [Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054](#) for more information.

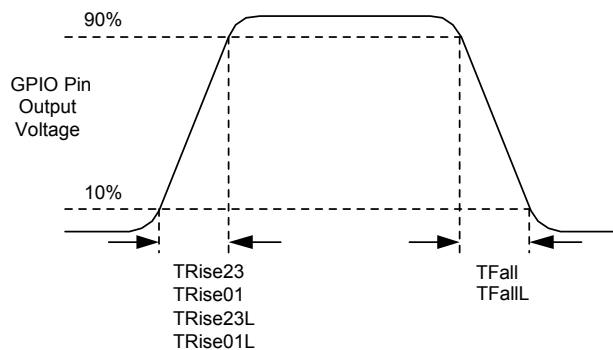
**AC General Purpose I/O Specifications (CY8C24193/493)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 26. AC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>GPIO</sub>	GPIO operating frequency	Normal strong mode Port 0, 1	0	–	6 MHz for 1.71 V < V <sub>DD</sub> < 2.40 V	MHz
			0	–	12 MHz for 2.40 V < V <sub>DD</sub> < 5.50 V	MHz
t <sub>RISE23</sub>	Rise time, strong mode, Cload = 50 pF Ports 2 or 3	V <sub>DD</sub> = 3.0 to 3.6 V, 10% to 90%	15	–	80	ns
t <sub>RISE23L</sub>	Rise time, strong mode low supply, Cload = 50 pF, Ports 2 or 3	V <sub>DD</sub> = 1.71 to 3.0 V, 10% to 90%	15	–	80	ns
t <sub>RISE01</sub>	Rise time, strong mode, Cload = 50 pF Ports 0 or 1	V <sub>DD</sub> = 3.0 to 3.6 V, 10% to 90% LDO enabled or disabled	10	–	50	ns
t <sub>RISE01L</sub>	Rise time, strong mode low supply, Cload = 50 pF, Ports 0 or 1	V <sub>DD</sub> = 1.71 to 3.0 V, 10% to 90% LDO enabled or disabled	10	–	80	ns
t <sub>FALL</sub>	Fall time, strong mode, Cload = 50 pF all ports	V <sub>DD</sub> = 3.0 to 3.6 V, 10% to 90%	10	–	50	ns
t <sub>FALLL</sub>	Fall time, strong mode low supply, Cload = 50 pF, all ports	V <sub>DD</sub> = 1.71 to 3.0 V, 10% to 90%	10	–	70	ns

**Figure 9. GPIO Timing Diagram**



**AC Comparator Specifications (CY8C24193/493)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 27. AC Low Power Comparator Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
t <sub>LPC</sub>	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage.	–	–	100	ns

**AC External Clock Specifications (CY8C24193/493)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

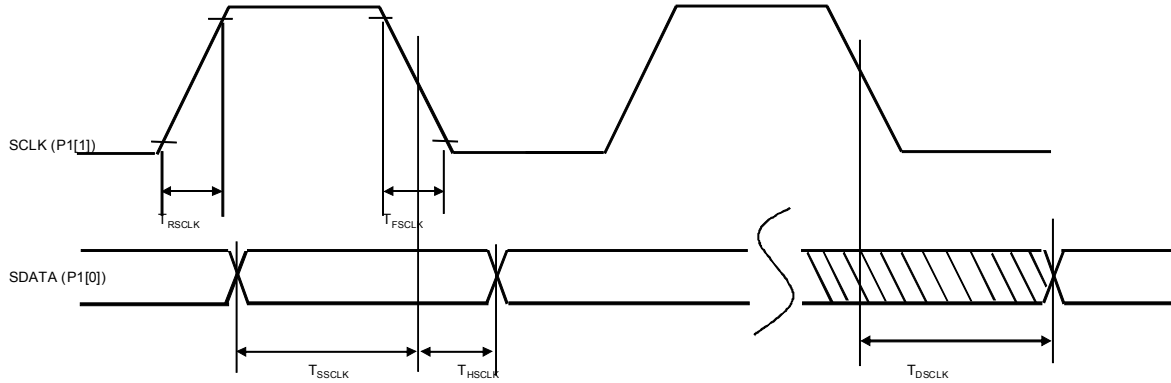
**Table 28. AC External Clock Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>OSCEXT</sub>	Frequency (external oscillator frequency)	–	0.75	–	25.20	MHz
	High period	–	20.60	–	5300	ns
	Low period	–	20.60	–	–	ns
	Power-up IMO to switch	–	150	–	–	μs



AC Programming Specifications (CY8C24193/493)

Figure 10. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 29. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t <sub>RSCLK</sub>	Rise time of SCLK	–	1	–	20	ns
t <sub>FSCLK</sub>	Fall time of SCLK	–	1	–	20	ns
t <sub>SSCLK</sub>	Data setup time to falling edge of SCLK	–	40	–	–	ns
t <sub>HSCLK</sub>	Data hold time from falling edge of SCLK	–	40	–	–	ns
F <sub>SCLK</sub>	Frequency of SCLK	–	0	–	8	MHz
t <sub>ERASEB</sub>	Flash erase time (block)	–	–	–	18	ms
t <sub>WRITE</sub>	Flash block write time	–	–	–	25	ms
t <sub>DSCLK</sub>	Data out delay from falling edge of SCLK	3.6 < V <sub>DD</sub>	–	–	60	ns
t <sub>DSCLK3</sub>	Data out delay from falling edge of SCLK	3.0 ≤ V <sub>DD</sub> ≤ 3.6	–	–	85	ns
t <sub>DSCLK2</sub>	Data out delay from falling edge of SCLK	1.71 ≤ V <sub>DD</sub> ≤ 3.0	–	–	130	ns
t <sub>XRST3</sub>	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	–	–	μs
t <sub>XRES</sub>	XRES pulse length	–	300	–	–	μs
t <sub>VDDWAIT</sub>	V <sub>DD</sub> stable to wait-and-poll hold off	–	0.1	–	1	ms
t <sub>VDDXRES</sub>	V <sub>DD</sub> stable to XRES assertion delay	–	14.27	–	–	ms
t <sub>POLL</sub>	SDAT high pulse time	–	0.01	–	200	ms
t <sub>ACQ</sub>	“Key window” time after a V <sub>DD</sub> ramp acquire event, based on 256 ILO clocks.	–	3.20	–	19.60	ms
t <sub>XRESINI</sub>	“Key window” time after an XRES event, based on 8 ILO clocks	–	98	–	615	μs

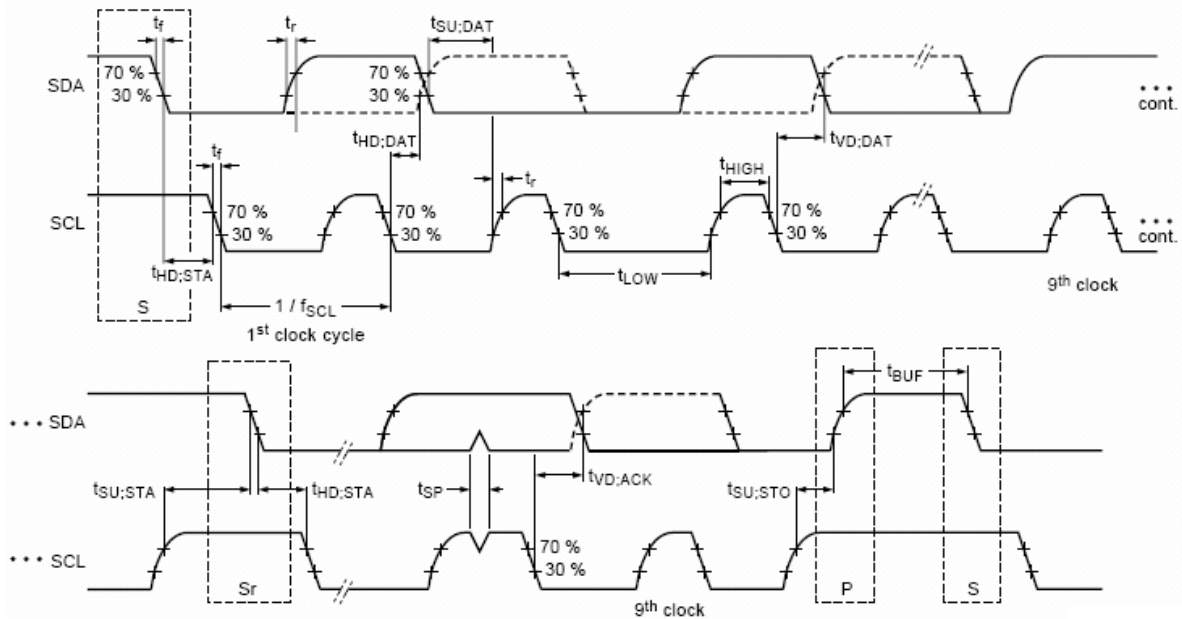
**AC I<sup>2</sup>C Specifications (CY8C24193/493)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 30. AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins**

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f <sub>SCL</sub>	SCL clock frequency	0	100	0	400	kHz
t <sub>HD;STA</sub>	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t <sub>LOW</sub>	LOW period of the SCL clock	4.7	–	1.3	–	µs
t <sub>HIGH</sub>	HIGH Period of the SCL clock	4.0	–	0.6	–	µs
t <sub>SU;STA</sub>	Setup time for a repeated START condition	4.7	–	0.6	–	µs
t <sub>HD;DAT</sub> <sup>[40]</sup>	Data hold time	20	3.45	20	0.90	µs
t <sub>SU;DAT</sub>	Data setup time	250	–	100 <sup>[53]</sup>	–	ns
t <sub>SU;STO</sub>	Setup time for STOP condition	4.0	–	0.6	–	µs
t <sub>BUF</sub>	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t <sub>SP</sub>	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

**Figure 11. Definition for Timing for Fast/Standard Mode on the I<sup>2</sup>C Bus**



**Notes**

40. To wake up from sleep using I2C hardware address match event, I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL. See the CY8C24x93 Silicon Errata document for more details.

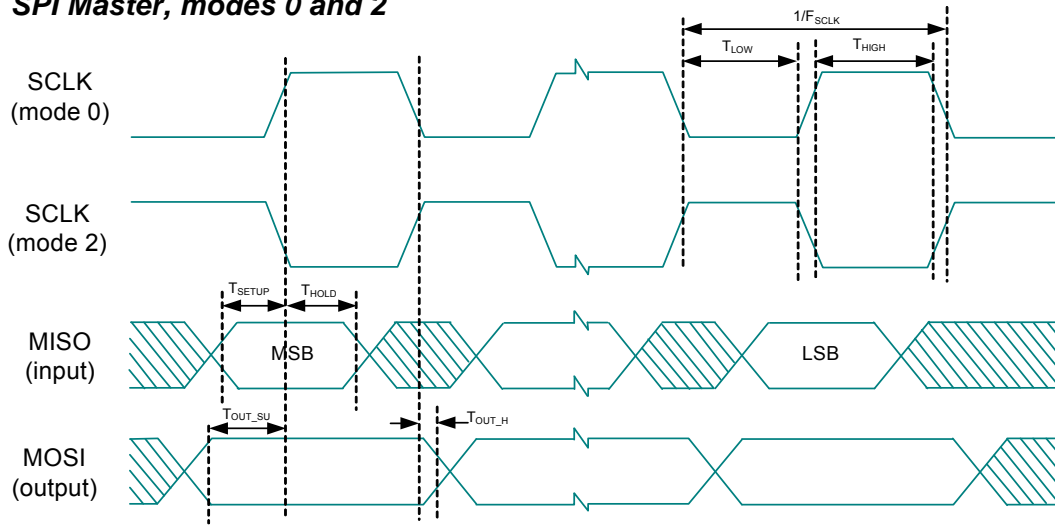
41. A Fast-Mode I<sup>2</sup>C-bus device can be used in a standard mode I<sup>2</sup>C-bus system, but the requirement  $t_{SU;DAT} \geq 250$  ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$  ns (according to the Standard-Mode I<sup>2</sup>C-bus specification) before the SCL line is released.

**Table 31. SPI Master AC Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{SCLK}$	SCLK clock frequency	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$	– –	– –	6 3	MHz MHz
DC	SCLK duty cycle	–	–	50	–	%
$t_{SETUP}$	MISO to SCLK setup time	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$	60 100	– –	– –	ns ns
$t_{HOLD}$	SCLK to MISO hold time	–	40	–	–	ns
$t_{OUT\_VAL}$	SCLK to MOSI valid time	–	–	–	40	ns
$t_{OUT\_H}$	MOSI high time	–	40	–	–	ns

**Figure 12. SPI Master Mode 0 and 2**

**SPI Master, modes 0 and 2**



**Figure 13. SPI Master Mode 1 and 3**

**SPI Master, modes 1 and 3**

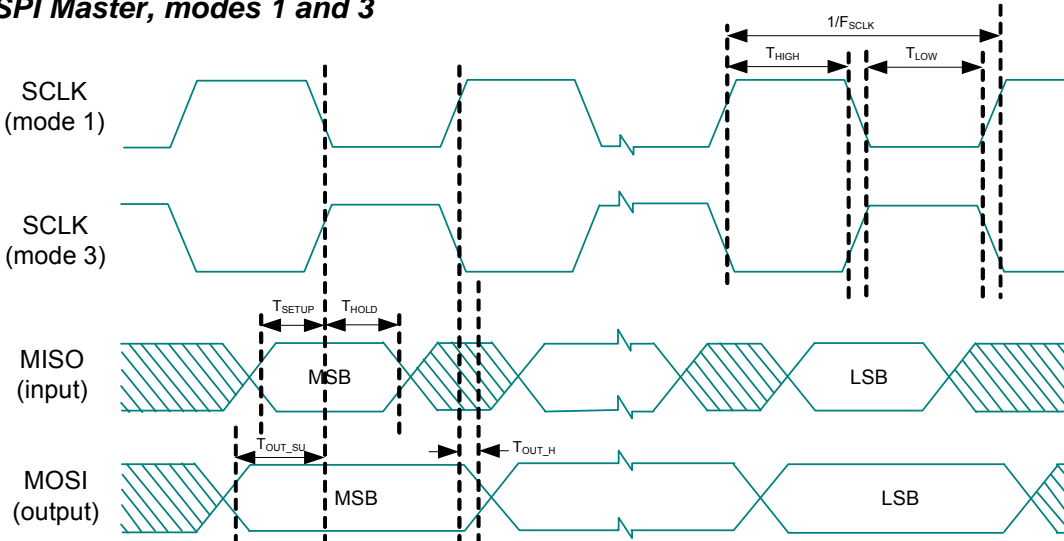


Table 32. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{SCLK}$	SCLK clock frequency	–	–	–	4	MHz
$t_{LOW}$	SCLK low time	–	42	–	–	ns
$t_{HIGH}$	SCLK high time	–	42	–	–	ns
$t_{SETUP}$	MOSI to SCLK setup time	–	30	–	–	ns
$t_{HOLD}$	SCLK to MOSI hold time	–	50	–	–	ns
$t_{SS\_MISO}$	SS high to MISO valid	–	–	–	153	ns
$t_{SCLK\_MISO}$	SCLK to MISO valid	–	–	–	125	ns
$t_{SS\_HIGH}$	SS high time	–	50	–	–	ns
$t_{SS\_CLK}$	Time from SS low to first SCLK	–	$2/SCLK$	–	–	ns
$t_{CLK\_SS}$	Time from last SCLK to SS high	–	$2/SCLK$	–	–	ns

Figure 14. SPI Slave Mode 0 and 2

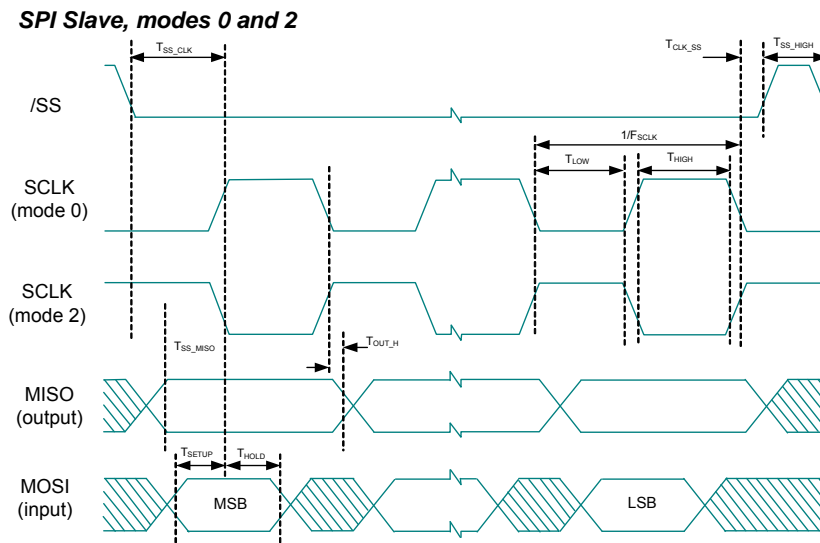
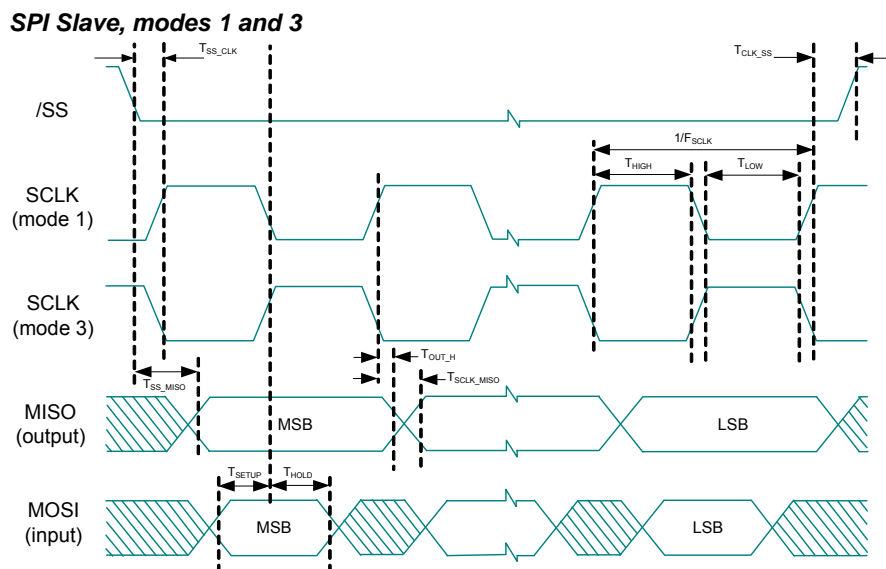


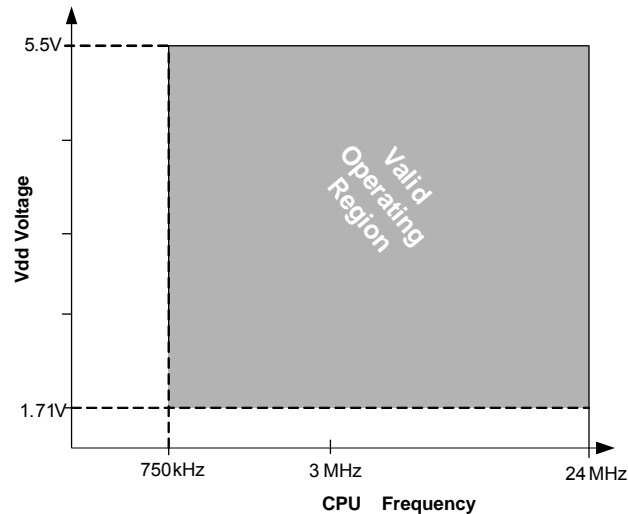
Figure 15. SPI Slave Mode 1 and 3



### Electrical Specifications (CY8C24093/293/393/693)

This section presents the DC and AC electrical specifications of the CY8C24093/293/393/693 PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at <http://www.cypress.com/psoc>.

Figure 16. Voltage versus CPU Frequency



### Absolute Maximum Ratings (CY8C24093/293/393/693)

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 33. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>STG</sub>	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	-55	+25	+125	°C
V <sub>DD</sub>	Supply voltage relative to V <sub>SS</sub>	-	-0.5	-	+6.0	V
V <sub>IO</sub>	DC input voltage	-	V <sub>SS</sub> - 0.5	-	V <sub>DD</sub> + 0.5	V
V <sub>IOZ</sub> <sup>[42]</sup>	DC voltage applied to tristate	-	V <sub>SS</sub> - 0.5	-	V <sub>DD</sub> + 0.5	V
I <sub>MIO</sub>	Maximum current into any port pin	-	-25	-	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	-	-	V
LU	Latch-up current	In accordance with JEDEC standard	-	-	200	mA

### Operating Temperature (CY8C24093/293/393/693)

Table 34. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>A</sub>	Ambient temperature	-	-40	-	+85	°C
T <sub>C</sub>	Commercial temperature range	-	0	-	70	°C
T <sub>J</sub>	Operational die temperature	The temperature rise from ambient to junction is package specific. Refer the <a href="#">Thermal Impedances on page 49</a> . The user must limit the power consumption to comply with this requirement.	-40	-	+100	°C

**Note**

42. Port1 pins are hot-swap capable with I/O configured in High-Z mode, and pin input voltage above V<sub>DD</sub>.

**DC Chip-Level Specifications (CY8C24093/293/393/693)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 35. DC Chip-Level Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DD}$ <sup>[43, 44, 45]</sup>	Supply voltage	No USB activity. Refer the table <a href="#">DC POR and LVD Specifications (CY8C24093/293/393/693)</a> on page 37	1.71	–	5.50	V
$V_{DDUSB}$ <sup>[43, 44, 45]</sup>	Operating voltage	USB activity, USB regulator enabled	4.35	–	5.25	V
		USB activity, USB regulator bypassed	3.15	3.3	3.60	V
$I_{DD24}$	Supply current, IMO = 24 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. No I/O sourcing current	–	–	4.00	mA
$I_{DD12}$	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. No I/O sourcing current	–	–	2.60	mA
$I_{DD6}$	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. No I/O sourcing current	–	–	1.80	mA
$I_{SB0}$	Deep sleep current	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	1.05	μA
$I_{SB1}$	Standby current with POR, LVD and sleep timer	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	μA
$I_{SB12C}$	Standby current with I <sup>2</sup> C enabled	Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz	–	1.64	–	μA

**Notes**

43. When  $V_{DD}$  remains in the range from 1.71 V to 1.9 V for more than 50 μs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 μs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the  $SR_{POWER\_UP}$  parameter.
44. If powering down in standby sleep mode, to properly detect and recover from a  $V_{DD}$  brown out condition any of the following actions must be taken:
  - a. Bring the device out of sleep before powering down.
  - b. Assure that  $V_{DD}$  falls below 100 mV before powering back up.
  - c. Set the No Buzz bit in the OSC\_CR0 register to keep the voltage monitoring circuit powered during sleep.
  - d. Increase the buzz rate to assure that the falling edge of  $V_{DD}$  is captured. The rate is configured through the PSSDC bits in the SLP\_CFG register. For the referenced registers, refer to the CY8C24x93 *Technical Reference Manual*. In deep sleep mode, additional low power voltage monitoring circuitry allows  $V_{DD}$  brown out conditions to be detected for edge rates slower than 1V/ms.
45. For USB mode, the  $V_{DD}$  supply for bus-powered application should be limited to 4.35 V–5.35 V. For self-powered application,  $V_{DD}$  should be 3.15 V–3.45 V.



**DC GPIO Specifications (CY8C24093/293/393/693)**

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 1.71 V to 2.4 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at 25 C and are for design guidance only.

**Table 36. 3.0 V to 5.5 V DC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>PU</sub>	Pull-up resistor	–	4	5.60	8	kΩ
V <sub>OH1</sub>	High output voltage Port 2 or 3 or 4 pins	I <sub>OH</sub> ≤ 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH2</sub>	High output voltage Port 2 or 3 or 4 pins	I <sub>OH</sub> = 1 mA, maximum of 20 mA source current in all I/Os	V <sub>DD</sub> – 0.90	–	–	V
V <sub>OH3</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH4</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I <sub>OH</sub> = 5 mA, maximum of 20 mA source current in all I/Os	V <sub>DD</sub> – 0.90	–	–	V
V <sub>OH5</sub>	High output voltage Port 1 Pins with LDO Regulator Enabled for 3 V out	I <sub>OH</sub> < 10 μA, V <sub>DD</sub> > 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
V <sub>OH6</sub>	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I <sub>OH</sub> = 5 mA, V <sub>DD</sub> > 3.1 V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V <sub>OH7</sub>	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I <sub>OH</sub> < 10 μA, V <sub>DD</sub> > 2.7 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V <sub>OH8</sub>	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I <sub>OH</sub> = 2 mA, V <sub>DD</sub> > 2.7 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V <sub>OH9</sub>	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I <sub>OH</sub> < 10 μA, V <sub>DD</sub> > 2.7 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
V <sub>OH10</sub>	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I <sub>OH</sub> = 1 mA, V <sub>DD</sub> > 2.7 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V <sub>OL</sub>	Low output voltage	I <sub>OL</sub> = 25 mA, V <sub>DD</sub> > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V <sub>IL</sub>	Input low voltage	–	–	–	0.80	V
V <sub>IH</sub>	Input high voltage	–	2.00	–	–	V
V <sub>H</sub>	Input hysteresis voltage	–	–	80	–	mV
I <sub>IL</sub>	Input leakage (Absolute Value)	–	–	0.001	1	μA
C <sub>PIN</sub>	Pin capacitance	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
V <sub>ILLVT3.3</sub>	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
V <sub>IHLVT3.3</sub>	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.4	–	–	V
V <sub>ILLVT5.5</sub>	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
V <sub>IHLVT5.5</sub>	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.7	–	–	V

**Table 37. 2.4 V to 3.0 V DC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>PU</sub>	Pull-up resistor	–	4	5.60	8	kΩ
V <sub>OH1</sub>	High output voltage Port 2 or 3 or 4 pins	I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH2</sub>	High output voltage Port 2 or 3 or 4 pins	I <sub>OH</sub> = 0.2 mA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.40	–	–	V
V <sub>OH3</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH4</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I <sub>OH</sub> = 2 mA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.50	–	–	V
V <sub>OH5A</sub>	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I <sub>OH</sub> < 10 μA, V <sub>DD</sub> > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V <sub>OH6A</sub>	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I <sub>OH</sub> = 1 mA, V <sub>DD</sub> > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V <sub>OL</sub>	Low output voltage	I <sub>OL</sub> = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V <sub>IL</sub>	Input low voltage	–	–	–	0.72	V
V <sub>IH</sub>	Input high voltage	–	1.40	–	–	V
V <sub>H</sub>	Input hysteresis voltage	–	–	80	–	mV
I <sub>IL</sub>	Input leakage (absolute value)	–	–	1	1000	nA
C <sub>PIN</sub>	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
V <sub>ILLVT2.5</sub>	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.7	V	–	
V <sub>IHLVT2.5</sub>	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.2	–	–	V

**Table 38. 1.71 V to 2.4 V DC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>PU</sub>	Pull-up resistor	–	4	5.60	8	kΩ
V <sub>OH1</sub>	High output voltage Port 2 or 3 or 4 pins	I <sub>OH</sub> = 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH2</sub>	High output voltage Port 2 or 3 or 4 pins	I <sub>OH</sub> = 0.5 mA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.50	–	–	V
V <sub>OH3</sub>	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I <sub>OH</sub> = 100 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH4</sub>	High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I <sub>OH</sub> = 2 mA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.50	–	–	V
V <sub>OL</sub>	Low output voltage	I <sub>OL</sub> = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V

**Table 38. 1.71 V to 2.4 V DC GPIO Specifications (continued)**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>IL</sub>	Input low voltage	–	–	–	0.30 × V <sub>DD</sub>	V
V <sub>IH</sub>	Input high voltage	–	0.65 × V <sub>DD</sub>	–	–	V
V <sub>H</sub>	Input hysteresis voltage	–	–	80	–	mV
I <sub>IL</sub>	Input leakage (absolute value)	–	–	1	1000	nA
C <sub>PIN</sub>	Capacitive load on pins	Package and pin dependent temp = 25 °C	0.50	1.70	7	pF

**Table 39. DC Characteristics – USB Interface**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>USBI</sub>	USB D+ pull-up resistance	With idle bus	900	–	1575	Ω
R <sub>USBA</sub>	USB D+ pull-up resistance	While receiving traffic	1425	–	3090	Ω
V <sub>OHUSB</sub>	Static output high	–	2.8	–	3.6	V
V <sub>OLUSB</sub>	Static output low	–	–	–	0.3	V
V <sub>DI</sub>	Differential input sensitivity	–	0.2	–	–	V
V <sub>CM</sub>	Differential input common mode range	–	0.8	–	2.5	V
V <sub>SE</sub>	Single ended receiver threshold	–	0.8	–	2.0	V
C <sub>IN</sub>	Transceiver capacitance	–	–	–	50	pF
I <sub>IO</sub>	High Z state data line leakage	On D+ or D- line	–10	–	+10	μA
R <sub>PS2</sub>	PS/2 pull-up resistance	–	3000	5000	7000	Ω
R <sub>EXT</sub>	External USB series resistor	In series with each USB pin	21.78	22.0	22.22	Ω

**DC Analog Mux Bus Specifications (CY8C24093/293/393/693)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 40. DC Analog Mux Bus Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>SW</sub>	Switch resistance to common analog bus	–	–	–	800	Ω
R <sub>GND</sub>	Resistance of initialization switch to V <sub>SS</sub>	–	–	–	800	Ω

The maximum pin voltage for measuring R<sub>SW</sub> and R<sub>GND</sub> is 1.8 V

**DC Low Power Comparator Specifications (CY8C24093/293/393/693)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 41. DC Comparator Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>LPC</sub>	Low power comparator (LPC) common mode	Maximum voltage limited to V <sub>DD</sub>	0.0	–	1.8	V
I <sub>LPC</sub>	LPC supply current	–	–	10	40	μA
V <sub>OSLPC</sub>	LPC voltage offset	–	–	3	30	mV

**Comparator User Module Electrical Specifications (CY8C24093/293/393/693)**

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range:  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ ,  $1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ .

**Table 42. Comparator User Module Electrical Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$t_{\text{COMP}}$	Comparator response time	50 mV overdrive	–	70	100	ns
Offset		Valid from 0.2 V to $V_{DD} - 0.2\text{ V}$	–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	$\mu\text{A}$
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input range		–	0		1.5	V

**ADC Electrical Specifications (CY8C24093/293/393/693)**
**Table 43. ADC User Module Electrical Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
<b>Input</b>						
$V_{\text{IN}}$	Input voltage range	–	0	–	$V_{\text{REFADC}}$	V
$C_{\text{IIN}}$	Input capacitance	–	–	–	5	pF
$R_{\text{IN}}$	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	$1/(500\text{fF} \times \text{data clock})$	$1/(400\text{fF} \times \text{data clock})$	$1/(300\text{fF} \times \text{data clock})$	$\Omega$
<b>Reference</b>						
$V_{\text{REFADC}}$	ADC reference voltage	–	1.14	–	1.26	V
<b>Conversion Rate</b>						
$F_{\text{CLK}}$	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. sample rate = $0.001 / (2^{\text{Resolution}} / \text{Data Clock})$	–	23.43	–	ksp/s
S10	10-bit sample rate	Data clock set to 6 MHz. sample rate = $0.001 / (2^{\text{resolution}} / \text{data clock})$	–	5.85	–	ksp/s
<b>DC Accuracy</b>						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
$E_{\text{OFFSET}}$	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
$E_{\text{GAIN}}$	Gain error	For any resolution	–5	–	+5	%FSR
<b>Power</b>						
$I_{\text{ADC}}$	Operating current	–	–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR ( $V_{DD} > 3.0\text{ V}$ )	–	24	–	dB
		PSRR ( $V_{DD} < 3.0\text{ V}$ )	–	30	–	dB

**DC POR and LVD Specifications (CY8C24093/293/393/693)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 44. DC POR and LVD Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>POR0</sub>	1.66 V selected in PSoC Designer	V <sub>DD</sub> must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V <sub>POR1</sub>	2.36 V selected in PSoC Designer		–	2.36	2.41	
V <sub>POR2</sub>	2.60 V selected in PSoC Designer		–	2.60	2.66	
V <sub>POR3</sub>	2.82 V selected in PSoC Designer		–	2.82	2.95	
V <sub>LVD0</sub>	2.45 V selected in PSoC Designer	–	2.40	2.45	2.51	V
V <sub>LVD1</sub>	2.71 V selected in PSoC Designer		2.64 <sup>[46]</sup>	2.71	2.78	
V <sub>LVD2</sub>	2.92 V selected in PSoC Designer		2.85 <sup>[47]</sup>	2.92	2.99	
V <sub>LVD3</sub>	3.02 V selected in PSoC Designer		2.95 <sup>[48]</sup>	3.02	3.09	
V <sub>LVD4</sub>	3.13 V selected in PSoC Designer		3.06	3.13	3.20	
V <sub>LVD5</sub>	1.90 V selected in PSoC Designer		1.84	1.90	2.32	
V <sub>LVD6</sub>	1.80 V selected in PSoC Designer		1.75 <sup>[49]</sup>	1.80	1.84	
V <sub>LVD7</sub>	4.73 V selected in PSoC Designer		4.62	4.73	4.83	

**DC Programming Specifications (CY8C24093/293/393/693)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 45. DC Programming Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>DDIWRITE</sub>	Supply voltage for flash write operations	–	1.71	–	5.25	V
I <sub>DDP</sub>	Supply current during programming or verify	–	–	5	25	mA
V <sub>ILP</sub>	Input low voltage during programming or verify	See the appropriate DC GPIO Specifications (CY8C24093/293/393/693) on page 33	–	–	V <sub>IL</sub>	V
V <sub>IHP</sub>	Input high voltage during programming or verify	See the appropriate DC GPIO Specifications (CY8C24093/293/393/693) on page 33	V <sub>IH</sub>	–	–	V
I <sub>ILP</sub>	Input current when Applying V <sub>ILP</sub> to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I <sub>IHP</sub>	Input current when applying V <sub>IHP</sub> to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V <sub>OLP</sub>	Output low voltage during programming or verify	–	–	–	V <sub>SS</sub> + 0.75	V
V <sub>OHP</sub>	Output high voltage during programming or verify	See appropriate DC GPIO Specifications (CY8C24093/293/393/693) on page 33. For V <sub>DD</sub> > 3 V use V <sub>OH4</sub> in Table 34 on page 31.	V <sub>OH</sub>	–	V <sub>DD</sub>	V
Flash <sub>ENPB</sub>	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
Flash <sub>DR</sub>	Flash data retention	Following maximum Flash write cycles; ambient temperature of 55 °C	20	–	–	Years

**Notes**

- 46. Always greater than 50 mV above V<sub>PPOR1</sub> voltage for falling supply.
- 47. Always greater than 50 mV above V<sub>PPOR2</sub> voltage for falling supply.
- 48. Always greater than 50 mV above V<sub>PPOR3</sub> voltage for falling supply.
- 49. Always greater than 50 mV above V<sub>PPOR0</sub> voltage for falling supply.

**DC I<sup>2</sup>C Specifications (CY8C24093/293/393/693)**

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 1.71 V to 2.4 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 46. DC I<sup>2</sup>C Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>IL12C</sub>	Input low level	$3.1\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	$0.25 \times V_{DD}$	V
		$2.5\text{ V} \leq V_{DD} \leq 3.0\text{ V}$	–	–	$0.3 \times V_{DD}$	V
		$1.71\text{ V} \leq V_{DD} \leq 2.4\text{ V}$	–	–	$0.3 \times V_{DD}$	V
V <sub>IH12C</sub>	Input high level	$1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$0.65 \times V_{DD}$	–	–	V

**DC Reference Buffer Specifications (CY8C24093/293/393/693)**

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 1.71 V to 2.4 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

**Table 47. DC Reference Buffer Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>Ref</sub>	Reference buffer output	$1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1	–	1.05	V
V <sub>RefHi</sub>	Reference buffer output	$1.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.2	–	1.25	V

**DC IDAC Specifications (CY8C24093/293/393/693)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 48. DC IDAC Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–4.5	–	+4.5	LSB	
IDAC_INL	Integral nonlinearity	–5	–	+5	LSB	
IDAC_Gain (Source)	Range = 0.5x	6.64	–	22.46	μA	DAC setting = 128 dec
	Range = 1x	14.5	–	47.8	μA	
	Range = 2x	42.7	–	92.3	μA	
	Range = 4x	91.1	–	170	μA	DAC setting = 128 dec
	Range = 8x	184.5	–	426.9	μA	DAC setting = 128 dec

**AC Chip-Level Specifications (CY8C24093/293/393/693)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 49. AC Chip-Level Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>IMO24</sub>	IMO frequency at 24 MHz Setting	–	22.8	24	25.2	MHz
F <sub>IMO12</sub>	IMO frequency at 12 MHz setting	–	11.4	12	12.6	MHz
F <sub>IMO6</sub>	IMO frequency at 6 MHz setting	–	5.7	6.0	6.3	MHz
F <sub>CPU</sub>	CPU frequency	–	0.75	–	25.20	MHz
F <sub>32K1</sub>	ILO frequency	–	15	32	50	kHz
F <sub>32K_U</sub>	ILO untrimmed frequency	–	13	32	82	kHz
DC <sub>IMO</sub>	Duty cycle of IMO	–	40	50	60	%
DC <sub>ILO</sub>	ILO duty cycle	–	40	50	60	%
SR <sub>POWER_UP</sub>	Power supply slew rate	V <sub>DD</sub> slew rate during power-up	–	–	250	V/ms
t <sub>XRST</sub>	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
t <sub>XRST2</sub>	External reset pulse width after power-up <sup>[50]</sup>	Applies after part has booted	10	–	–	μs
t <sub>OS</sub>	Startup time of ECO	–	–	1	–	s
t <sub>JIT_IMO</sub> <sup>[51]</sup>	N=32	6 MHz IMO cycle-to-cycle jitter (RMS)	–	0.7	6.7	ns
		6 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	4.3	29.3	ns
		6 MHz IMO period jitter (RMS)	–	0.7	3.3	ns
		12 MHz IMO cycle-to-cycle jitter (RMS)	–	0.5	5.2	ns
		12 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	2.3	5.6	ns
		12 MHz IMO period jitter (RMS)	–	0.4	2.6	ns
		24 MHz IMO cycle-to-cycle jitter (RMS)	–	1.0	8.7	ns
		24 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	1.4	6.0	ns
		24 MHz IMO period jitter (RMS)	–	0.6	4.0	ns

**Notes**

50. The minimum required XRES pulse length is longer when programming the device (see Table 55 on page 42).

51. Refer to Cypress Jitter Specifications application note, [Understanding Datasheet Jitter Specifications for Cypress Timing Products](#) for more information.



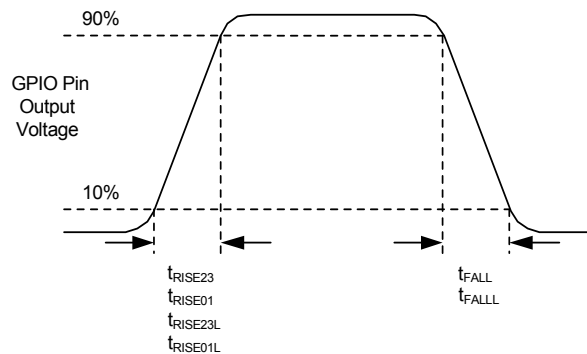
**AC GPIO Specifications (CY8C24093/293/393/693)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 50. AC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{GPIO}$	GPIO operating frequency	Normal strong mode Port 0, 1	0	–	6 MHz for 1.71 V < $V_{DD}$ < 2.40 V 12 MHz for 2.40 V < $V_{DD}$ < 5.50 V	MHz  MHz
$t_{RISE23}$	Rise time, strong mode, Cload = 50 pF Port 2 or 3 or 4 pins	$V_{DD}$ = 3.0 to 3.6 V, 10% to 90%	15	–	80	ns
$t_{RISE23L}$	Rise time, strong mode low supply, Cload = 50 pF, Port 2 or 3 or 4 pins	$V_{DD}$ = 1.71 to 3.0 V, 10% to 90%	15	–	80	ns
$t_{RISE01}$	Rise time, strong mode, Cload = 50 pF Ports 0 or 1	$V_{DD}$ = 3.0 to 3.6 V, 10% to 90% LDO enabled or disabled	10	–	50	ns
$t_{RISE01L}$	Rise time, strong mode low supply, Cload = 50 pF, Ports 0 or 1	$V_{DD}$ = 1.71 to 3.0 V, 10% to 90% LDO enabled or disabled	10	–	80	ns
$t_{FALL}$	Fall time, strong mode, Cload = 50 pF all ports	$V_{DD}$ = 3.0 to 3.6 V, 10% to 90%	10	–	50	ns
$t_{FALLL}$	Fall time, strong mode low supply, Cload = 50 pF, all ports	$V_{DD}$ = 1.71 to 3.0 V, 10% to 90%	10	–	70	ns

**Figure 17. GPIO Timing Diagram**



**Table 51. AC Characteristics – USB Data Timings**

Symbol	Description	Conditions	Min	Typ	Max	Units
t <sub>DRATE</sub>	Full speed data rate	Average bit rate	12 – 0.25%	12	12 + 0.25%	MHz
t <sub>JR1</sub>	Receiver jitter tolerance	To next transition	–18.5	–	18.5	ns
t <sub>JR2</sub>	Receiver jitter tolerance	To pair transition	–9.0	–	9	ns
t <sub>DJ1</sub>	FS Driver jitter	To next transition	–3.5	–	3.5	ns
t <sub>DJ2</sub>	FS Driver jitter	To pair transition	–4.0	–	4.0	ns
t <sub>FDEOP</sub>	Source jitter for differential transition	To SE0 transition	–2.0	–	5	ns
t <sub>FEOPT</sub>	Source SE0 interval of EOP	–	160.0	–	175	ns
t <sub>FEOPR</sub>	Receiver SE0 interval of EOP	–	82.0	–	–	ns
t <sub>FST</sub>	Width of SE0 interval during differential transition	–	–	–	14	ns

**Table 52. AC Characteristics – USB Driver**

Symbol	Description	Conditions	Min	Typ	Max	Units
t <sub>FR</sub>	Transition rise time	50 pF	4	–	20	ns
t <sub>FF</sub>	Transition fall time	50 pF	4	–	20	ns
t <sub>FRFM</sub> <sup>[52]</sup>	Rise/fall time matching	–	90	–	111	%
V <sub>CRS</sub>	Output signal crossover voltage	–	1.30	–	2.00	V

**AC Comparator Specifications (CY8C24093/293/393/693)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 53. AC Low Power Comparator Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
t <sub>LPC</sub>	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage.	–	–	100	ns

**AC External Clock Specifications (CY8C24093/293/393/693)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 54. AC External Clock Specifications**

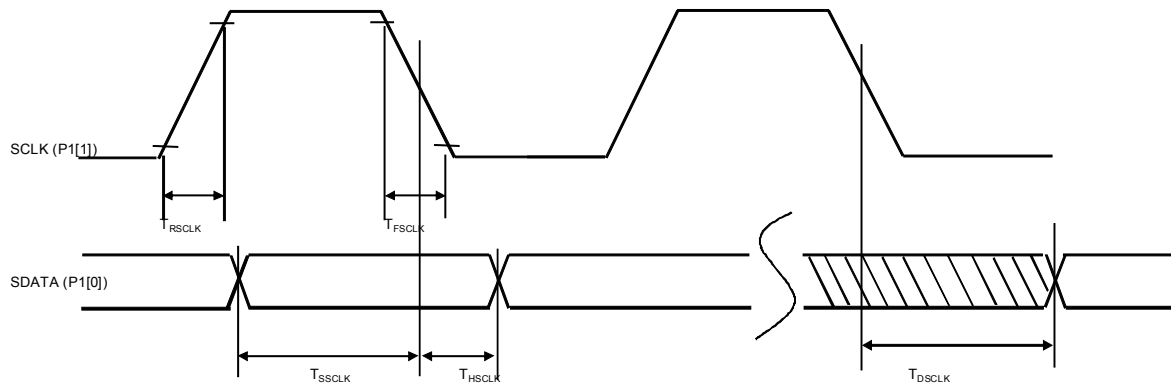
Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>OSCEXT</sub>	Frequency (external oscillator frequency)	–	0.75	–	25.20	MHz
	High period	–	20.60	–	5300	ns
	Low period	–	20.60	–	–	ns
	Power-up IMO to switch	–	150	–	–	μs

**Note**

52. T<sub>FRFM</sub> is not met under all conditions. There is a corner case at lower supply voltages, such as those under 3.3 V. This condition does not affect USB communications. Signal integrity tests show an excellent eye diagram at 3.15 V.

AC Programming Specifications (CY8C24093/293/393/693)

Figure 18. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 55. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$t_{RSCLK}$	Rise time of SCLK	–	1	–	20	ns
$t_{FSCLK}$	Fall time of SCLK	–	1	–	20	ns
$t_{SSCLK}$	Data setup time to falling edge of SCLK	–	40	–	–	ns
$t_{HSCLK}$	Data hold time from falling edge of SCLK	–	40	–	–	ns
$F_{SCLK}$	Frequency of SCLK	–	0	–	8	MHz
$t_{ERASEB}$	Flash erase time (block)	–	–	–	18	ms
$t_{WRITE}$	Flash block write time	–	–	–	25	ms
$t_{DSCLK}$	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	–	–	60	ns
$t_{DSCLK3}$	Data out delay from falling edge of SCLK	$3.0 \leq V_{DD} \leq 3.6$	–	–	85	ns
$t_{DSCLK2}$	Data out delay from falling edge of SCLK	$1.71 \leq V_{DD} \leq 3.0$	–	–	130	ns
$t_{XRST3}$	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	–	–	$\mu$ s
$t_{XRES}$	XRES pulse length	–	300	–	–	$\mu$ s
$t_{VDDWAIT}$	$V_{DD}$ stable to wait-and-poll hold off	–	0.1	–	1	ms
$t_{VDDXRES}$	$V_{DD}$ stable to XRES assertion delay	–	14.27	–	–	ms
$t_{POLL}$	SDATA high pulse time	–	0.01	–	200	ms
$t_{ACQ}$	“Key window” time after a $V_{DD}$ ramp acquire event, based on 256 ILO clocks.	–	3.20	–	19.60	ms
$t_{XRESINI}$	“Key window” time after an XRES event, based on 8 ILO clocks	–	98	–	615	$\mu$ s

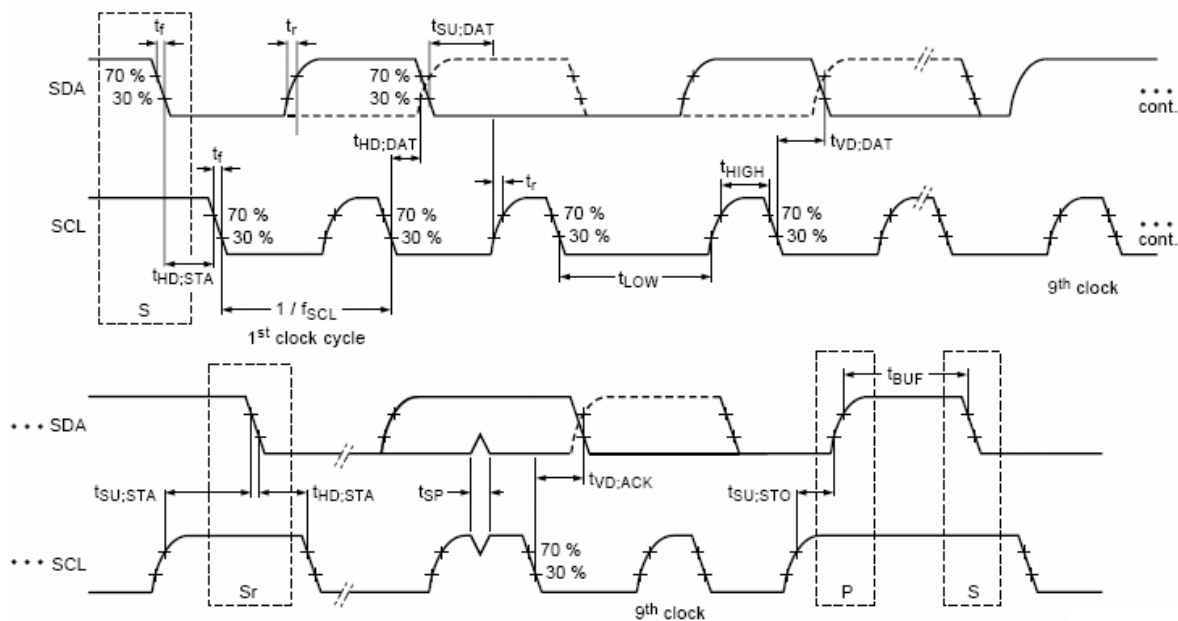
**AC I<sup>2</sup>C Specifications (CY8C24093/293/393/693)**

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 56. AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins**

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f <sub>SCL</sub>	SCL clock frequency	0	100	0	400	kHz
t <sub>HD;STA</sub>	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t <sub>LOW</sub>	LOW period of the SCL clock	4.7	–	1.3	–	µs
t <sub>HIGH</sub>	HIGH Period of the SCL clock	4.0	–	0.6	–	µs
t <sub>SU;STA</sub>	Setup time for a repeated START condition	4.7	–	0.6	–	µs
t <sub>HD;DAT</sub>	Data hold time	0	3.45	0	0.90	µs
t <sub>SU;DAT</sub>	Data setup time	250	–	100 <sup>[53]</sup>	–	ns
t <sub>SU;STO</sub>	Setup time for STOP condition	4.0	–	0.6	–	µs
t <sub>BUF</sub>	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t <sub>SP</sub>	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

**Figure 19. Definition for Timing for Fast/Standard Mode on the I<sup>2</sup>C Bus**



**Note**

53. A Fast-Mode I<sup>2</sup>C-bus device can be used in a standard mode I<sup>2</sup>C-bus system, but the requirement  $t_{SU;DAT} \geq 250$  ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$  ns (according to the Standard-Mode I<sup>2</sup>C-bus specification) before the SCL line is released.

Table 57. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{SCLK}$	SCLK clock frequency	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$	– –	– –	6 3	MHz MHz
DC	SCLK duty cycle	–	–	50	–	%
$t_{SETUP}$	MISO to SCLK setup time	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$	60 100	– –	– –	ns ns
$t_{HOLD}$	SCLK to MISO hold time	–	40	–	–	ns
$t_{OUT\_VAL}$	SCLK to MOSI valid time	–	–	–	40	ns
$t_{OUT\_H}$	MOSI high time	–	40	–	–	ns

Figure 20. SPI Master Mode 0 and 2

**SPI Master, modes 0 and 2**

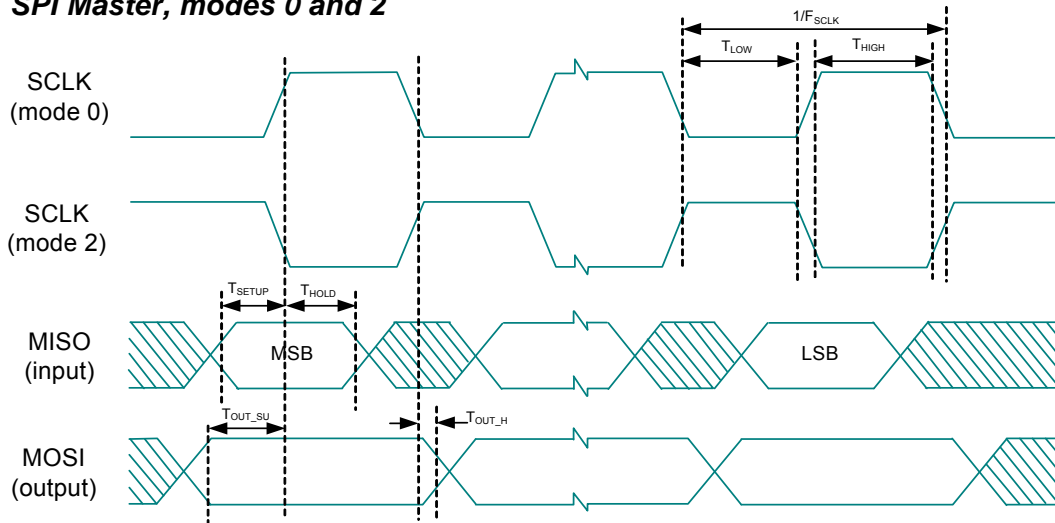


Figure 21. SPI Master Mode 1 and 3

**SPI Master, modes 1 and 3**

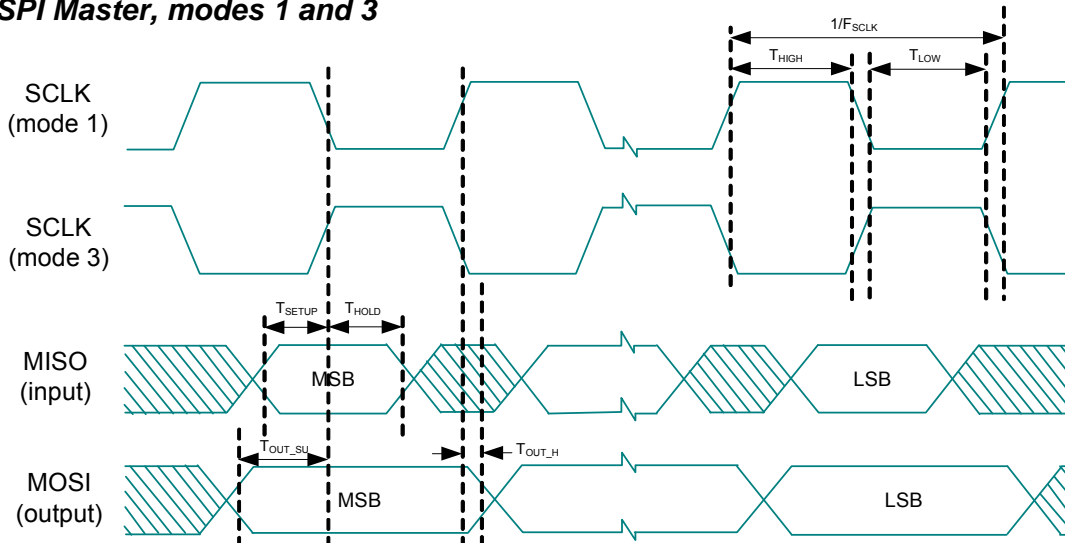


Table 58. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{SCLK}$	SCLK clock frequency	–	–	–	4	MHz
$t_{LOW}$	SCLK low time	–	42	–	–	ns
$t_{HIGH}$	SCLK high time	–	42	–	–	ns
$t_{SETUP}$	MOSI to SCLK setup time	–	30	–	–	ns
$t_{HOLD}$	SCLK to MOSI hold time	–	50	–	–	ns
$t_{SS\_MISO}$	SS high to MISO valid	–	–	–	153	ns
$t_{SCLK\_MISO}$	SCLK to MISO valid	–	–	–	125	ns
$t_{SS\_HIGH}$	SS high time	–	50	–	–	ns
$t_{SS\_CLK}$	Time from SS low to first SCLK	–	2/SCLK	–	–	ns
$t_{CLK\_SS}$	Time from last SCLK to SS high	–	2/SCLK	–	–	ns

Figure 22. SPI Slave Mode 0 and 2

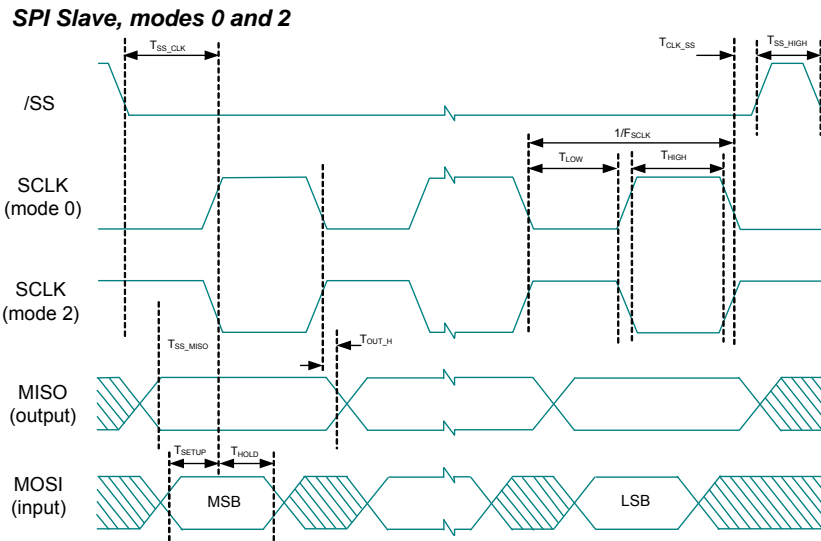
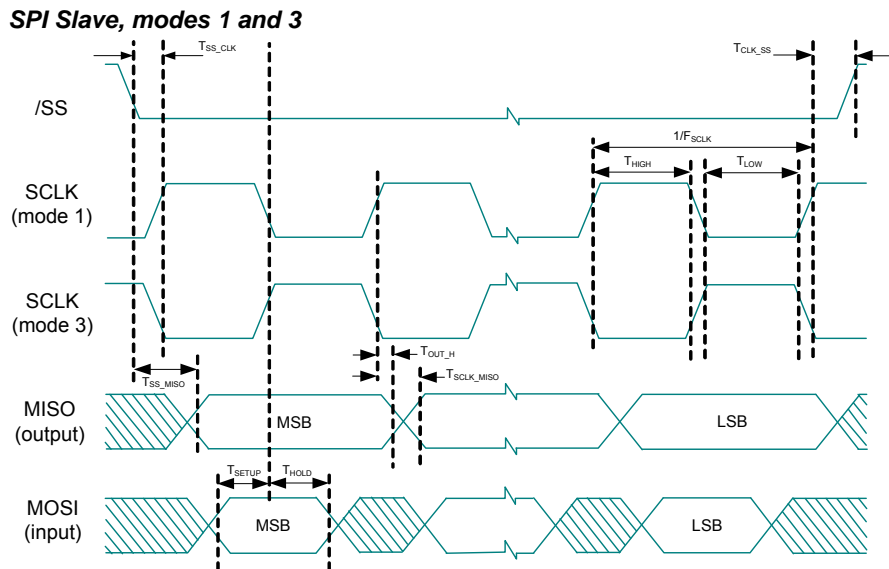


Figure 23. SPI Slave Mode 1 and 3

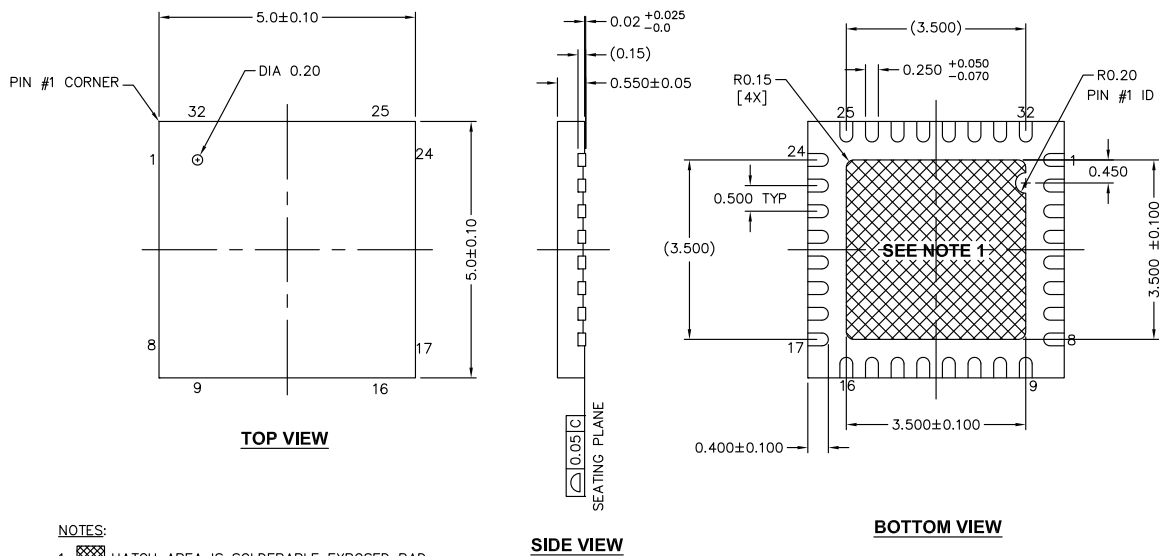


### Packaging Information


This section illustrates the packaging specifications for the CY8C24X93 PSoC device, along with the thermal impedances for each package.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at <http://www.cypress.com/design/MR10161>.

**Figure 24. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168**



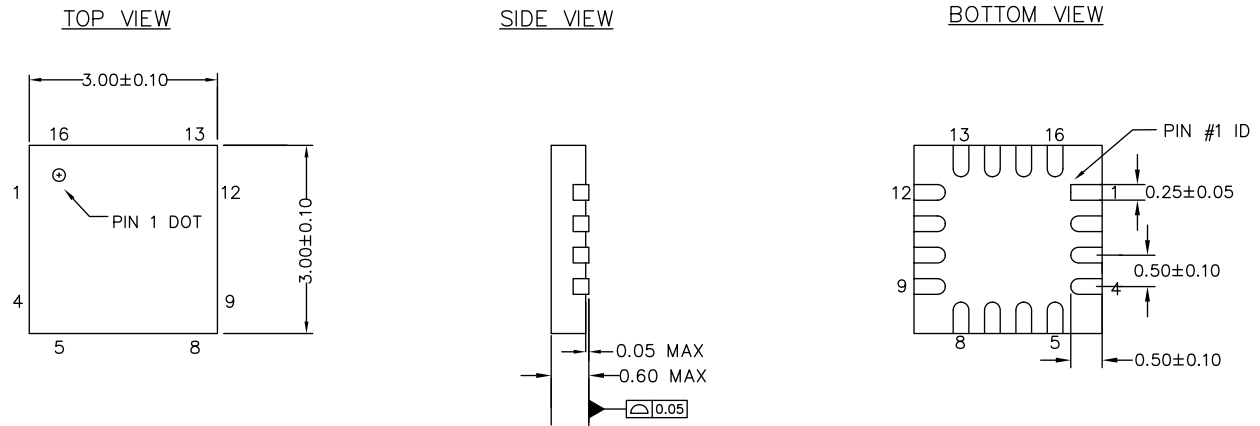
**NOTES:**

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 \*E



Figure 25. 16-pin Chip On Lead (3 x 3 x 0.6 mm) LG16A/LD16A (Sawn) Package Outline, 001-09116

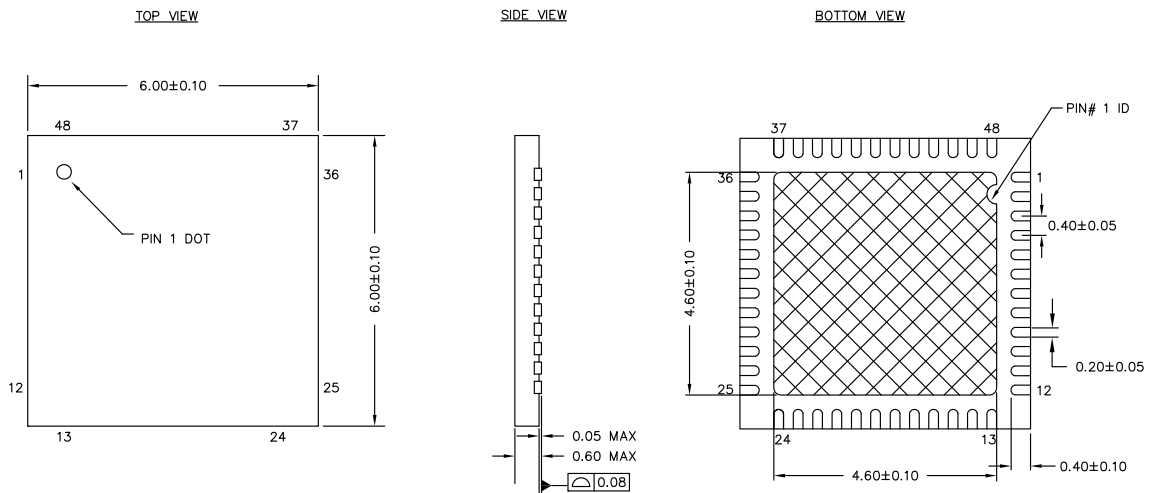


NOTES


1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 \*J

Figure 26. 48-pin QFN (6 x 6 x 0.6 mm) LQ48A 4.6 x 4.6 E-Pad (Sawn) Package Outline, 001-57280

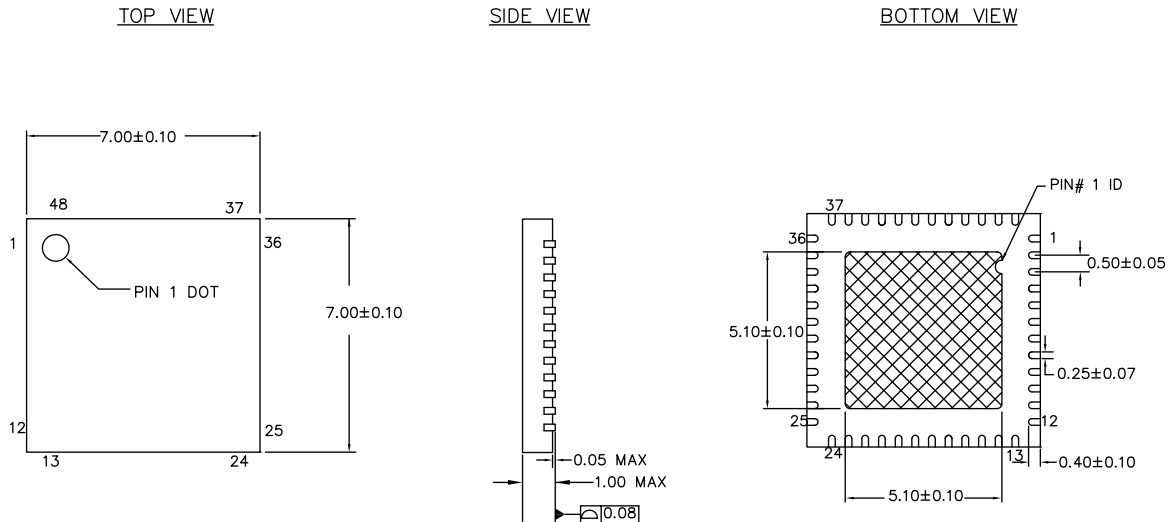


NOTES:


1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±7 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 \*E

Figure 27. 48-pin QFN (7 × 7 × 1.0 mm) LT48A 5.1 × 5.1 E-Pad (SAWN) Package Outline, 001-13191



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 \*H

**Important Notes**

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at [http://www.amkor.com/products/notes\\_papers/MLFAppNote.pdf](http://www.amkor.com/products/notes_papers/MLFAppNote.pdf).
- Pinned vias for thermal conduction are not required for the low power PSoC device.

**Thermal Impedances**

**Table 59. Thermal Impedances per Package**

Package	Typical $\theta_{JA}$ <sup>[54]</sup>	Typical $\theta_{JC}$
16-pin QFN (No Center Pad)	33 °C/W	–
32-pin QFN <sup>[55]</sup>	20 °C/W	–
48-pin QFN (6 × 6 × 0.6 mm) <sup>[55]</sup>	25.20 °C/W	3.04 °C/W
48-pin QFN (7 × 7 × 1.0 mm) <sup>[55]</sup>	18 °C/W	–

**Capacitance on Crystal Pins**

**Table 60. Typical Package Capacitance on Crystal Pins**

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

**Solder Reflow Specifications**

Table 61 shows the solder reflow temperature limits that must not be exceeded.

**Table 61. Solder Reflow Specifications**

Package	Maximum Peak Temperature ( $T_C$ )	Maximum Time above $T_C - 5$ °C
16-pin QFN	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds
48-pin QFN (6 × 6 × 0.6 mm)	260 °C	30 seconds
48-pin QFN (7 × 7 × 1.0 mm)	260 °C	30 seconds

**Notes**

54.  $T_J = T_A + \text{Power} \times \theta_{JA}$ .

55. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

## Development Tool Selection

### Software

#### *PSoC Designer™*

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at <http://www.cypress.com>.

#### *PSoC Programmer*

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at <http://www.cypress.com>.

### Development Kits

All development kits are sold at the Cypress Online Store.

#### *CY3215-DK Basic Development Kit*

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations.

PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29X66A Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466A-24PXI 28-PDIP Chip Samples

### Evaluation Tools

All evaluation tools are sold at the Cypress Online Store. For more information on PSoC 1 kits, visit the link <http://www.cypress.com/?rID=63754>

### Device Programmers

All device programmers are purchased from the Cypress Online Store.

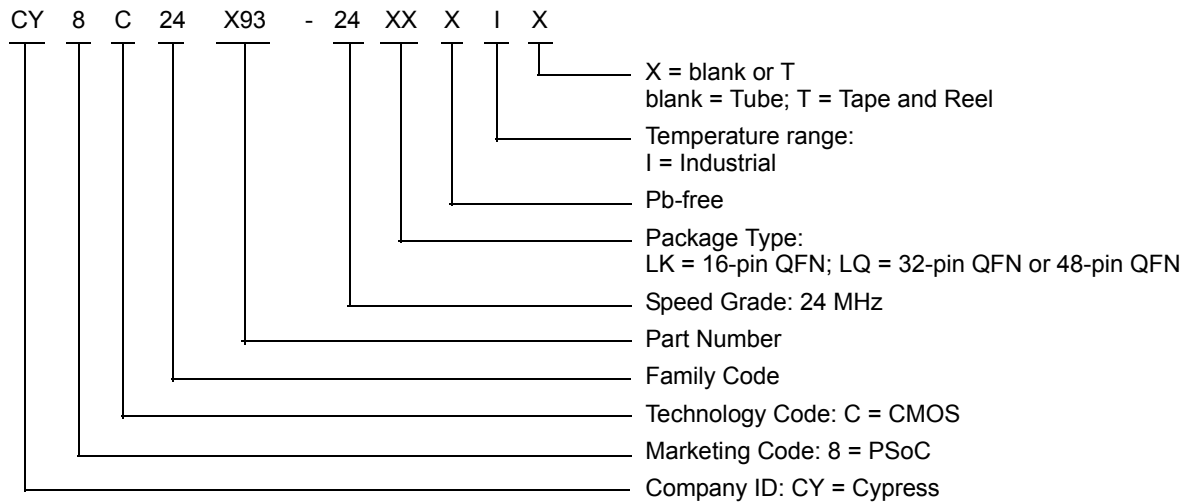
## Ordering Information

The following table lists the CY8C24X93 PSoC devices' key package features and ordering codes.

**Table 62. PSoC Device Key Features and Ordering Information**

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Digital I/O Pins	Analog Inputs <sup>[56]</sup>	XRES Pin	USB	ADC	Supported by OCD
16-pin QFN (3 × 3 × 0.6 mm)	CY8C24093-24LKXI	8 K	1 K	13	13	Yes	No	Yes	No
32-pin QFN (5 × 5 × 0.6 mm)	CY8C24193-24LQXI	8 K	1 K	28	28	Yes	No	Yes	Yes
32-pin QFN (5 × 5 × 0.6 mm)	CY8C24293-24LQXI	16 K	2 K	28	28	Yes	No	Yes	No
48-pin QFN (6 × 6 × 0.6 mm)	CY8C24393-24LQXI	16 K	2 K	34	34	Yes	No	Yes	No
48-pin QFN (7 × 7 × 1.0 mm)	CY8C24493-24LTXI	32 K	2 K	36	36	Yes	Yes	Yes	Yes
48-pin QFN (6 × 6 × 0.6 mm)	CY8C24693-24LQXI	32 K	2 K	34	34	Yes	No	Yes	No
48-pin QFN (OCD) (7 × 7 × 1.0 mm)	CY8C240093-24LTXI	32 K	2 K	36	36	Yes	Yes	Yes	–

## Ordering Code Definitions



**Note**

56. Dual-function Digital I/O Pins also connect to the common analog mux.

## Acronyms

**Table 63. Acronyms Used in this Document**

Acronym	Description
AC	Alternating Current
ADC	Analog-to-Digital Converter
API	Application Programming Interface
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DC	Direct Current
EOP	End Of Packet
FSR	Full Scale Range
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
I <sup>2</sup> C	Inter-Integrated Circuit
ICE	In-Circuit Emulator
IDAC	Digital Analog Converter Current
ILO	Internal Low Speed Oscillator
IMO	Internal Main Oscillator
I/O	Input/Output
ISSP	In-System Serial Programming
LCD	Liquid Crystal Display
LDO	Low Dropout (regulator)
LSB	Least-Significant Bit
LVD	Low Voltage Detect
MCU	Micro-Controller Unit
MIPS	Mega Instructions Per Second
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most-Significant Bit
OCD	On-Chip Debugger
POR	Power On Reset
PPOR	precision power on reset
PSRR	Power Supply Rejection Ratio
PWRSYS	Power System
PSoC <sup>®</sup>	Programmable System-on-Chip
SLIMO	Slow Internal Main Oscillator
SRAM	Static Random Access Memory
SNR	Signal to Noise Ratio
QFN	Quad Flat No-lead
SCL	Serial I2C Clock
SDA	Serial I2C Data
SDATA	Serial ISSP Data
SPI	Serial Peripheral Interface

**Table 63. Acronyms Used in this Document (continued)**

Acronym	Description
SS	Slave Select
SSOP	Shrink Small Outline Package
TC	Test Controller
USB	Universal Serial Bus
USB D+	USB Data+
USB D-	USB Data-
WLCSP	Wafer Level Chip Scale Package
XTAL	Crystal

## Document Conventions

### Units of Measure

Table 64. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
dB	decibel
fF	femtofarad
g	gram
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
KHz	kilohertz
Ksps	kilo samples per second
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
nF	nanofarad
ns	nanosecond
nV	nanovolt
W	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
s	sigma: one standard deviation
V	volt
W	watt

## Reference Documents

- [Technical reference manual for CY8C24x93 devices](#)
- [In-system Serial Programming \(ISSP\) protocol for CY8C24x93 \(AN2026C\)](#)
- [Host Sourced Serial Programming for CY8C24x93 devices \(AN59389\)](#)

## Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

## Glossary

Crosspoint connection	Connection between any GPIO combination via analog multiplexer bus.
Differential non-linearity	Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step.
Hold time	Hold time is the time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.
I <sup>2</sup> C	It is a serial multi-master bus used to connect low speed peripherals to MCU.
Integral nonlinearity	It is a term describing the maximum deviation between the ideal output of a DAC/ADC and the actual output level.
Latch-up current	Current at which the latch-up test is conducted according to JESD78 standard (at 125 degree Celsius)
Power supply rejection ratio (PSRR)	The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device.
Setup time	Period required to prepare a device, machine, process, or system for it to be ready to function.
SPI	Serial peripheral interface is a synchronous serial data link standard.



## Appendix A: Silicon Errata for the CY8C24093/293/393/693 Family

This section describes the errata for the CY8C24093/293/393/693 family. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

### CY8C24093/293/393/693 Qualification Status

Product Status: Production released.

### CY8C24093/293/393/693 Errata Summary

The following Errata items apply to the CY8C24093/293/393/693 datasheet 001-86894.

#### 1. DoubleTimer0 ISR

##### ■ Problem Definition

When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,B0h (PT0\_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice.

##### ■ Parameters Affected

No datasheet parameters are affected.

##### ■ Trigger Condition(S)

Triggered by enabling one-shot mode in the timer, and using the timer to wake from sleep mode.

##### ■ Scope of Impact

The ISR may be executed twice.

##### ■ Workaround

In the ISR, firmware should clear the one-shot bit with a statement such as “and reg[B0h], FDh”

##### ■ Fix Status

Will not be fixed

##### ■ Changes

None

## 2. Missed GPIO Interrupt

### ■ Problem Definition

When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run.

### ■ Parameters Affected

No datasheet parameters are affected.

### ■ Trigger Condition(S)

Triggered by enabling sleep mode, then having GPIO interrupt occur simultaneously with a Timer 0 or Sleep Timer interrupt.

### ■ Scope of Impact

The GPIO interrupt service routine will not be run.

### ■ Workaround

The system should be architected such that a missed GPIO interrupt may be detected. For example, if a GPIO is used to wake the system to perform some function, the system should detect if the function is not performed, and re-issue the GPIO interrupt.

Alternatively, if a GPIO interrupt is required to wake the system, then firmware should disable the Sleep Timer and Timer0.

Alternatively, the ISR's for Sleep Timer and Timer0 should manually check the state of the GPIO to determine if the host system has attempted to generate a GPIO interrupt.

### ■ Fix Status

Will not be fixed

### ■ Changes

None

## 3. Missed Interrupt During Transition to Sleep

### ■ Problem Definition

If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed.

### ■ Parameters Affected

No datasheet parameters are affected.

### ■ Trigger Condition(S)

Triggered by enabling sleep mode just prior to an interrupt.

### ■ Scope of Impact

The relevant interrupt service routine will not be run.

### ■ Workaround

None.

### ■ Fix Status

Will not be fixed

### ■ Changes

None

#### **4. Wakeup from sleep with analog interrupt**

##### **■ Problem Definition**

Device wakes up from sleep when an analog interrupt is trigger

##### **■ Parameters Affected**

No datasheet parameters are affected.

##### **■ Trigger Condition(S)**

Triggered by enabling analog interrupt during sleep mode when device operating temperature is 50 °C or above

##### **■ Scope of Impact**

Device unexpectedly wakes up from sleep

##### **■ Workaround**

Disable the analog interrupt before entering sleep and turn it back on upon wake-up.

##### **■ Fix Status**

Will not be fixed

##### **■ Changes**

None

**5. Wake-up from Sleep with Hardware I2C Address match on Pins P1[0], P1[1]**

■ **Problem Definition**

I2C interface needs 20 ns hold time on SDA line with respect to falling edge of SCL, to wake-up from sleep using I2C hardware address match event.

■ **Parameters Affected**

$t_{HD;DAT}$  increased to 20 ns from 0 ns

■ **Trigger Condition(S)**

This is an issue only when all these three conditions are met:

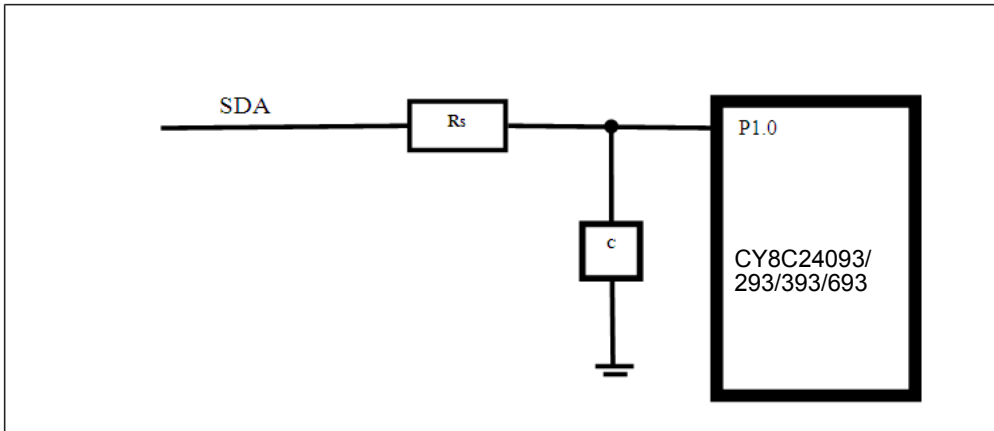
- 1) P1.0 and P1.1 are used as I2C pins,
- 2) Wakeup from sleep with hardware address match feature is enabled, and
- 3) I2C master does not provide 20 ns hold time on SDA with respect to falling edge of SCL.

■ **Scope of Impact**

These trigger conditions cause the device to never wake-up from sleep based on I2C address match event

■ **Workaround**

For a design that meets all of the trigger conditions, the following suggested circuit has to be implemented as a work-around. The R and C values proposed are 100 ohm and 200 pF respectively.



■ **Fix Status**

Will not be fixed

■ **Changes**

None

## 6. I2C Port Pin Pull-up Supply Voltage

### ■ Problem Definition

Pull-up resistor on I2C interface cannot be connected to a supply voltage that is greater than 0.7 V of CY8C24093/293/393/693  $V_{DD}$ .

### ■ Parameters Affected

None.

### ■ Trigger Condition(S)

This problem occurs only when the I2C master is powered at a higher voltage than CY8C24093/293/393/693.

### ■ Scope of Impact

This trigger condition will corrupt the I2C communication between the I2C host and the CY8C24093/293/393/693 controller.

### ■ Workaround

I2C master cannot be powered at a supply voltage that is greater than 0.7 V compared to CY8C24093/293/393/693 supply voltage.

### ■ Fix Status

Will not be fixed

### ■ Changes

None

## 7. Port1 Pin Voltage

### ■ Problem Definition

Pull-up resistor on port1 pins cannot be connected to a voltage that is greater than 0.7 V higher than CY8C24093/293/393/693  $V_{DD}$ .

### ■ Parameters Affected

None.

### ■ Trigger Condition(S)

This problem occurs only when port1 pins are at voltage 0.7 V higher than  $V_{DD}$  of CY8C24093/293/393/693.

### ■ Scope of Impact

This trigger condition will not allow CY8C24093/293/393/693 to drive the output signal on port1 pins, input path is unaffected by this condition.

### ■ Workaround

Port1 should not be connected to a higher voltage than  $V_{DD}$  of CY8C24093/293/393/693.

### ■ Fix Status

Will not be fixed

### ■ Changes

None

## Appendix B: Silicon Errata for the PSoC® CY8C24193/493 Families

This section describes the errata for the PSoC® CY8C24193/493 families. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

### CY8C24193/493 Qualification Status

Product Status: Production released.

### CY8C24193/493 Errata Summary

The following Errata items apply to the CY8C24193/493 datasheet 001-86894.

#### 1. Wakeup from sleep may intermittently fail

##### ■ Problem Definition

When the device is put to sleep in Standby or I2C\_USB Mode and the bandgap circuit is refreshed less frequently than every 8 ms (default), the device may not come out of sleep when a sleep-ending input is received.

##### ■ Parameters Affected

None

##### ■ Trigger Condition(S)

By default, when the device is in the Standby or I2C\_USB sleep modes, the bandgap circuit is powered-up approximately every 8 ms to facilitate detection of POR or LVD events. This interval can be lengthened or the periodic power-up disabled to reduce sleep current by setting the ALT\_BUZZ bits in the SLP\_CFG2 register or the Disable Buzz bit in the OSC\_CR0 register respectively. If the bandgap circuit refresh interval is set longer than the default 8 ms, the device may fail to wakeup from sleep and enter a locked up state that can only be recovered by Watchdog Reset, XRES, or POR.

##### ■ Scope of Impact

The trigger conditions outlined above may cause the device to never wakeup.

##### ■ Workaround

Prior to entering Standby or I2C\_USB sleep modes, do not lengthen or disable the bandgap refresh interval by manipulating the ALT\_BUZZ bits in the SLP\_CFG2 register or the Disable Buzz bit in the OSC\_CR0 register respectively.

##### ■ Fix Status

This issue will not be corrected in the next silicon revision.

## 2. I<sup>2</sup>C Errors

### ■ Problem Definition

The I<sup>2</sup>C block exhibits occasional data and bus corruption errors when the I<sup>2</sup>C master initiates transactions while the device is transitioning in to or out of sleep mode.

### ■ Parameters Affected

Affects reliability of I<sup>2</sup>C communication to device, and between I<sup>2</sup>C master and third party I<sup>2</sup>C slaves.

### ■ Trigger Condition(S)

Triggered by transitions into and out of the device's sleep mode.

### ■ Scope of Impact

Data errors result in incorrect data reported to the I<sup>2</sup>C master, or incorrect data received from the master by the device. Bus corruption errors can corrupt data in transactions between the I<sup>2</sup>C master and third party I<sup>2</sup>C slaves.

### ■ Workaround

Firmware workarounds are available in firmware. Generally the workaround consists of disconnecting the I<sup>2</sup>C block from the bus prior to going to sleep modes. I<sup>2</sup>C transactions during sleep are supported by a protocol in which the master wakes the device prior to the I<sup>2</sup>C transaction.

### ■ Fix Status

To be fixed in future silicon.

### ■ Changes

None

## 3. DoubleTimer0 ISR

### ■ Problem Definition

When programmable timer 0 is used in "one-shot" mode by setting bit 1 of register 0.B0h (PT0\_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice.

### ■ Parameters Affected

No datasheet parameters are affected.

### ■ Trigger Condition(S)

Triggered by enabling one-shot mode in the timer, and using the timer to wake from sleep mode.

### ■ Scope of Impact

The ISR may be executed twice.

### ■ Workaround

In the ISR, firmware should clear the one-shot bit with a statement such as `"and reg[B0h], FDh"`

### ■ Fix Status

Will not be fixed

### ■ Changes

None

#### 4. Missed GPIO Interrupt

##### ■ Problem Definition

When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run.

##### ■ Parameters Affected

No datasheet parameters are affected.

##### ■ Trigger Condition(S)

Triggered by enabling sleep mode, then having GPIO interrupt occur simultaneously with a Timer 0 or Sleep Timer interrupt.

##### ■ Scope of Impact

The GPIO interrupt service routine will not be run.

##### ■ Workaround

The system should be architected such that a missed GPIO interrupt may be detected. For example, if a GPIO is used to wake the system to perform some function, the system should detect if the function is not performed, and re-issue the GPIO interrupt.

Alternatively, if a GPIO interrupt is required to wake the system, then firmware should disable the Sleep Timer and Timer0.

Alternatively, the ISR's for Sleep Timer and Timer0 should manually check the state of the GPIO to determine if the host system has attempted to generate a GPIO interrupt.

##### ■ Fix Status

Will not be fixed

##### ■ Changes

None

#### 5. Missed Interrupt During Transition to Sleep

##### ■ Problem Definition

If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed.

##### ■ Parameters Affected

No datasheet parameters are affected.

##### ■ Trigger Condition(S)

Triggered by enabling sleep mode just prior to an interrupt.

##### ■ Scope of Impact

The relevant interrupt service routine will not be run.

##### ■ Workaround

None.

##### ■ Fix Status

Will not be fixed

##### ■ Changes

None



## **6. Wakeup from sleep with analog interrupt**

### ■ **Problem Definition**

Device wakes up from sleep when an analog interrupt is trigger

### ■ **Parameters Affected**

No datasheet parameters are affected.

### ■ **Trigger Condition(S)**

Triggered by enabling analog interrupt during sleep mode when device operating temperature is 50 °C or above

### ■ **Scope of Impact**

Device unexpectedly wakes up from sleep

### ■ **Workaround**

Disable the analog interrupt before entering sleep and turn it back on upon wakeup.

### ■ **Fix Status**

Will not be fixed

### ■ **Changes**

None

## Document History Page

Document Title: CY8C24X93, PSoC® Programmable System-on-Chip				
Document Number: 001-86894				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3947416	AMKA	04/02/2013	New data sheet.
*A	3971208	AMKA	04/30/2013	Changed status from Preliminary to Final. Updated <a href="#">Features</a> . Updated <a href="#">PSoC® Functional Overview</a> (Updated <a href="#">Analog system</a> (Updated <a href="#">IDAC</a> ), updated <a href="#">Additional System Resources</a> ). Updated <a href="#">Ordering Information</a> (Updated part numbers).
*B	4009884	AMKA	05/24/2013	Updated <a href="#">Logic Block Diagram</a> . Updated <a href="#">Getting Started</a> (Updated <a href="#">Silicon Errata</a> ). Updated <a href="#">Development Tool Selection</a> (Updated <a href="#">Evaluation Tools</a> (Removed CY3210-PSoCEval1)). Updated <a href="#">Reference Documents</a> . Added <a href="#">Appendix A: Silicon Errata for the CY8C24093/293/393/693 Family</a> . Added <a href="#">Appendix B: Silicon Errata for the PSoC® CY8C24193/493 Families</a> .
*C	5262060	ASRI	05/06/2016	Updated hyperlinks across the document. Added <a href="#">More Information</a> . Updated <a href="#">Packaging Information</a> : spec 001-09116 – Changed revision from *H to *J. spec 001-13191 – Changed revision from *G to *H. Updated to new template. Completing Sunset Review.

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