TS512M~2GSDC

Secure Digital Card

Description

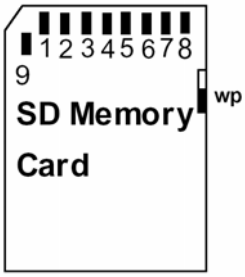
Secure Digital Card of high capacity but economic cost. It is specifically designed to meet the security, capacity and small form factor requirements in newly emerging audio and video consumer electronic devices.Transcend Secure Digital Card can lead you to a colorful digital world.

Features

- ROHS compliant product
- Operating Voltage: 2.7 ~ 3.6V
- Operating Temperature: -25 ~ 85°C
- Insertion/removal durability: 10,000 cycles
- Fully compatible with SD card spec. v1.1
- Mechanical Write Protection Switch
- Forward compatibility to MultiMediaCard Version 2.11
- Supports Copy Protection for Recorded Media(CPRM) for music and other commercial media
- Form Factor: 24mm x 32mm x 2.1mm

Placement

Front

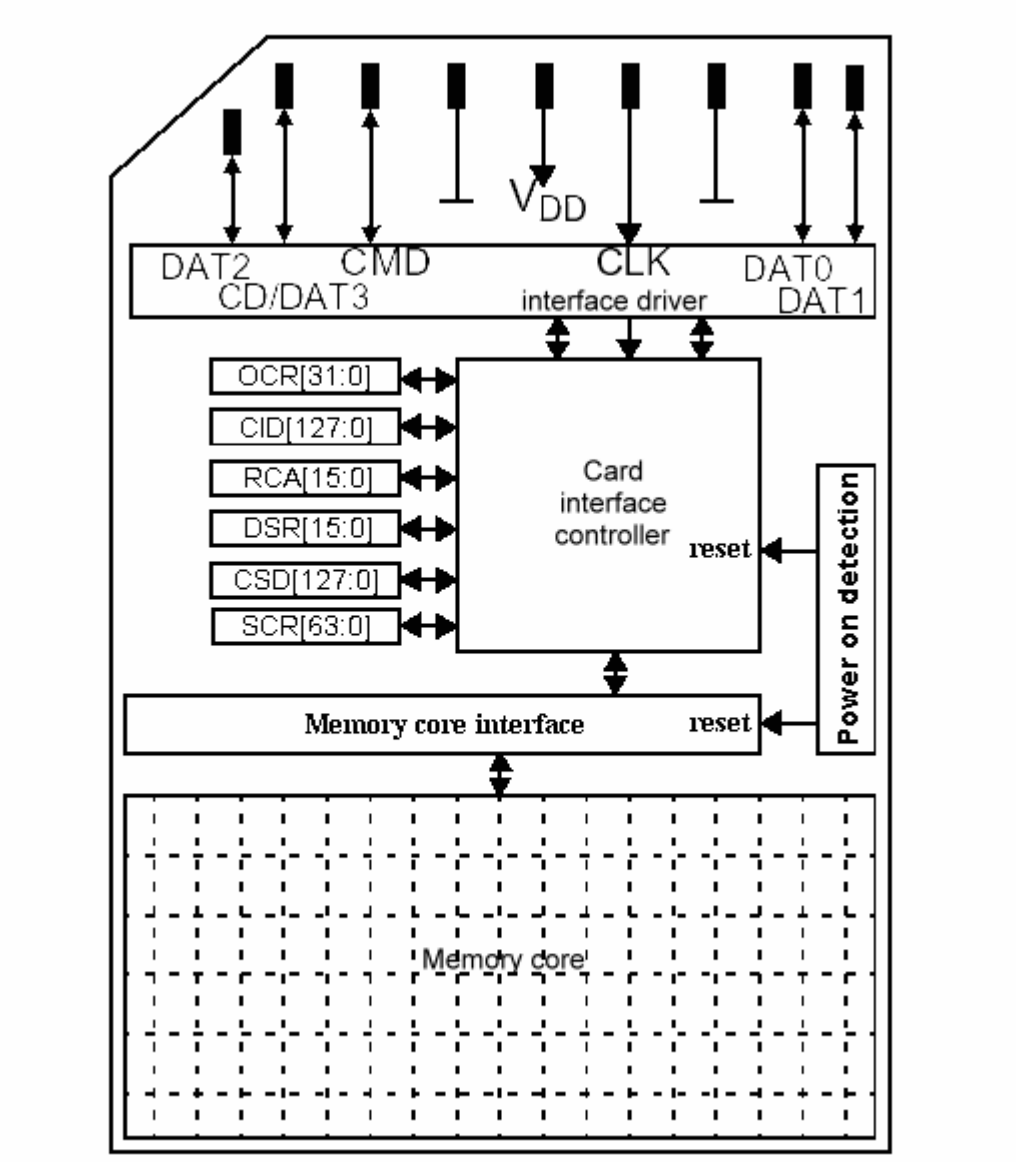


Back

Pin Definition

Pin No.	SD Mode			SPI Mode		
	Name	Type	Description	Name	Type	Description
1	CD/DAT	I/O/PP[3]	Card Detect/Data Line [Bit3]	CS	I	Chip Select (neg true)
2	CMD	PP	Command/Response	DI	I	Data In
3	V_{SS1}	S	Supply voltage ground	VSS	S	Supply voltage ground
4	V_{DD}	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	V_{SS2}	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit1]	RSV		
9	DAT2	I/O/PP	Data Line [Bit2]	RSV		

Architecture



Bus Operating Conditions

• General

Parameter	Symbol	Min.	Max.	Unit	Remark
Peak voltage on all lines		-0.3	VDD+0.3	V	
All Inputs					
Input Leakage Current		-10	10	μA	
All Outputs					
Output Leakage Current		-10	10	μA	

• Power Supply Voltage

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage	V_{DD}	2.0	3.6	V	CMD0, 15,55,ACMD41 commands
Supply voltage specified in OCR register		2.7	3.6	V	Except CMD0, 15,55, ACMD41 commands
Supply voltage differentials (V_{SS1}, V_{SS2})		-0.3	0.3	V	
Power up time			250	ms	From 0v to V_{DD} Min.

Note. The current consumption of any card during the power-up procedure must not exceed 10 mA.

• Bus Signal Line Load

The total capacitance C_L the CLK line of the SD Memory Card bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{CARD} of each card connected to this line:
$C_L = C_{HOST} + C_{BUS} + N*C_{CARD}$

Where N is the number of connected cards. Requiring the sum of the host and bus capacitances not to exceed 30 pF for up to 10 cards, and 40 pF for up to 30 cards, the following values must not be exceeded:

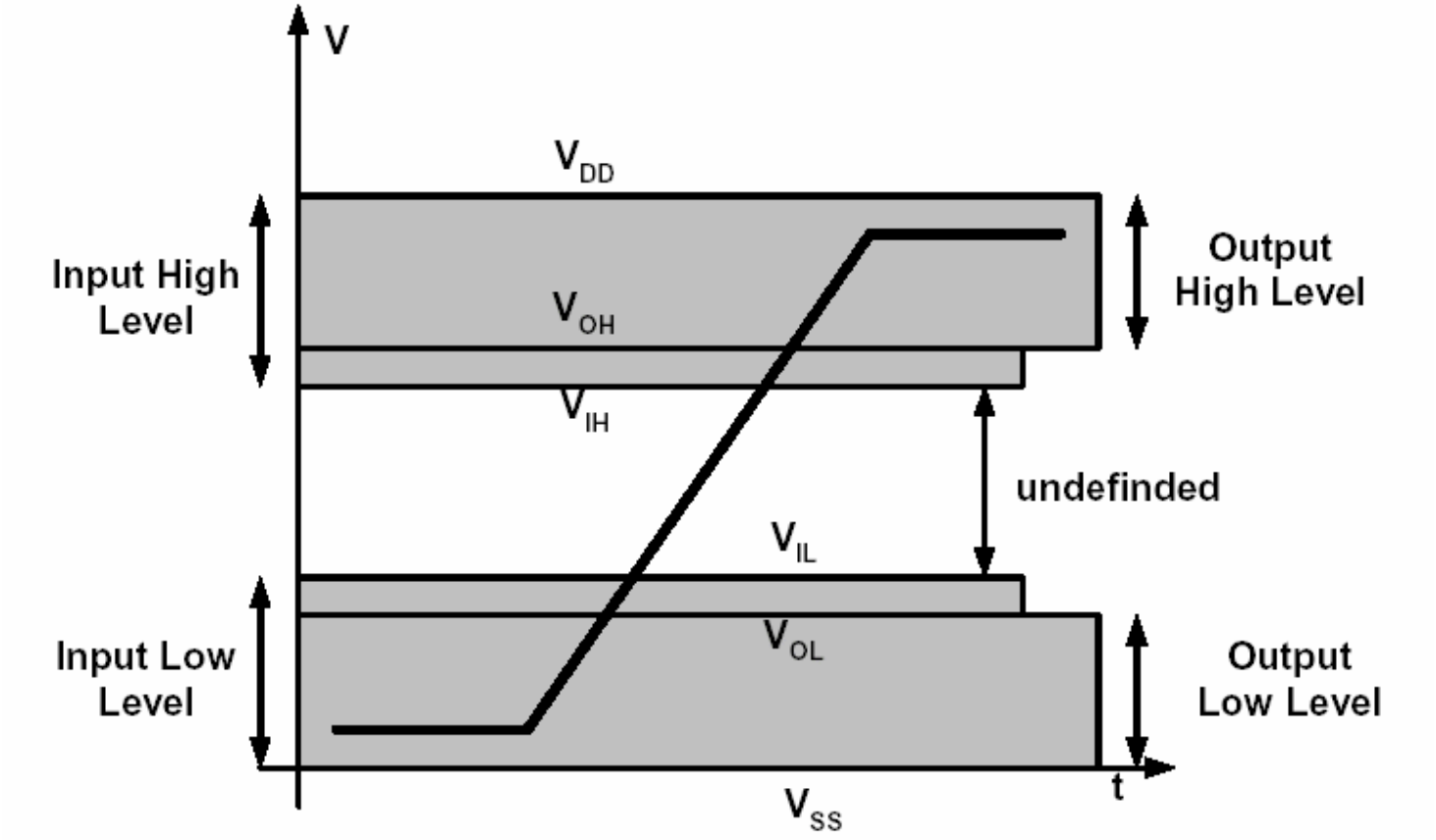
Parameter	Symbol	Min.	Max.	Unit	Remark
Bus signal line capacitance	C_L		100	pF	$f_{PP} \leq 20$ MHz, 7 cards
Single card capacitance	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	$f_{PP} \leq 20$ MHz
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection

Note that the total capacitance of CMD and DAT lines will be consist of C_{HOST}, C_{BUS} and one C_{CARD} only since they are connected separately to the SD Memory Card host.

Parameter	Symbol	Min.	Max.	Unit	Remark
Pull-up resistance	R_{CMD}, R_{DAT}	10	100	kΩ	To prevent bus floating
Bus signal line capacitance	C_L		250	pF	$f_{PP} \leq 5$ MHz, 21 cards

• Bus Signal Levels

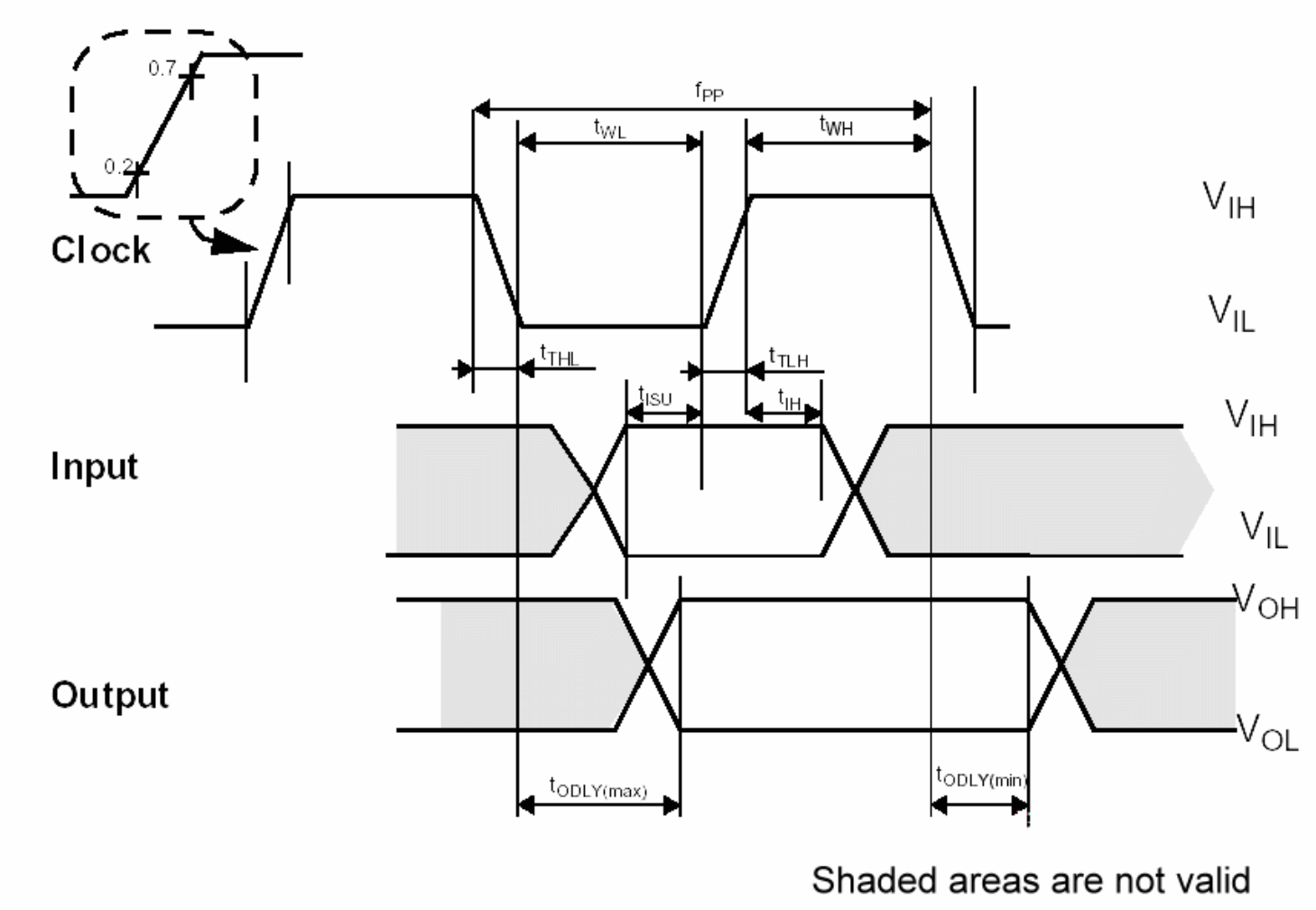
As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range:

Parameter	Symbol	Min.	Max.	Unit	Remark
Output HIGH voltage	V_{OH}	0.75* V_{DD}		V	I_{OH} = -100 µA @V_{DD} min
Output LOW voltage	V_{OL}		0.125* V_{DD}	V	I_{OL} = -100 µA @V_{DD} min
Input HIGH voltage	V_{IH}	0.625* V_{DD}	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} – 0.3	0.25* V_{DD}	V	

• **Bus Timing**



Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	$C_L \leq 100$ pF, (7 cards)
Clock frequency Identification Mode (The low freq. is required for MultiMediaCard compatibility.)	f_{OD}	0	400	KHz	$C_L \leq 250$ pF, (21 cards)
Clock low time	t_{WL}	10		ns	$C_L \leq 100$ pF, (7 cards)
		50		ns	$C_L \leq 250$ pF, (21 cards)
Clock high time	t_{WH}	10		ns	$C_L \leq 100$ pF, (7 cards)
		50		ns	$C_L \leq 250$ pF, (21 cards)
Clock rise time	t_{TLH}		10	ns	$C_L \leq 100$ pF, (7 cards)
			50	ns	$C_L \leq 250$ pF, (21 cards)

Clock fall time	t_{THL}		10	ns	$C_L \leq 100$ pF, (7 cards)
			50	ns	$C_L \leq 250$ pF, (21 cards)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	$C_L \leq 25$ pF, (1 cards)
Input hold time	t_{IH}	5		ns	$C_L \leq 25$ pF, (1 cards)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time	t_{ODLY}	0	14	ns	$C_L \leq 25$ pF, (1 cards)

Reliability and Durability

Temperature	Operation: -25°C / 85°C Storage: -40°C (168h) / 85°C (500h) Junction temperature: max. 95°C
Moisture and corrosion	Operation: 25°C / 95% rel. humidity Storage: 40°C / 93% rel. hum./500h Salt Water Spray: 3% NaCl/35C; 24h acc. MIL STD Method 1009
Durability	10.000 mating cycles; test procedure: tbd.
Bending	10N
Torque	0.15N.m or +/-2.5 deg
Drop test	1.5m free fall
UV light exposure	UV: 254nm, 15Ws/cm² according to ISO 7816-1
Visual inspection Shape and form	No warp page; no mold skin; complete form; no cavities surface smoothness <= -0.1 mm/cm² within contour; no cracks; no pollution (fat, oil dust, etc.)
Minimum moving force of WP witch	40gf (Ensures that the WP switch will not slide while it is inserted to the connector.)
WP Switch cycles	minimum 1000 Cycles(@Slide force 0.4N to 5N)

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