Product Features：

<Common>

- Packaged NAND flash memory with *e*•MMC™ 4.5 interface
- Compliant with *e*•MMC™ Specification Ver.4.4, 4.41 & 4.5
- Bus mode
  - High-speed *e*•MMC™ protocol
  - Provide variable clock frequencies of 0-200MHz.
  - Ten-wire bus (clock, 1 bit command, 8 bit data bus) and a hardware reset.
- Supports three different data bus widths : 1 bit(default), 4 bits, 8 bits
  - Data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52 MHz)
  - Single data rate : up to 200Mbyte/s @ HS200(Host clock @ 200MHz)
  - Dual data rate : up to 104Mbyte/s @ 52MHz
- Supports (Alternate) Boot Operation Mode to provide a simple boot sequence method
- Supports SLEEP/AWAKE (CMD5).
- Host initiated explicit sleep mode for power saving
- Enhanced Write Protection with Permanent and Partial protection options
- Supports Multiple User Data Partition with Enhanced User Data Area options
- Supports Background Operations & High Priority Interrupt (HPI)
- Supports enhanced storage media feature for better reliability
- Operating voltage range :
  - VCCQ = 1.8 V/3.3 V
  - VCC = 3.3 V

- Error free memory access
  - Internal error correction code (ECC) to protect data communication
  - Internal enhanced data management algorithm
  - Solid protection of sudden power failure safe-update operations for data content
- Security
  - Support secure bad block erase commands
  - Enhanced write Protection with permanent and partial protection options
- Quality
  - RoHS compliant (for detailed RoHS declaration, please contact your KSI representative.)

Device Summary:

Table 1 – Device Summary

Product Part number	NAND Density	Package	Operating voltage
KE4CN2H5A	4GB	FBGA153	VCC=3.3V, VCCQ=1.8V/3.3V
KE4CN3H5A	8GB	FBGA153	
KE4CN4A5A	16GB	FBGA153	

1. Product Description

Kingston e•MMC™ products follow the JEDEC e•MMC™ 4.5 standard. It is an ideal universal storage solutions for many electronic devices, including smartphones, tablet PCs, PDAs, eBook readers, digital cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes. E•MMC™ encloses the MLC NAND and e•MMC™ controller inside as one JEDEC standard package, providing a standard interface to the host. The e•MMC™ controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

1.1. *e*•MMC™ Standard Specification

The Kingston NAND Device is fully compatible with the JEDEC Standard Specification No.JESD84-B45.

This datasheet describes the key and specific features of the Kingston *e*•MMC™ Device. Any additional information required interfacing the Device to a host system and all the practical methods for device detection and access can be found in the proper sections of the JEDEC Standard Specification.

2. Product Specification

2.1. System Performance

Table 2 – *e*•MMC™ Device Performance

Products	Typical value	
	Read Sequential (MB/s)	Write Sequential (MB/s)
KE4CN2H5A	85	12
KE4CN3H5A	166	25
KE4CN4A5A	166	45

Note 1: Values given for an 8-bit bus width, running HS200 mode from KSI proprietary tool, VCC=3.3V, VCCQ=3.3V.

Note 2: For performance number under other test conditions, please contact your KSI representatives.

Note 3: Performance numbers might be subject to changes without notice.

2.2. Power Consumption

Table 3 – *e*•MMC™ Device Power Consumption

Products	Read(mA)	Write(mA)	Standby(mA)
	Typ	Typ	Typ
KE4CN2H5A	89	49	0.156
KE4CN3H5A	91	73	0.157
KE4CN4A5A	95	100	0.19

Note 1; Values given for an 8-bit bus width, a clock frequency of 52MHz DDR mode, VCC= 3.3V±5%, VCCQ=3.3V±5%
Note 2: Current numbers might be subject to changes without notice.

3. *e*•MMC™ Device and System

3.1. *e*•MMC™ System Overview

The *e*•MMC™ specification covers the behavior of the interface and the Device controller. As part of this specification the existence of a host controller and a memory storage array are implied but the operation of these pieces is not fully specified.

The Kingston NAND Device contains a single chip MMC controller and NAND flash memory module. The micro-controller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory.

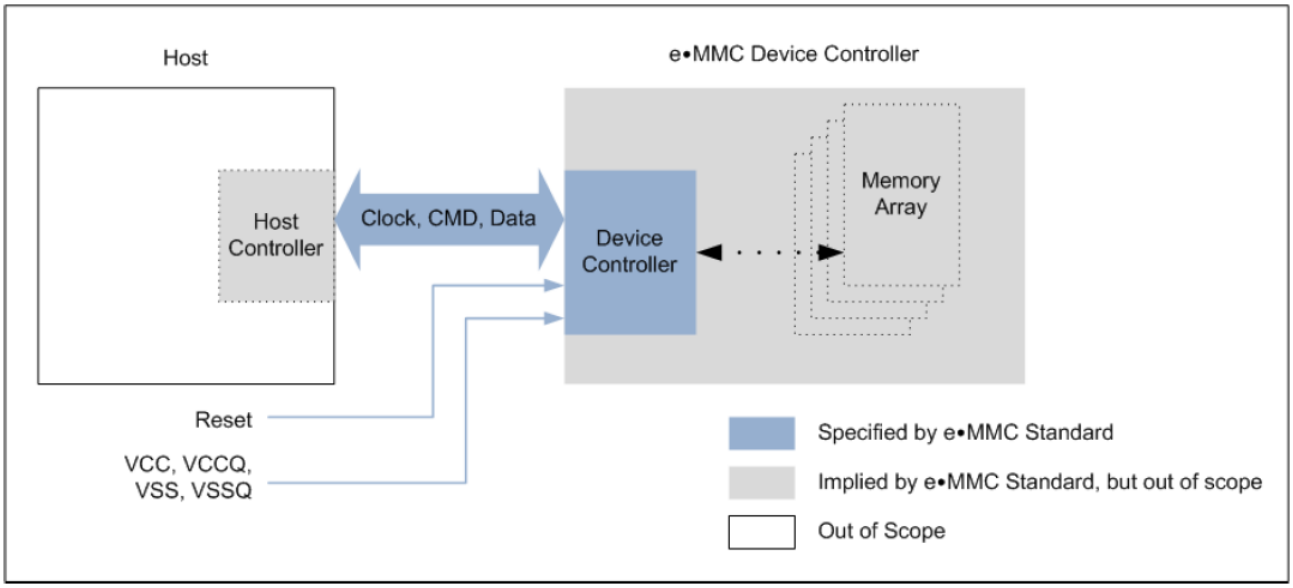

Figure 1 – *e*•MMC™ System Overview

3.2. Memory Addressing

Previous implementations of the *e*•MMC™ specification (versions up to v4.1) are following byte addressing with 32 bit field. This addressing mechanism permitted for *e*•MMC™ densities up to and including 2 GB.

To support larger densities the addressing mechanism was update to support sector addresses (512 B sectors). The sector addresses shall be used for all devices with capacity larger than 2 GB.

To determine the addressing mode use the host should read bit [30:29] in the OCR register.

3.3. *e*•MMC™ Device Overview

The *e*•MMC™ device transfers data via a configurable number of data bus signals. The communication signals are:

3.3.1 Clock (CLK)

Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.

3.3.2 Command (CMD)

This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the *e*•MMC™ host controller to the *e*•MMC™ Device and responses are sent from the Device to the host.

3.3.3 Input/Outputs (DAT0-DAT7)

These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the *e*•MMC™ host controller. The *e*•MMC™ Device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1–DAT7.

The signals on the *e*•MMC™ interface are described in Table 4.

Table 4 – *e*•MMC™ Interface

Name	Type[1]	Description
CLK	I	Clock
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data

DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware reset
VCC	S	Supply voltage for Core
VCCQ	S	Supply voltage for I/O
VSS	S	Supply voltage ground for Core
VSSQ	S	Supply voltage ground for I/O
Note1：**I**: input; **O**: output; **PP**: push-pull; **OD**: open-drain; **NC**: Not connected (or logical high); **S**: power supply.		

Each Device has a set of information registers (see also 0, Device Registers.)

Table 5 – *e*•MMC™ Registers

Name	Width (bytes)	Description	Implementation
CID	16	Device Identification number, an individual number for identification.	Mandatory
RCA	2	Relative Device Address, is the Device system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register, to configure the Device's output drivers.	Optional
CSD	16	Device Specific Data, information about the Device operation conditions.	Mandatory
OCR	4	Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the Device.	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0	Mandatory

The host may reset the device by:

- Switching the power supply off and back on. The device shall have its own power-on detection circuitry which puts the device into a defined state after the power-on Device.

- A reset signal
- By sending a special command

3.4. Bus Protocol

After a power-on reset, the host must initialize the device by a special message-based *e*•MMC™ bus protocol. For more details, refer to section 5.3.1 of the JEDEC Standard Specification No.JESD84-B45.

3.5. Bus Speed Modes

e•MMC™ defines several bus speed modes. **Table 6** summarizes the various modes.

Table 6— Bus Speed Modes

Mode Name	Data Rate	IO Voltage	Bus Width	Frequency	Max Data Transfer (implies x8 bus width)
Backwards Compatibility with legacy MMC card	Single	3.3/1.8V	1, 4, 8	0-26MHz	26MB/s
High Speed SDR	Single	3.3/1.8V	4, 8	0-52MHz	52MB/s
High Speed DDR	Dual	3.3/1.8V	4, 8	0-52MHz	104MB/s
HS200	Single	1.8V	4, 8	0-200MHz	200MB/s

3.5.1 HS200 Bus Speed Mode

The HS200 mode offers the following features:

- SDR Data sampling method
- CLK frequency up to 200MHz Data rate – up to 200MB/s
- or 8-bits bus width supported
- Single ended signaling with 4 selectable Drive Strength
- Signaling levels of 1.8V
- Tuning concept for Read Operations

4. Device Registers

Within the Device interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands (see Section 6.10 of JESD84-B45). The OCR, CID and CSD registers carry the Device/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters. The EXT_CSD register carries both, Device specific information and actual configuration parameters.

4.1. OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices. For detailed register setting value, please refer to appendix or KSI FAE.

4.2. CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (*e*•MMC™ protocol). For detailed register setting value, please refer to appendix or KSI FAE.

4.3. CSD Register

The Card-Specific Data (CSD) register provides information on how to access the Device contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. For detailed register setting value, please refer to appendix or KSI FAE.

4.4. Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For detailed register setting value, please refer to appendix or KSI FAE.

4.5. RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the *Stand-by State* with CMD7. For detailed register setting value, please refer to appendix or KSI FAE.

4.6. DSR Register

The 16-bit driver stage register (DSR) is described in detail in Section 7.6 of the JEDEC Standard Specification No.JESD84-B45. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage. For detailed register setting value, please refer to appendix or KSI FAE.

5. The *e*•MMC™ bus

The *e*•MMC™ bus has ten communication lines and three supply lines:

- **CMD**： Command is a bidirectional signal. The host and Device drivers are operating in two modes, open drain and push/pull.
- **DAT0-7**： Data lines are bidirectional signals. Host and Device drivers are operating in push-pull mode
- **CLK**： Clock is a host to Device signal. CLK operates in push-pull mode

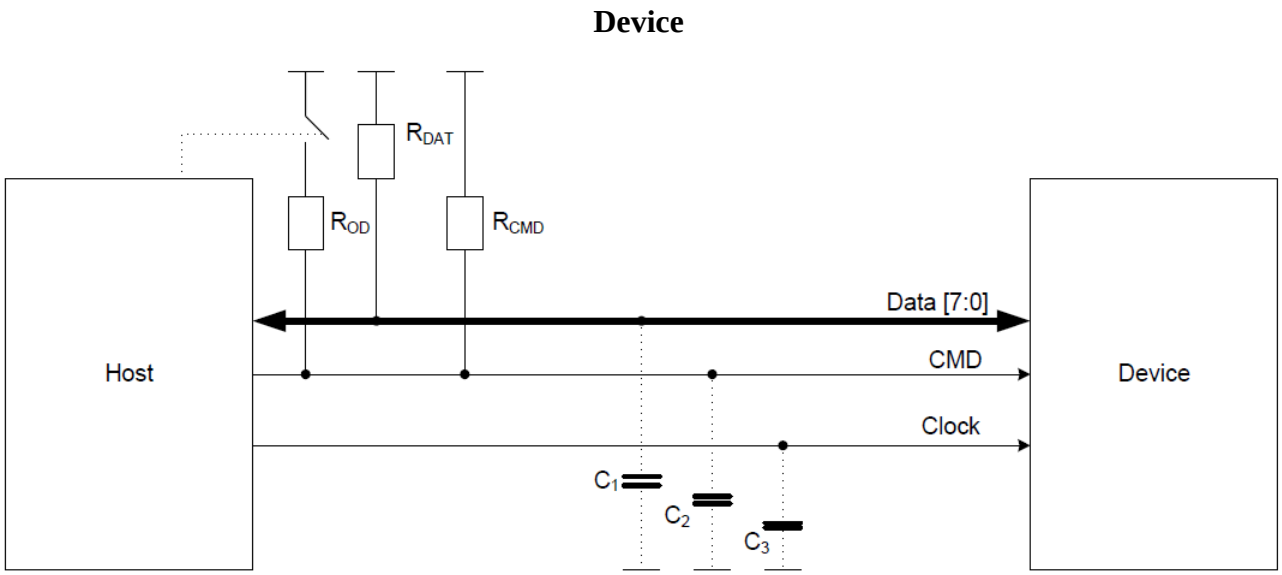

Figure 5 – Bus Circuitry Diagram

The R_{OD} is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the R_{OD}. R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT lines against bus floating device when all device drivers are in a high-impedance mode.

A constant current source can replace the R_{OD} by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable R_{OD} implementation, a fixed R_{CMD} can be used).

5.1. *e*•MMC™ Power Supply Voltage

The *e*•MMC™ supports one or more combinations of VCC and VCCQ as shown in Table 13. The VCCQ must be defined at equal to or less than VCC. The available voltage configuration is shown in Table 14.

Table 13 – *e*•MMC™ Power Supply Voltage

Parameter	Symbol	MIN	MAX	Unit	Remarks
Supply voltage (NAND)	VCC	2.7	3.6	V	
Supply voltage (I/O)	VCCQ	2.7	3.6	V	
		1.65	1.95	V	
Supply power-up for 3.3V	t_{PRUH}		35	ms	
Supply power-up for 1.8V	t_{PRUL}		25	ms	

The *e*•MMC™ must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations (see Table 14).

Table 14 – *e*•MMC™ Voltage Combinations

		VccQ	
		1.65V–1.95V	**2.7V–3.6V[1]**
Vcc	**2.7V-3.6V**	Valid	Valid
Note1：VccQ (I/O) 3.3 volt range is not supported in HS200 devices			

6. Temperature

Parameter	Rating	Unit	Note
Operating junction temperature	-25 ~ +85	℃	
Storage temperature	-40 ~ +85	℃	