A Microchip Technology Company

4 Mbit (x16) Multi-Purpose Flash Plus

SST39VF401C / SST39VF402C
SST39LF401C / SST39LF402C

Die / Wafer Sales Specifications

Features

- **Organized as 256K x16**
- **Single Voltage Read and Write Operations**
  - 2.7-3.6V for SST39VF401C/402C
  - 3.0-3.6V for SST39LF401C/402C
- **Superior Reliability**
  - Endurance: 100,000 Cycles (Typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption (typical values at 5 MHz)**
  - Active Current: 5 mA (typical)
  - Standby Current: 3 µA (typical)
  - Auto Low Power Mode: 3 µA (typical)
- **Hardware Block-Protection/WP# Input Pin**
  - Top Block-Protection (top 8 KWord)
  - Bottom Block-Protection (bottom 8 KWord)
- **Sector-Erase Capability**
  - Uniform 2 KWord sectors
- **Block-Erase Capability**
  - Flexible block architecture; one 8-, two 4-, one 16-, and seven 32-KWord blocks
- **Chip-Erase Capability**
- **Erase-Suspend/Erase-Resume Capabilities**
- **Hardware Reset Pin (RST#)**
- **Latched Address and Data**
- **Security-ID Feature**
  - SST: 128 bits; User: 128 words
- **Fast Read Access Time:**
  - 70 ns for SST39VF401C/402C
  - 55 ns for SST39LF401C/402C
- **Fast Erase and Word-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 40 ms (typical)
  - Word-Program Time: 7 µs (typical)
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Write Detection**
  - Toggle Bits
  - Data# Polling
  - Ready/Busy# Pin
- **CMOS I/O Compatibility**
- **JEDEC Standard**
  - Flash EEPROM Pinouts and command sets

Product Description

The SST39VF401C/402C and SST39LF401C/402C devices are 512K x16 CMOS Multi-Purpose Flash Plus (MPF+) manufactured with SST proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39VF401C/402C and SST39LF401C/402C write (Program or Erase) with a 2.7-3.6V power supply. These devices conform to JEDEC standard pinouts for x16 memories.

Featuring high performance Word-Program, the SST39VF401C/402C and SST39LF401C/402C devices provide a typical Word-Program time of 7 µsec. These devices use Toggle Bit, Data# Polling, or the RY/BY# pin to indicate the completion of Program operation. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

The SST39VF401C/402C and SST39LF401C/402C devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during Erase and Program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any

given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications.

This specification provides additional information about die/wafer sales. For device operating conditions, please refer to the SST39VF401C / SST39VF402C / SST39LF401C / SST39LF402C data sheet.

Pad Description and Coordinates

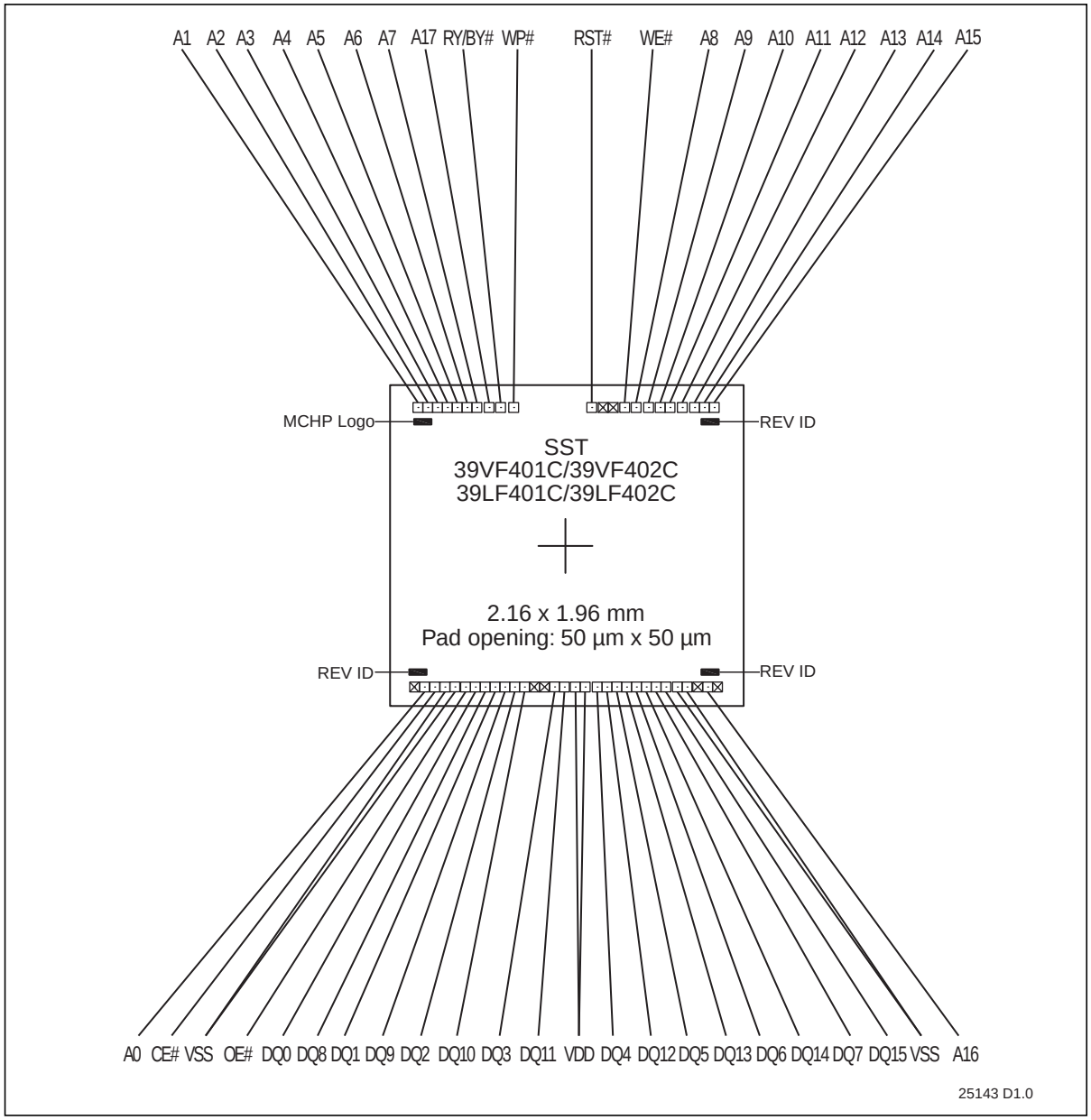

Figure 1: Pad Locations for SST39VF401C / SST39VF402C / SST39LF401C / SST39LF402C

Table 1: Pin Description

Symbol	Pin Name	Functions
A_{MS}[1]-A_0	Address Inputs	To provide memory addresses. During Sector-Erase A_{MS}-A_{11} address lines will select the sector. During Block-Erase A_{MS}-A_{15} address lines will select the block.
DQ_{15}-DQ_0	Data Input/output	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high.
WP#	Write Protect	To protect the top/bottom boot block from Erase/Program operation when grounded.
RST#	Reset	To reset and return the device to Read mode.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the Write operations.
V_{DD}	Power Supply	To provide power supply voltage: 2.7-3.6V
V_{SS}	Ground	
NC	No Connection	Unconnected pins.
RY/BY#	Ready/Busy#	To output the status of a Program or Erase operation RY/BY# is a open drain output, so a 10KΩ - 100KΩ pull-up resistor is required to allow RY/BY# to transition high indicating the device is ready to read.

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1. A_{MS} = Most significant address
   A_{MS} = A_{17}

Die Size: 2.16 mm x 2.37 mm (85.04 mil x 93.31 mils)
Pad Opening: 50 µm x 50 µm
Die Code: F100600-Ax
Product Revision: A

Table 2: Pad Coordinates (1 of 2)

Signal Name	X Coordinate	Y Coordinate
A15	905	850
A14	845	850
A13	785	850
A12	710	850
A11	635	850
A10	575	850
A9	504	850
A8	428	850
WE#	358	850
RST#	157	850
WP#	-320	850
RYBY#	-400	850
A17	-470	850
A7	-545	850
A6	-605	850
A5	-665	850
A4	-725	850
A3	-785	850
A2	-845	850
A1	-905	850
A0	-865	-857
CE#	-802	-857
VSS	-740	-857
	-679	-857
OE#	-614	-857
DQ0	-554	-857
DQ8	-494	-857
DQ1	-434	-857
DQ9	-374	-857
DQ2	-314	-857
DQ10	-254	-857
DQ3	-70	-857
DQ11	-10	-857
VDD	56	-857
	117	-857
DQ4	190	-857
DQ12	250	-857

Table 2: Pad Coordinates (Continued) (2 of 2)

Signal Name	X Coordinate	Y Coordinate
DQ5	310	-857
DQ13	370	-857
DQ6	430	-857
DQ14	490	-857
DQ7	550	-857
DQ15	610	-857
VSS	680	-857
	739	-857
A16	865	-857

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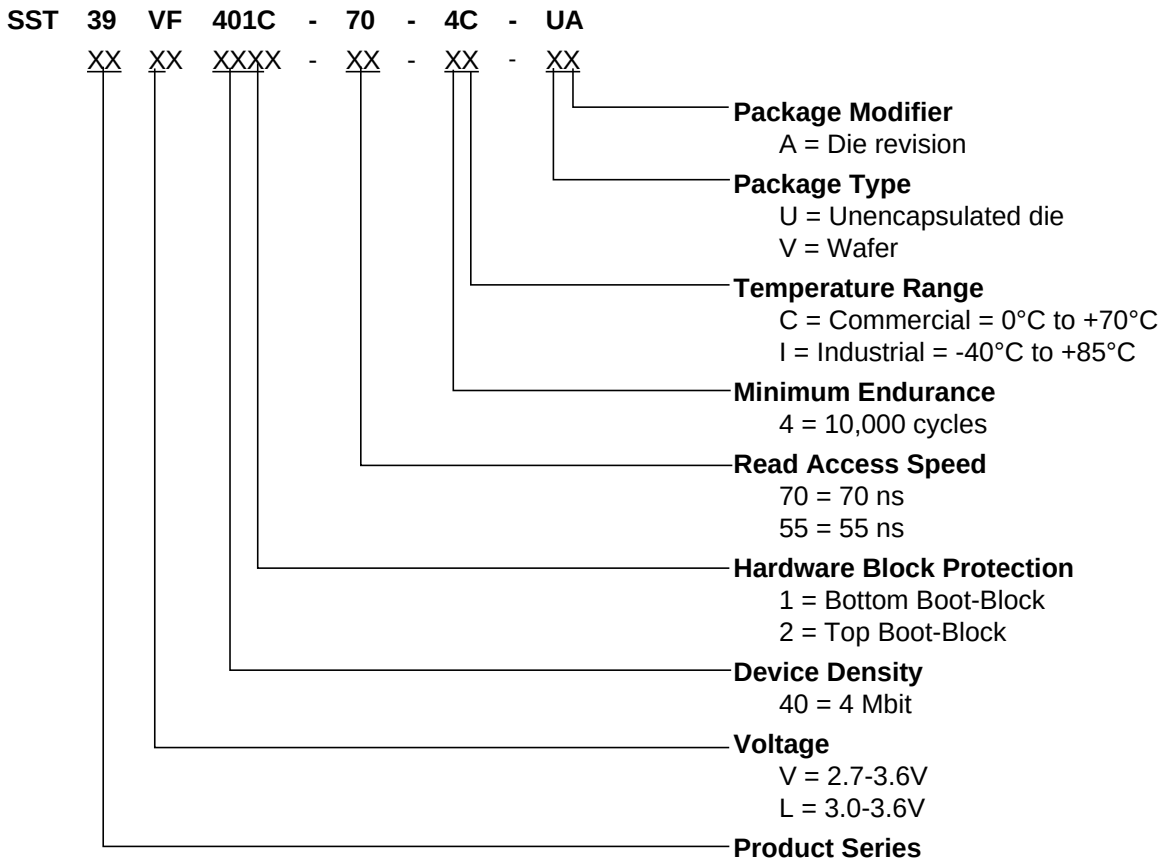
Product Ordering Information



Valid Combinations for SST39VF401C

SST39VF401C-70-4C-UA	SST39VF401C-70-4C-VA
SST39VF401C-70-4I-UA	SST39VF401C-70-4I-VA

Valid Combinations for SST39VF402C

SST39VF402C-70-4C-UA	SST39VF402C-70-4C-VA
SST39VF402C-70-4I-UA	SST39VF402C-70-4I-VA

Valid Combinations for SST39LF401C

SST39LF401C-55-4C-UA	SST39LF401C-55-4C-VA

Valid Combinations for SST39LF402C

SST39LF402C-55-4C-UA	SST39LF402C-55-4C-VA

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Table 3: Revision History

Number	Description	Date
A	• Initial release of specification	Aug 2012

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