

FEATURES

High relative accuracy (INL): ± 2 LSB maximum @ 16 bits
Tiny package: 3 mm \times 3 mm, 16-lead LFCSP
Total unadjusted error (TUE): $\pm 0.1\%$ of FSR maximum

Offset error: ± 1.5 mV maximum
Gain error: $\pm 0.1\%$ of FSR maximum
High drive capability: 20 mA, 0.5 V from supply rails
User selectable gain of 1 or 2 (GAIN pin)
Reset to zero scale or midscale (RSTSEL pin)
1.8 V logic compatibility
50 MHz SPI with readback or daisy chain
Low glitch: 0.5 nV-sec
Robust 4 kV HBM and 1.5 kV FICDM ESD rating
Low power: 1.8 mW at 3 V
2.7 V to 5.5 V power supply
 -40°C to $+105^{\circ}\text{C}$ temperature range

APPLICATIONS

Digital gain and offset adjustment
Programmable attenuators
Process control (PLC I/O cards)
Industrial automation
Data acquisition systems

GENERAL DESCRIPTION

The **AD5686/AD5684**, members of the *nanoDAC+*™ family, are low power, quad, 16-/12-bit buffered voltage output DACs. The devices include a gain select pin giving a full-scale output of 2.5 V (gain = 1) or 5 V (gain = 2). All devices operate from a single 2.7 V to 5.5 V supply, are guaranteed monotonic by design, and exhibit less than 0.1% FSR gain error and 1.5 mV offset error performance. The devices are available in a 3 mm \times 3 mm LFCSP and a TSSOP package.

The **AD5686/AD5684** also incorporate a power-on reset circuit and a RSTSEL pin that ensures that the DAC outputs power up to zero scale or midscale and remain at that level until a valid write takes place. Each part contains a per-channel power-down feature that reduces the current consumption of the device to 4 μA at 3 V while in power-down mode.

The **AD5686/AD5684** employ a versatile SPI interface that operates at clock rates up to 50 MHz, and all devices contain a V_{LOGIC} pin intended for 1.8 V/3 V/5 V logic.

FUNCTIONAL BLOCK DIAGRAM

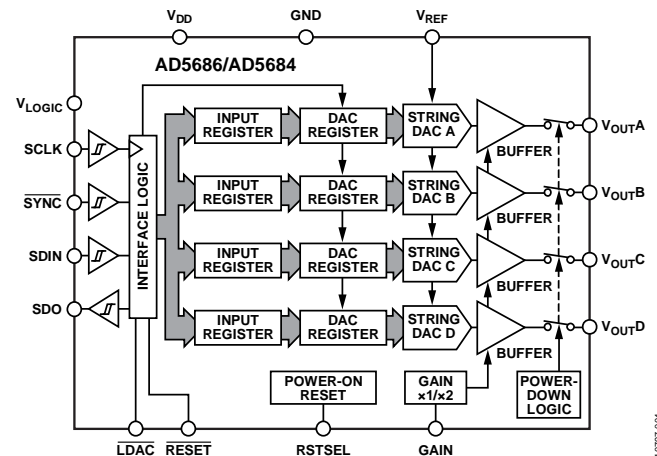


Figure 1.

 Table 1. Quad *nanoDAC+* Devices

| Interface | Reference | 16-Bit | 14-Bit | 12-Bit |
|------------------|-----------|-------------------------|-------------------------|-------------------------|
| SPI | Internal | AD5686R | AD5685R | AD5684R |
| SPI | External | AD5686 | | AD5684 |
| I ² C | Internal | AD5696R | AD5695R | AD5694R |
| I ² C | External | AD5696 | | AD5694 |

PRODUCT HIGHLIGHTS

- High Relative Accuracy (INL).
AD5686 (16-bit): ± 2 LSB maximum
AD5684 (12-bit): ± 1 LSB maximum
- Excellent DC Performance.
 Total unadjusted error: $\pm 0.1\%$ of FSR maximum
 Offset error: ± 1.5 mV maximum
 Gain error: $\pm 0.1\%$ of FSR maximum
- Two Package Options.
 3 mm \times 3 mm, 16-lead LFCSP
 16-lead TSSOP

Rev. 0

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REVISION HISTORY

7/12—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$; $V_{REF} = 2.5\text{ V}$; $1.8\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted. $R_L = 2\text{ k}\Omega$; $C_L = 200\text{ pF}$.

Table 2.

| Parameter | A Grade ¹ | | | B Grade ¹ | | | Unit | Test Conditions/Comments |
|--|----------------------|------------|--------------------|----------------------|------------|--------------------|------------------------------|---|
| | Min | Typ | Max | Min | Typ | Max | | |
| STATIC PERFORMANCE ² | | | | | | | | |
| AD5686 | | | | | | | | |
| Resolution | 16 | | | 16 | | | Bits | |
| Relative Accuracy | | ± 2 | ± 8 | | ± 1 | ± 2 | LSB | Gain = 2 |
| | | ± 2 | ± 8 | | ± 1 | ± 3 | LSB | Gain = 1 |
| Differential Nonlinearity | | | ± 1 | | | ± 1 | LSB | Guaranteed monotonic by design |
| AD5684 | | | | | | | | |
| Resolution | 12 | | | 12 | | | Bits | |
| Relative Accuracy | | ± 0.12 | ± 2 | | ± 0.12 | ± 1 | LSB | |
| Differential Nonlinearity | | | ± 1 | | | ± 1 | LSB | Guaranteed monotonic by design |
| Zero-Code Error | | 0.4 | 4 | | 0.4 | 1.5 | mV | All 0s loaded to DAC register |
| Offset Error | | +0.1 | ± 4 | | +0.1 | ± 1.5 | mV | |
| Full-Scale Error | | +0.01 | ± 0.2 | | +0.01 | ± 0.1 | % of FSR | All 1s loaded to DAC register |
| Gain Error | | ± 0.02 | ± 0.2 | | ± 0.02 | ± 0.1 | % of FSR | |
| Total Unadjusted Error | | ± 0.01 | ± 0.25 | | ± 0.01 | ± 0.1 | % of FSR | Gain = 2 |
| | | | ± 0.25 | | | ± 0.2 | % of FSR | Gain = 1 |
| Offset Error Drift ³ | | ± 1 | | | ± 1 | | $\mu\text{V}/^\circ\text{C}$ | |
| Gain Temperature Coefficient ³ | | ± 1 | | | ± 1 | | ppm | Of FSR/ $^\circ\text{C}$ |
| DC Power Supply Rejection Ratio ³ | | 0.15 | | | 0.15 | | mV/V | DAC code = midscale; $V_{DD} = 5\text{ V} \pm 10\%$ |
| DC Crosstalk ³ | | ± 2 | | | ± 2 | | μV | Due to single channel, full-scale output change |
| | | ± 3 | | | ± 3 | | $\mu\text{V}/\text{mA}$ | Due to load current change |
| | | ± 2 | | | ± 2 | | μV | Due to powering down (per channel) |
| OUTPUT CHARACTERISTICS ³ | | | | | | | | |
| Output Voltage Range | 0 | | V_{REF} | 0 | | V_{REF} | V | Gain = 1 |
| | 0 | | $2 \times V_{REF}$ | 0 | | $2 \times V_{REF}$ | V | Gain = 2, see Figure 23 |
| Capacitive Load Stability | | 2 | | | 2 | | nF | $R_L = \infty$ |
| | | 10 | | | 10 | | nF | $R_L = 1\text{ k}\Omega$ |
| Resistive Load ⁴ | 1 | | | 1 | | | k Ω | |
| Load Regulation | | 80 | | | 80 | | $\mu\text{V}/\text{mA}$ | $5\text{ V} \pm 10\%$, DAC code = midscale; $-30\text{ mA} \leq I_{OUT} \leq +30\text{ mA}$ |
| | | 80 | | | 80 | | $\mu\text{V}/\text{mA}$ | $3\text{ V} \pm 10\%$, DAC code = midscale; $-20\text{ mA} \leq I_{OUT} \leq +20\text{ mA}$ |
| Short-Circuit Current ⁵ | | 40 | | | 40 | | mA | |
| Load Impedance at Rails ⁶ | | 25 | | | 25 | | Ω | See Figure 23 |
| Power-Up Time | | 2.5 | | | 2.5 | | μs | Coming out of power-down mode; $V_{DD} = 5\text{ V}$ |
| REFERENCE INPUT | | | | | | | | |
| Reference Current | | 90 | | | 90 | | μA | $V_{REF} = V_{DD} = V_{LOGIC} = 5.5\text{ V}$, gain = 1 |
| | | 180 | | | 180 | | μA | $V_{REF} = V_{DD} = V_{LOGIC} = 5.5\text{ V}$, gain = 2 |
| Reference Input Range | 1 | | V_{DD} | 1 | | V_{DD} | V | Gain = 1 |
| | 1 | | $V_{DD}/2$ | 1 | | $V_{DD}/2$ | V | Gain = 2 |
| Reference Input Impedance | | 16 | | | 16 | | k Ω | Gain = 2 |
| | | 32 | | | 32 | | k Ω | Gain = 1 |

| Parameter | A Grade ¹ | | | B Grade ¹ | | | Unit | Test Conditions/Comments |
|-----------------------------------|------------------------|------|------------------------|------------------------|------|------------------------|------|---|
| | Min | Typ | Max | Min | Typ | Max | | |
| LOGIC INPUTS ³ | | | | | | | | |
| Input Current | | | ±2 | | | ±2 | μA | Per pin |
| Input Low Voltage (V_{INL}) | | | $0.3 \times V_{LOGIC}$ | | | $0.3 \times V_{LOGIC}$ | V | |
| Input High Voltage (V_{INH}) | $0.7 \times V_{LOGIC}$ | | | $0.7 \times V_{LOGIC}$ | | | V | |
| Pin Capacitance | | 2 | | | 2 | | pF | |
| LOGIC OUTPUTS (SDO) ³ | | | | | | | | |
| Output Low Voltage, V_{OL} | | | 0.4 | | | 0.4 | V | $I_{SINK} = 200 \mu A$ |
| Output High Voltage, V_{OH} | $V_{LOGIC} - 0.4$ | | | $V_{LOGIC} - 0.4$ | | | V | $I_{SOURCE} = 200 \mu A$ |
| Floating State Output Capacitance | | 4 | | | 4 | | pF | |
| POWER REQUIREMENTS | | | | | | | | |
| V_{LOGIC} | 1.8 | | 5.5 | 1.8 | | 5.5 | V | |
| I_{LOGIC} | | | 3 | | | 3 | μA | |
| V_{DD} | 2.7 | | 5.5 | 2.7 | | 5.5 | V | Gain = 1 |
| | $V_{REF} + 1.5$ | | 5.5 | $V_{REF} + 1.5$ | | 5.5 | V | Gain = 2 |
| I_{DD} | | | | | | | | $V_{IH} = V_{DD}, V_{IL} = GND, V_{DD} = 2.7 V \text{ to } 5.5 V$ |
| Normal Mode ⁷ | | 0.59 | 0.7 | | 0.59 | 0.7 | mA | |
| All Power-Down Modes ⁸ | | 1 | 4 | | 1 | 4 | μA | −40°C to +85°C |
| | | | 6 | | | 6 | μA | −40°C to +105°C |

¹ Temperature range, A and B grade: −40°C to +105°C.

² DC specifications tested with the outputs unloaded, unless otherwise noted. Upper dead band = 10 mV and exists only when $V_{REF} = V_{DD}$ with gain = 1 or when $V_{REF}/2 = V_{DD}$ with gain = 2. Linearity calculated using a reduced code range of 256 to 65,280 (AD5686) or 12 to 4080 (AD5684).

³ Guaranteed by design and characterization; not production tested.

⁴ Channel A and Channel B can have a combined output current of up to 30 mA. Similarly, Channel C and Channel D can have a combined output current of up to 30 mA up to a junction temperature of 110°C.

⁵ $V_{DD} = 5 V$. The device includes current limiting that is intended to protect the device during temporary overload conditions. Junction temperature can be exceeded during current limit. Operation above the specified maximum operation junction temperature may impair device reliability.

⁶ When drawing a load current at either rail, the output voltage headroom with respect to that rail is limited by the 25 Ω typical channel resistance of the output devices. For example, when sinking 1 mA, the minimum output voltage = $25 \Omega \times 1 \text{ mA} = 25 \text{ mV}$ (see Figure 23).

⁷ Interface inactive. All DACs active. DAC outputs unloaded.

⁸ All DACs powered down.

AC CHARACTERISTICS

$V_{DD} = 2.7\text{ V to }5.5\text{ V}$; $V_{REF} = 2.5\text{ V}$; $1.8\text{ V} \leq V_{LOGIC} \leq 5.5\text{ V}$; $R_L = 2\text{ k}\Omega$ to GND; $C_L = 200\text{ pF}$ to GND; all specifications T_{MIN} to T_{MAX} , unless otherwise noted.¹

Table 3.

| Parameter ² | Min | Typ | Max | Unit | Test Conditions/Comments ³ |
|--|-----|------|-----|------------------------------|--|
| Output Voltage Settling Time | | | | | |
| AD5686 | | 5 | 8 | μs | ¼ to ¾ scale settling to $\pm 2\text{ LSB}$ |
| AD5684 | | 5 | 7 | μs | ¼ to ¾ scale settling to $\pm 2\text{ LSB}$ |
| Slew Rate | | 0.8 | | $\text{V}/\mu\text{s}$ | |
| Digital-to-Analog Glitch Impulse | | 0.5 | | $\text{nV}\cdot\text{sec}$ | 1 LSB change around major carry |
| Digital Feedthrough | | 0.13 | | $\text{nV}\cdot\text{sec}$ | |
| Multiplying Bandwidth | | 500 | | kHz | |
| Digital Crosstalk | | 0.1 | | $\text{nV}\cdot\text{sec}$ | |
| Analog Crosstalk | | 0.2 | | $\text{nV}\cdot\text{sec}$ | |
| DAC-to-DAC Crosstalk | | 0.3 | | $\text{nV}\cdot\text{sec}$ | |
| Total Harmonic Distortion ⁴ | | -80 | | dB | At ambient, $\text{BW} = 20\text{ kHz}$, $V_{DD} = 5\text{ V}$, $f_{OUT} = 1\text{ kHz}$ |
| Output Noise Spectral Density | | 100 | | $\text{nV}/\sqrt{\text{Hz}}$ | DAC code = midscale, 10 kHz ; gain = 2 |
| Output Noise | | 6 | | $\mu\text{V p-p}$ | 0.1 Hz to 10 Hz |
| SNR | | 90 | | dB | At ambient, $\text{BW} = 20\text{ kHz}$, $V_{DD} = 5\text{ V}$, $f_{OUT} = 1\text{ kHz}$ |
| SFDR | | 83 | | dB | At ambient, $\text{BW} = 20\text{ kHz}$, $V_{DD} = 5\text{ V}$, $f_{OUT} = 1\text{ kHz}$ |
| SINAD | | 80 | | dB | At ambient, $\text{BW} = 20\text{ kHz}$, $V_{DD} = 5\text{ V}$, $f_{OUT} = 1\text{ kHz}$ |

¹ Guaranteed by design and characterization; not production tested.

² See the Terminology section.

³ Temperature range is -40°C to $+105^\circ\text{C}$, typical @ 25°C .

⁴ Digitally generated sine wave @ 1 kHz .

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1 \text{ ns/V}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 2. $V_{DD} = 2.7 \text{ V}$ to 5.5 V , $1.8 \text{ V} \leq V_{LOGIC} \leq 5.5 \text{ V}$; $V_{REF} = 2.5 \text{ V}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 4.

| Parameter ¹ | Symbol | 1.8 V ≤ V _{LOGIC} < 2.7 V | | 2.7 V ≤ V _{LOGIC} ≤ 5.5 V | | Unit |
|--|-----------------|------------------------------------|-----|------------------------------------|-----|------|
| | | Min | Max | Min | Max | |
| SCLK Cycle Time | t ₁ | 33 | | 20 | | ns |
| SCLK High Time | t ₂ | 16 | | 10 | | ns |
| SCLK Low Time | t ₃ | 16 | | 10 | | ns |
| SYNC to SCLK Falling Edge Setup Time | t ₄ | 15 | | 10 | | ns |
| Data Setup Time | t ₅ | 8 | | 5 | | ns |
| Data Hold Time | t ₆ | 8 | | 5 | | ns |
| SCLK Falling Edge to SYNC Rising Edge | t ₇ | 15 | | 10 | | ns |
| Minimum SYNC High Time | t ₈ | 20 | | 20 | | ns |
| SYNC Falling Edge to SCLK Fall Ignore | t ₉ | 16 | | 10 | | ns |
| LDAC Pulse Width Low | t ₁₀ | 25 | | 15 | | ns |
| SCLK Falling Edge to LDAC Rising Edge | t ₁₁ | 30 | | 20 | | ns |
| SCLK Falling Edge to LDAC Falling Edge | t ₁₂ | 20 | | 20 | | ns |
| RESET Minimum Pulse Width Low | t ₁₃ | 30 | | 30 | | ns |
| RESET Pulse Activation Time | t ₁₄ | 30 | | 30 | | ns |
| Power-Up Time ² | | 4.5 | | 4.5 | | μs |

¹ Maximum SCLK frequency is 50 MHz at $V_{DD} = 2.7 \text{ V}$ to 5.5 V , $1.8 \text{ V} \leq V_{LOGIC} \leq V_{DD}$. Guaranteed by design and characterization; not production tested.

² Time to exit power-down to normal mode of AD5686/AD5684 operation, 32nd clock edge to 90% of DAC midscale value, with output unloaded.

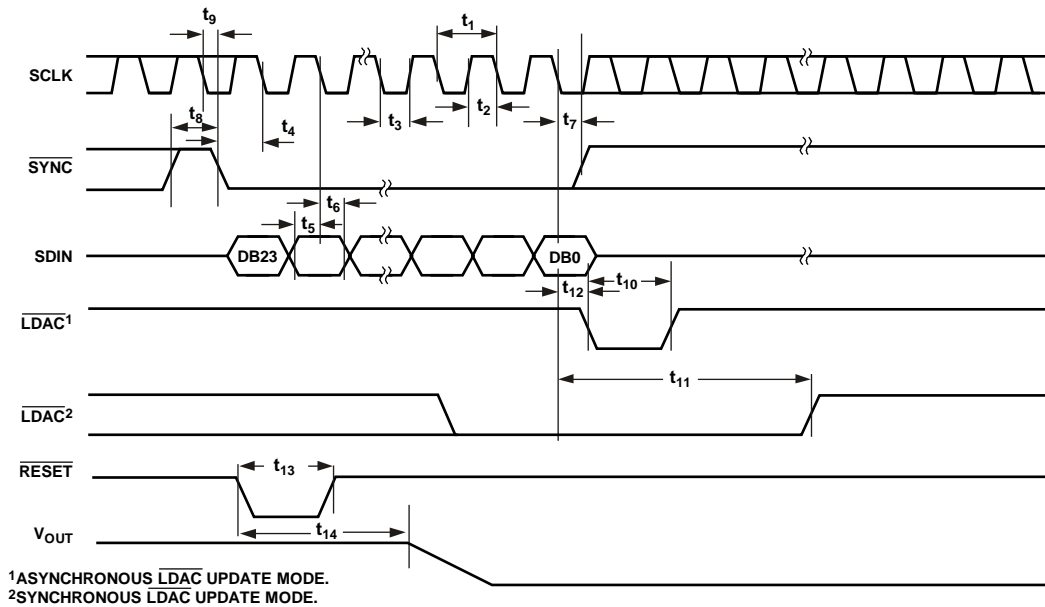


Figure 2. Serial Write Operation

10797-902

DAISY-CHAIN AND READBACK TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1 \text{ ns/V}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 4 and Figure 5. $V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$, $1.8 \text{ V} \leq V_{LOGIC} \leq 5.5 \text{ V}$; $V_{REF} = 2.5 \text{ V}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.

Table 5.

| Parameter ¹ | Symbol | 1.8 V ≤ V _{LOGIC} < 2.7 V | | 2.7 V ≤ V _{LOGIC} ≤ 5.5 V | | Unit |
|---------------------------------------|-----------------|------------------------------------|-----|------------------------------------|-----|------|
| | | Min | Max | Min | Max | |
| SCLK Cycle Time | t ₁ | 66 | | 40 | | ns |
| SCLK High Time | t ₂ | 33 | | 20 | | ns |
| SCLK Low Time | t ₃ | 33 | | 20 | | ns |
| SYNC to SCLK Falling Edge | t ₄ | 33 | | 20 | | ns |
| Data Setup Time | t ₅ | 5 | | 5 | | ns |
| Data Hold Time | t ₆ | 5 | | 5 | | ns |
| SCLK Falling Edge to SYNC Rising Edge | t ₇ | 15 | | 10 | | ns |
| Minimum SYNC High Time | t ₈ | 60 | | 30 | | ns |
| Minimum SYNC High Time | t ₉ | 60 | | 30 | | ns |
| SDO Data Valid from SCLK Rising Edge | t ₁₀ | | 36 | | 25 | ns |
| SCLK Falling Edge to SYNC Rising Edge | t ₁₁ | 15 | | 10 | | ns |
| SYNC Rising Edge to SCLK Rising Edge | t ₁₂ | 15 | | 10 | | ns |

¹ Maximum SCLK frequency is 25 MHz or 15 MHz at $V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$, $1.8 \text{ V} \leq V_{LOGIC} \leq V_{DD}$. Guaranteed by design and characterization; not production tested.

Circuit and Timing Diagrams

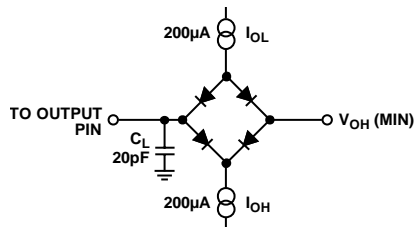


Figure 3. Load Circuit for Digital Output (SDO) Timing Specifications

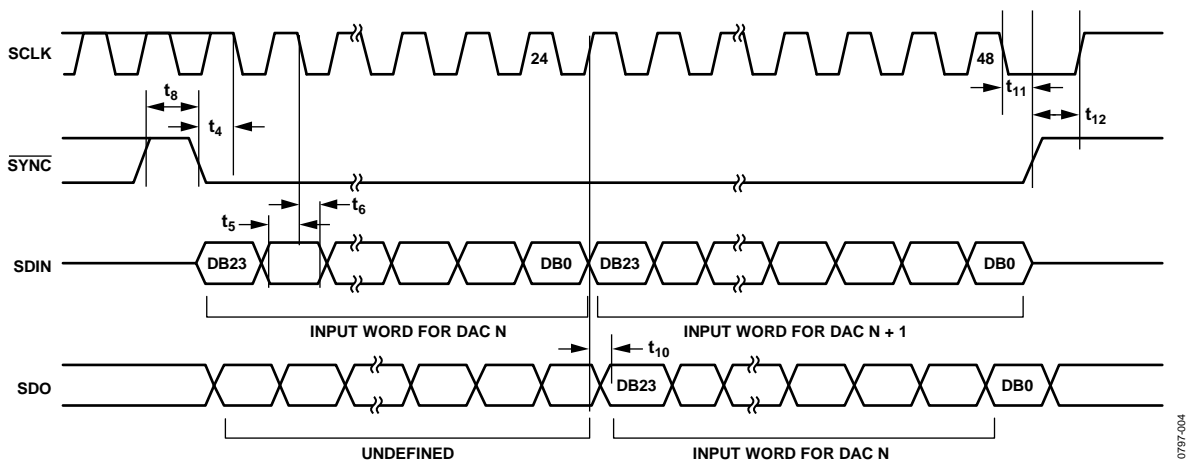


Figure 4. Daisy-Chain Timing Diagram

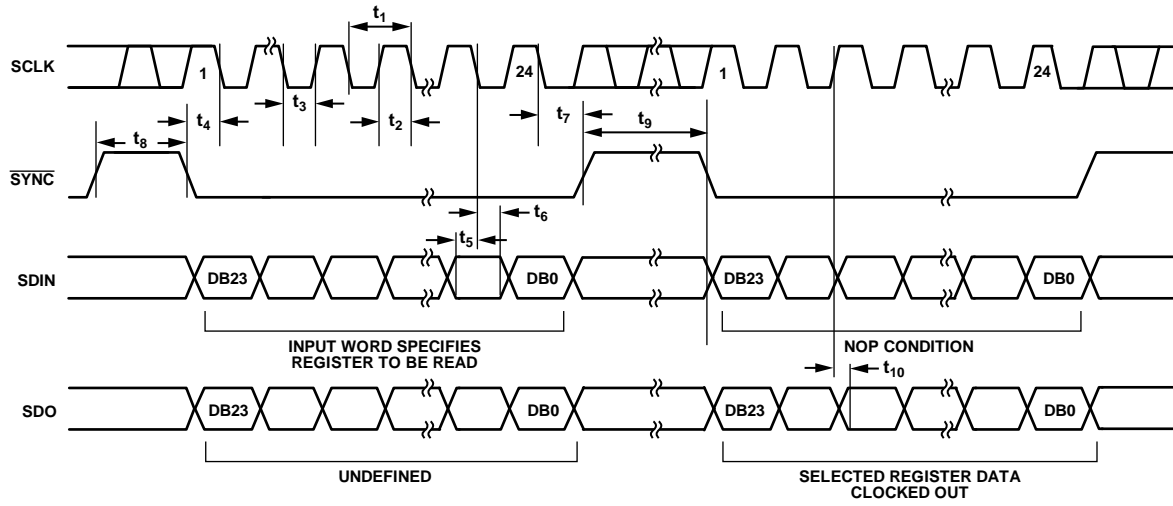


Figure 5. Readback Timing Diagram

10797-005

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 6.

| Parameter | Rating |
|---|-------------------------------|
| V_{DD} to GND | -0.3 V to +7 V |
| V_{LOGIC} to GND | -0.3 V to +7 V |
| V_{OUT} to GND | -0.3 V to $V_{DD} + 0.3$ V |
| V_{REF} to GND | -0.3 V to $V_{DD} + 0.3$ V |
| Digital Input Voltage to GND | -0.3 V to $V_{LOGIC} + 0.3$ V |
| Operating Temperature Range | -40°C to +105°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 125°C |
| 16-Lead TSSOP, θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board) | 112.6°C/W |
| 16-Lead LFCSP, θ_{JA} Thermal Impedance, 0 Airflow (4-Layer Board) | 70°C/W |
| Reflow Soldering Peak Temperature, Pb Free (J-STD-020) | 260°C |
| ESD | |
| HBM ¹ | 4 kV |
| FICDM | 1.5 kV |

¹ Human body model (HBM) classification.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

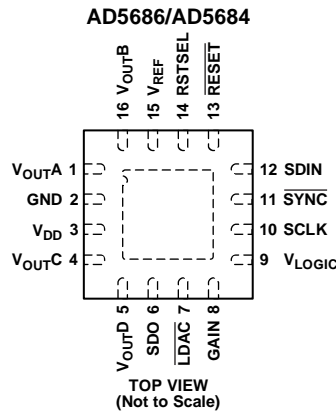
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES

1. THE EXPOSED PAD MUST BE TIED TO GND.

Figure 6. 16-Lead LFCSP Pin Configuration

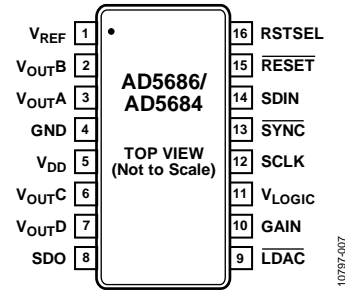


Figure 7. 16-Lead TSSOP Pin Configuration

Table 7. Pin Function Descriptions

| Pin No. | | Mnemonic | Description |
|---------|-------|---------------------------|--|
| LFCSP | TSSOP | | |
| 1 | 3 | V_{OUTA} | Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation. |
| 2 | 4 | GND | Ground Reference Point for All Circuitry on the Part. |
| 3 | 5 | V_{DD} | Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 μ F capacitor in parallel with a 0.1 μ F capacitor to GND. |
| 4 | 6 | V_{OUTC} | Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation. |
| 5 | 7 | V_{OUTD} | Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation. |
| 6 | 8 | SDO | Serial Data Output. Can be used to daisy-chain a number of AD5686/AD5684 devices together or can be used for readback. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock. |
| 7 | 9 | $\overline{\text{LDAC}}$ | $\overline{\text{LDAC}}$ can be operated in two modes, asynchronously and synchronously. Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to be simultaneously updated. This pin can also be tied permanently low. |
| 8 | 10 | GAIN | Span Set Pin. When this pin is tied to GND, all four DAC outputs have a span from 0 V to V_{REF} . When this pin is tied to V_{DD} , all four DAC outputs have a span from 0 V to $2 \times V_{REF}$. |
| 9 | 11 | V_{LOGIC} | Digital Power Supply. Voltage ranges from 1.8 V to 5.5 V. |
| 10 | 12 | SCLK | Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz. |
| 11 | 13 | $\overline{\text{SYNC}}$ | Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, data is transferred in on the falling edges of the next 24 clocks. |
| 12 | 14 | SDIN | Serial Data Input. These devices have a 24-bit input shift register. Data is clocked into the register on the falling edge of the serial clock input. |
| 13 | 15 | $\overline{\text{RESET}}$ | Asynchronous Reset Input. The $\overline{\text{RESET}}$ input is falling edge sensitive. When $\overline{\text{RESET}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{RESET}}$ is activated, the input register and the DAC register are updated with zero scale or midscale, depending on the state of the RSTSEL pin. |
| 14 | 16 | RSTSEL | Power-On Reset Pin. Tying this pin to GND powers up all four DACs to zero scale. Tying this pin to V_{DD} powers up all four DACs to midscale. |
| 15 | 1 | V_{REF} | Reference Input Voltage. |
| 16 | 2 | V_{OUTB} | Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation. |
| 17 | N/A | EPAD | Exposed Pad. The exposed pad must be tied to GND. |

TYPICAL PERFORMANCE CHARACTERISTICS

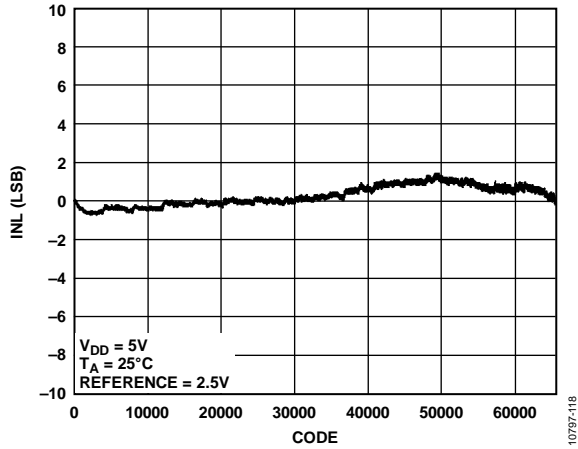


Figure 8. AD5686 INL

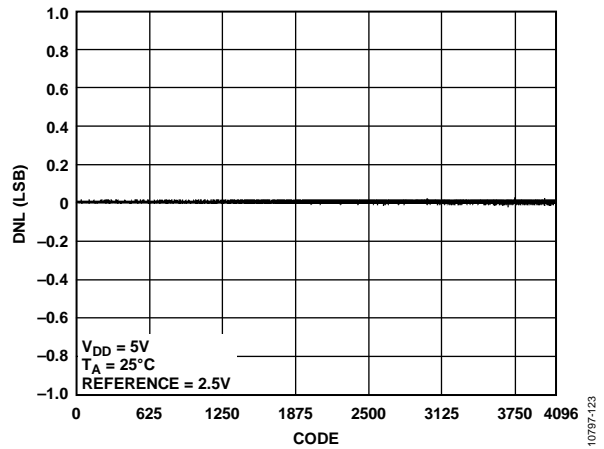


Figure 11. AD5684 DNL

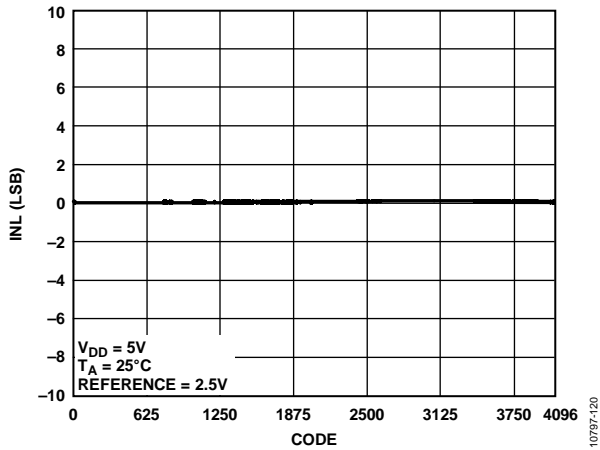


Figure 9. AD5684 INL

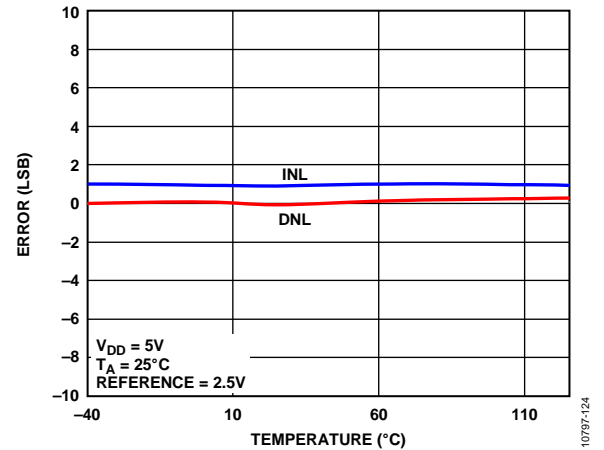


Figure 12. INL Error and DNL Error vs. Temperature

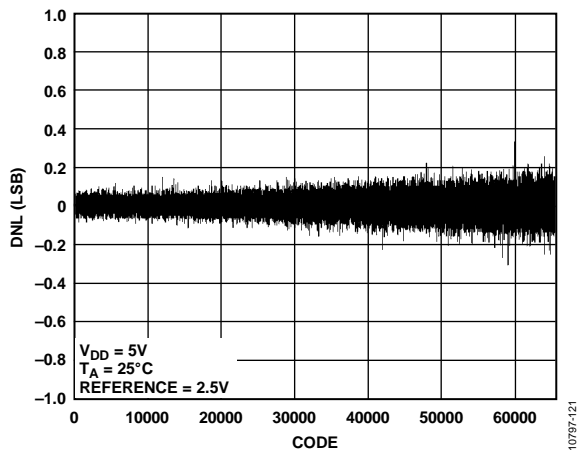


Figure 10. AD5686 DNL

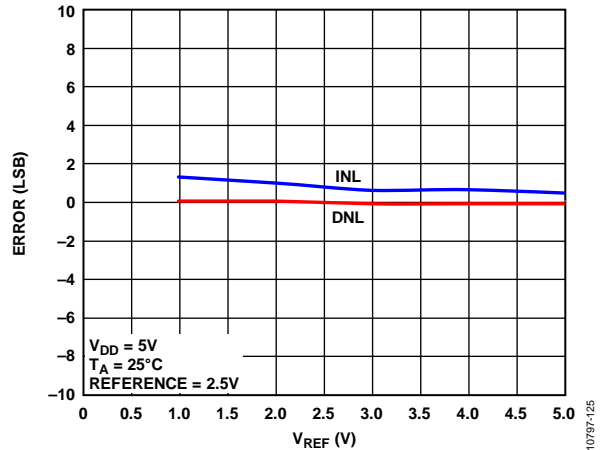


Figure 13. INL Error and DNL Error vs. V_{REF}

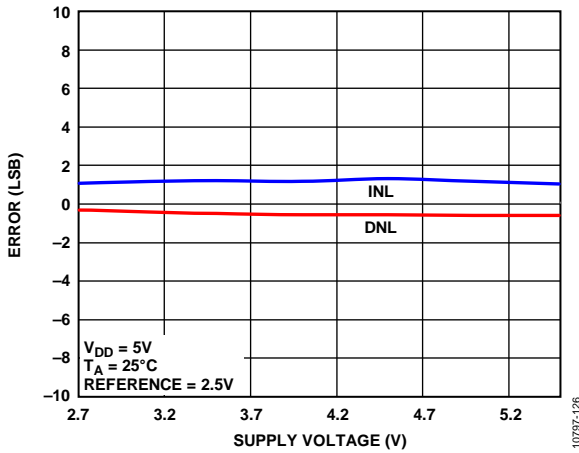


Figure 14. INL Error and DNL Error vs. Supply Voltage

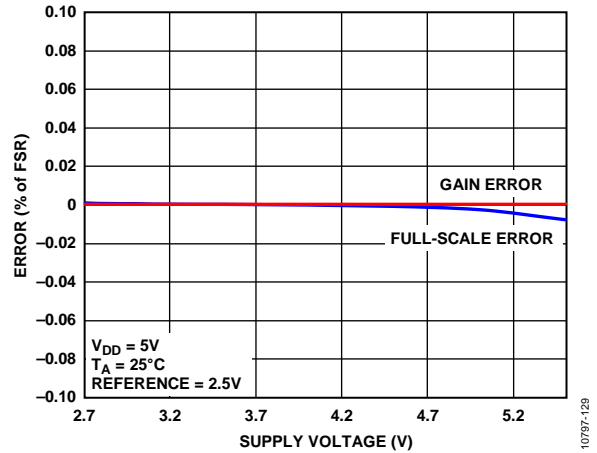


Figure 17. Gain Error and Full-Scale Error vs. Supply Voltage

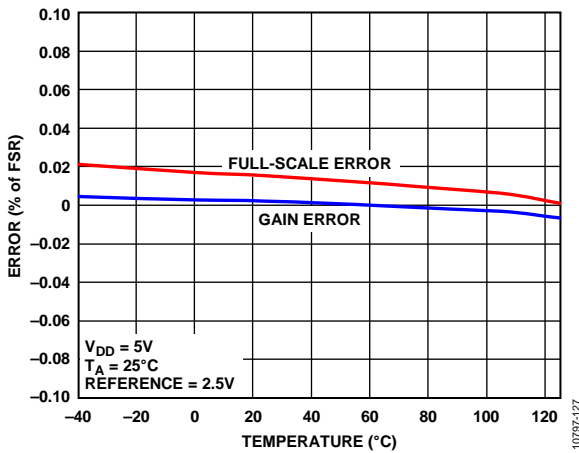


Figure 15. Gain Error and Full-Scale Error vs. Temperature

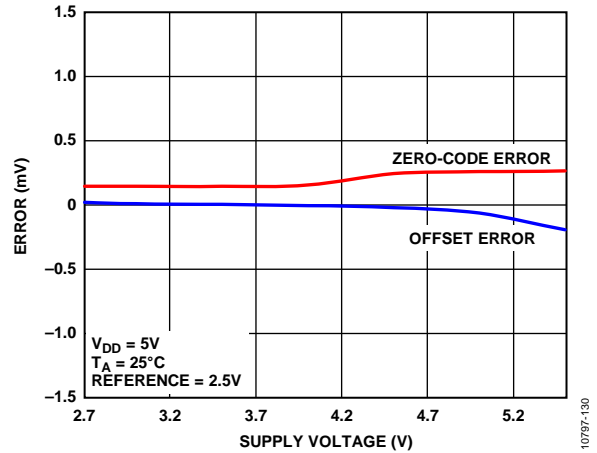


Figure 18. Zero-Code Error and Offset Error vs. Supply Voltage

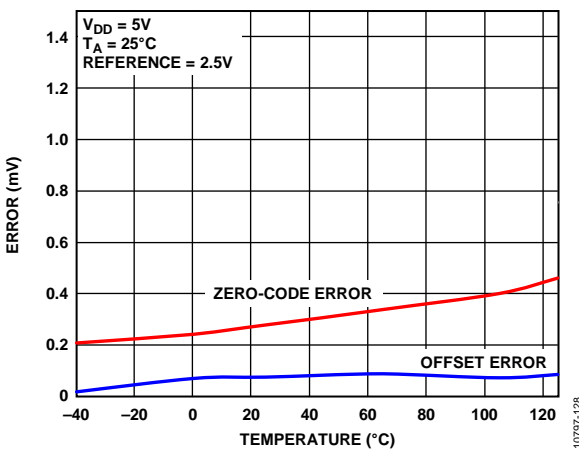


Figure 16. Zero-Code Error and Offset Error vs. Temperature

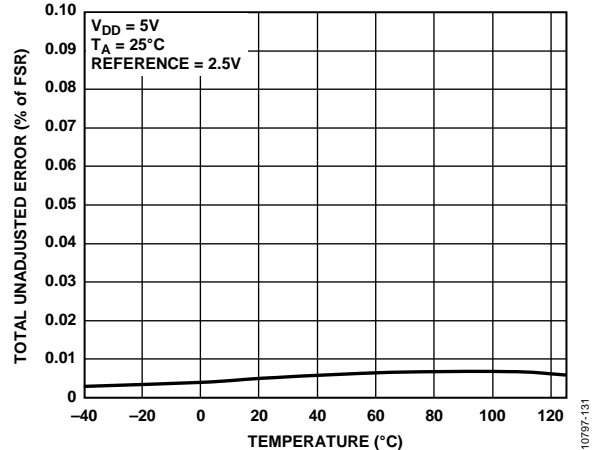


Figure 19. TUE vs. Temperature

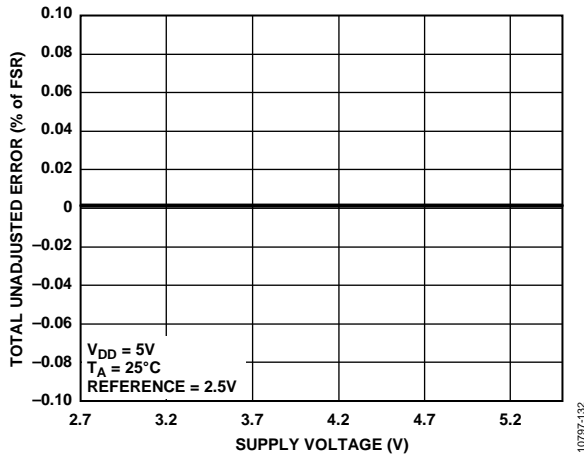


Figure 20. TUE vs. Supply Voltage, Gain = 1

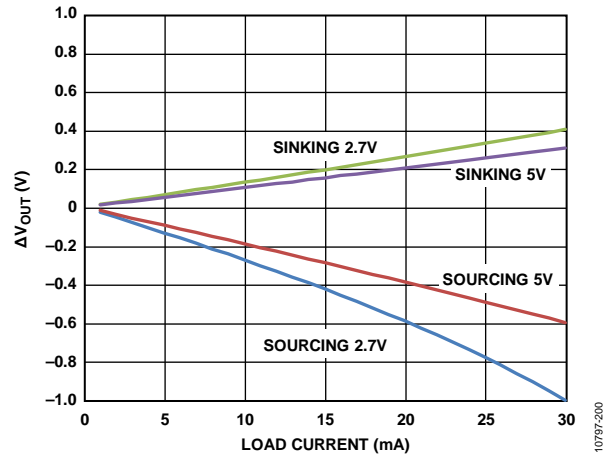


Figure 23. Headroom/Footroom vs. Load Current

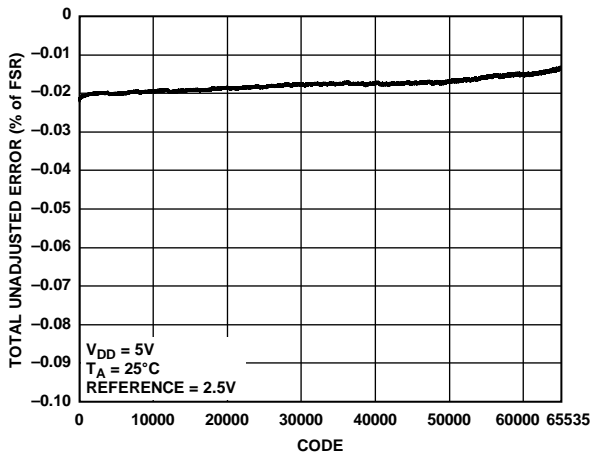


Figure 21. TUE vs. Code

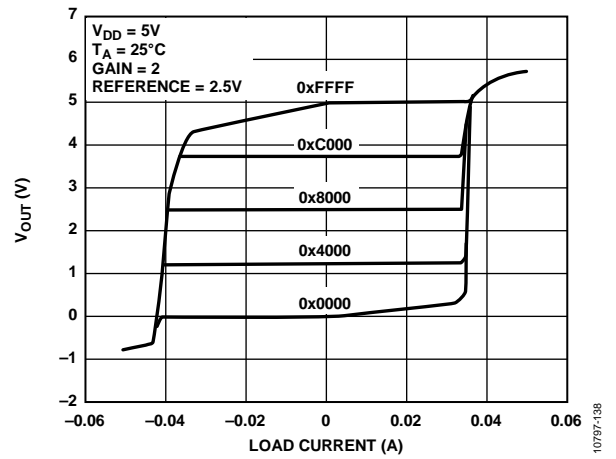


Figure 24. Source and Sink Capability at 5 V

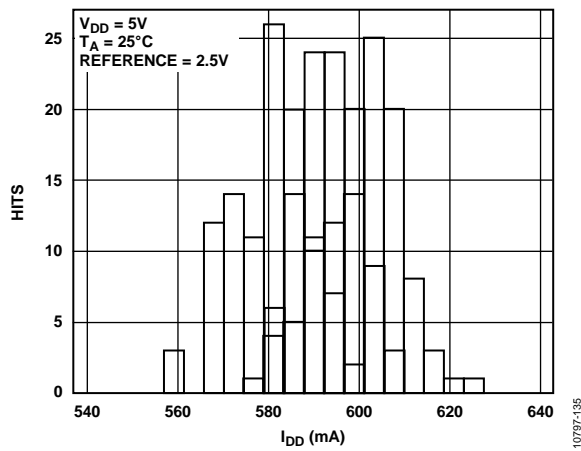


Figure 22. I_{DD} Histogram

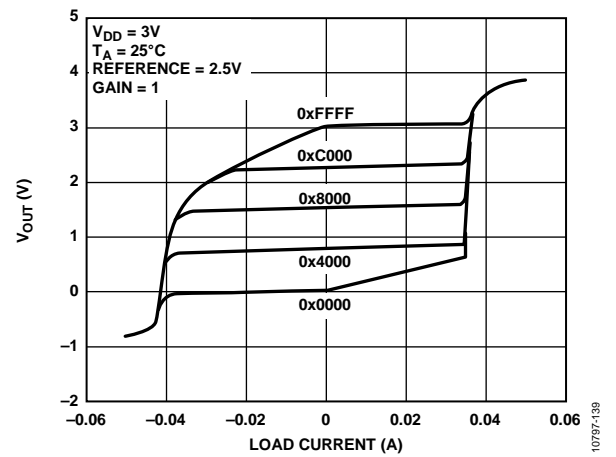


Figure 25. Source and Sink Capability at 3 V

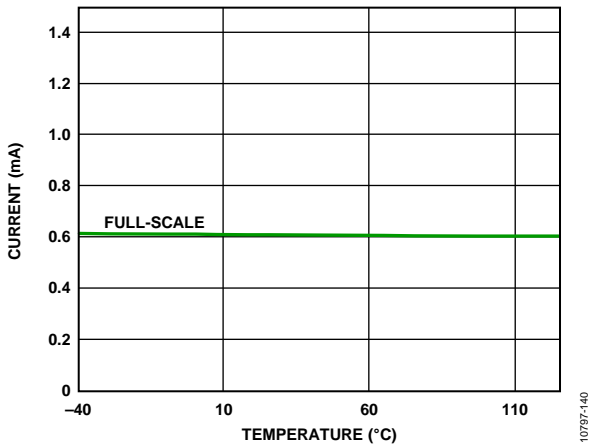


Figure 26. Supply Current vs. Temperature

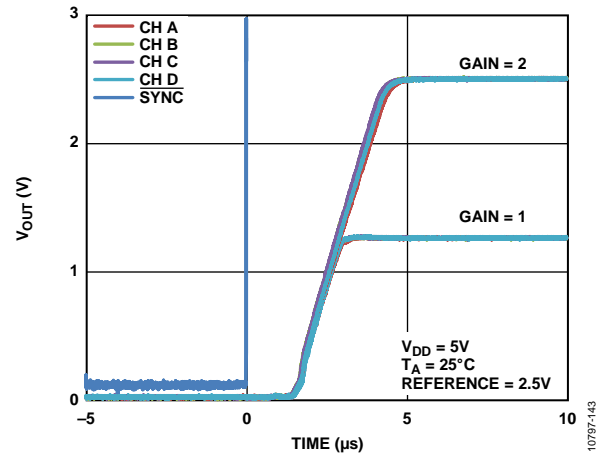


Figure 29. Exiting Power-Down to Midscale

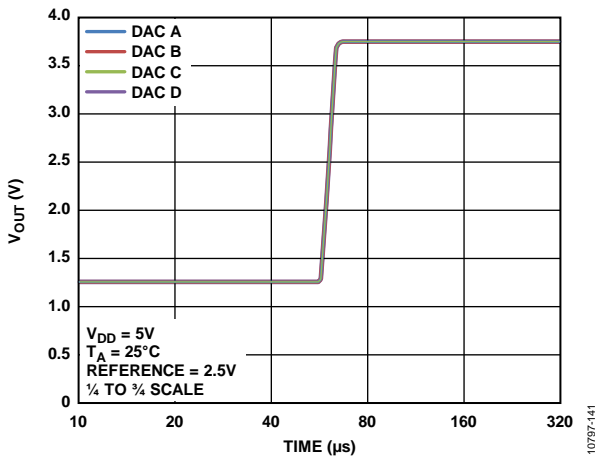


Figure 27. Settling Time, 5 V

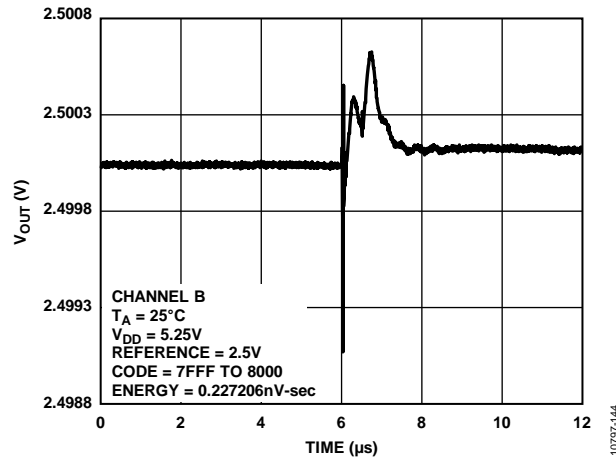


Figure 30. Digital-to-Analog Glitch Impulse

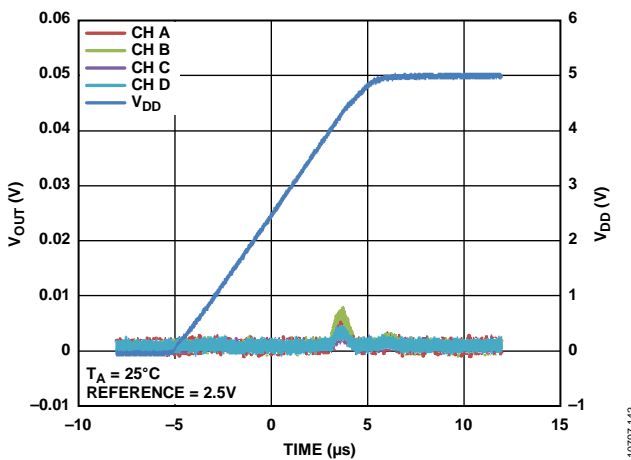


Figure 28. Power-On Reset to 0 V

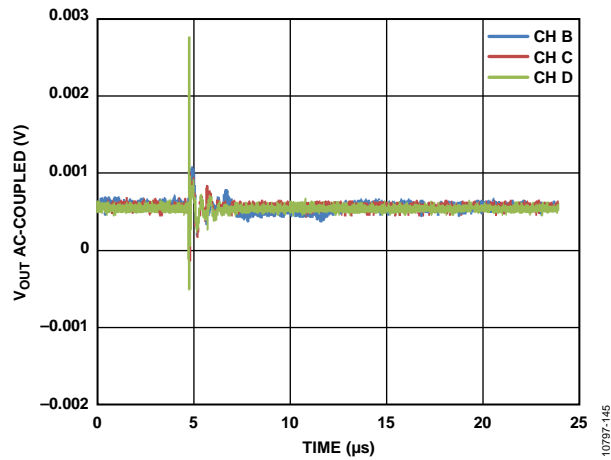


Figure 31. Analog Crosstalk, Channel A

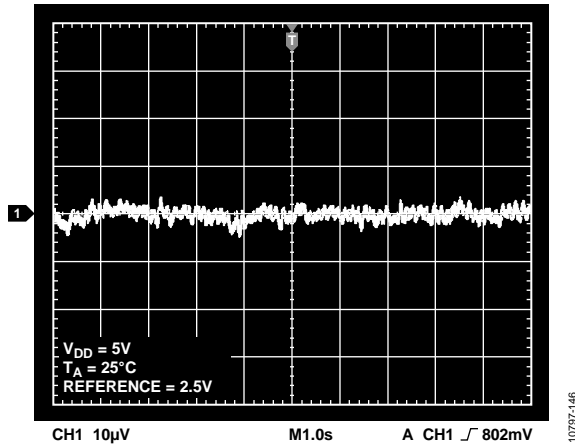


Figure 32. 0.1 Hz to 10 Hz Output Noise Plot

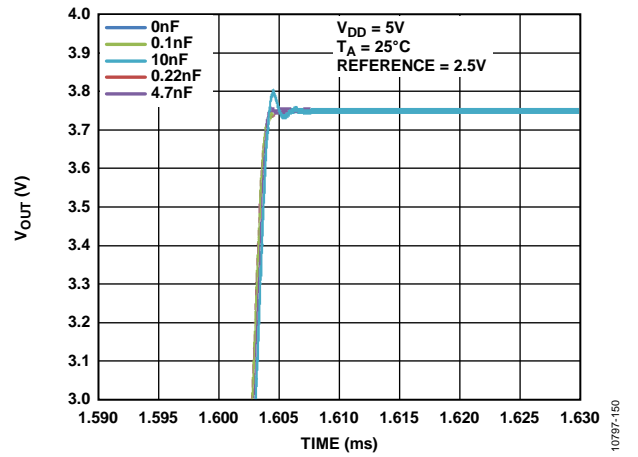


Figure 34. Settling Time vs. Capacitive Load

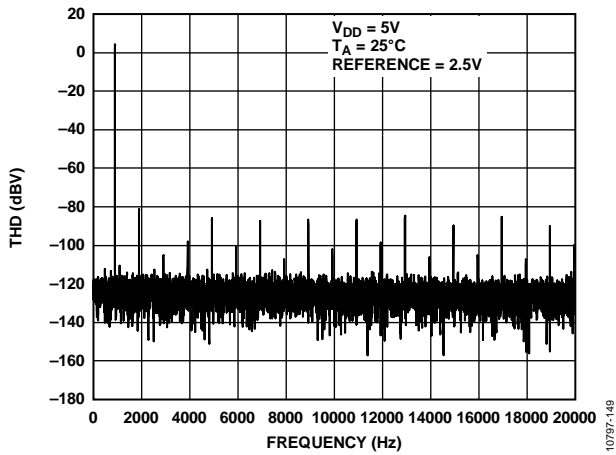


Figure 33. Total Harmonic Distortion @ 1 kHz

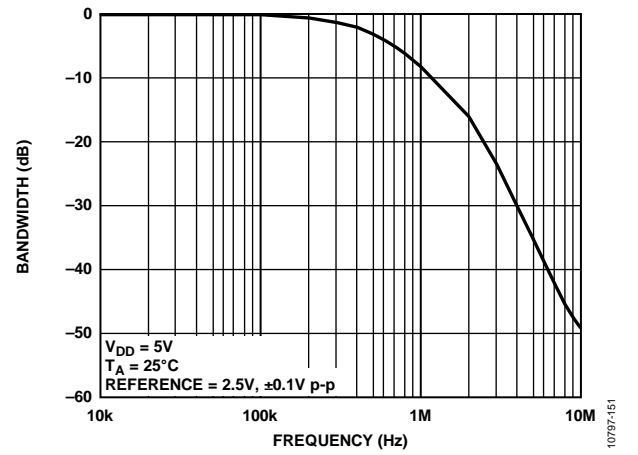


Figure 35. Multiplying Bandwidth, Reference = 2.5 V, ±0.1 V p-p, 10 kHz to 10 MHz

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)

For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 8.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB maximum ensures monotonicity. These DACs are guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 10.

Zero-Code Error

Zero-code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5686/AD5684 because the output of the DAC cannot go below 0 V due to a combination of the offset errors in the DAC and the output amplifier. Zero-code error is expressed in mV. A plot of zero-code error vs. temperature can be seen in Figure 16.

Full-Scale Error

Full-scale error is a measurement of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be $V_{DD} - 1$ LSB. Full-scale error is expressed in percent of full-scale range (% of FSR). A plot of full-scale error vs. temperature can be seen in Figure 15.

Gain Error

Gain error is a measurement of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal expressed as % of FSR.

Offset Error Drift

Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in $\mu\text{V}/^\circ\text{C}$.

Gain Temperature Coefficient

Gain temperature coefficient is a measurement of the change in gain error with changes in temperature. It is expressed in ppm of FSR/ $^\circ\text{C}$.

Offset Error

Offset error is a measurement of the difference between V_{OUT} (actual) and V_{OUT} (ideal) expressed in mV in the linear region of the transfer function. It can be negative or positive.

DC Power Supply Rejection Ratio (PSRR)

DC PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in mV/V. V_{REF} is held at 2.5 V, and V_{DD} is varied by $\pm 10\%$.

Output Voltage Settling Time

The output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a $\frac{1}{4}$ to $\frac{3}{4}$ full-scale input change and is measured from the rising edge of SYNC.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-sec, and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000) (see Figure 30).

Digital Feedthrough

Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-sec and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Noise Spectral Density

Noise spectral density is a measurement of the internally generated random noise. Random noise is characterized as a spectral density ($\text{nV}/\sqrt{\text{Hz}}$). It is measured by loading the DAC to midscale and measuring noise at the output. It is measured in $\text{nV}/\sqrt{\text{Hz}}$.

DC Crosstalk

DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in μV .

DC crosstalk due to load current change is a measurement of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in $\mu\text{V}/\text{mA}$.

Digital Crosstalk

Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-sec.

Analog Crosstalk

Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa). Then execute a software LDAC and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-sec.

DAC-to-DAC Crosstalk

DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC in response to a digital code change and subsequent analog output change of another DAC. It is measured by loading the attack channel with a full-scale code change (all 0s to all 1s and vice versa) using the write to and update commands while monitoring the output of another channel that is at midscale. The energy of the glitch is expressed in nV-sec.

Multiplying Bandwidth

The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output.

Total Harmonic Distortion (THD)

THD is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measurement of the harmonics present on the DAC output. It is measured in dB.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER

The AD5686/AD5684 are quad, 16-/12-bit, serial input, voltage output DACs. The parts operate from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5686/AD5684 in a 24-bit word format via a 3-wire serial interface. The AD5686/AD5684 incorporate a power-on reset circuit to ensure that the DAC output powers up to a known output state. The devices also have a software power-down mode that reduces the typical current consumption to typically 4 μ A.

TRANSFER FUNCTION

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REF} \times Gain \left[\frac{D}{2^N} \right]$$

where:

D is the decimal equivalent of the binary code that is loaded to the DAC register as follows:

- 0 to 4095 for the 12-bit device.
- 0 to 65,535 for the 16-bit device.

N is the DAC resolution.

V_{REF} is the value of the external reference.

$Gain$ is the gain of the output amplifier and is set to 1 by default. The gain can be set to $\times 1$ or $\times 2$ using the gain select pin. When this pin is tied to GND, all four DAC outputs have a span of 0 V to V_{REF} . When this pin is tied to V_{DD} , all four DAC outputs have a span of 0 V to $2 \times V_{REF}$.

DAC ARCHITECTURE

The DAC architecture consists of a string DAC followed by an output amplifier. Figure 36 shows a block diagram of the DAC architecture.

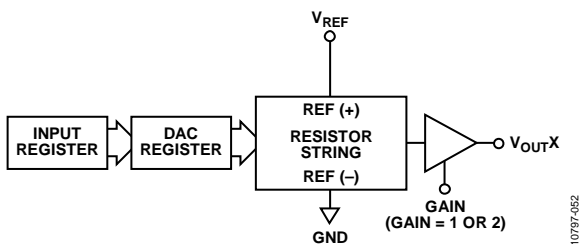


Figure 36. Single DAC Channel Architecture Block Diagram

The resistor string structure is shown in Figure 37. It is a string of resistors, each of Value R . The code loaded to the DAC register determines the node on the string where the voltage is to be tapped off and fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because the DAC is a string of resistors, it is guaranteed monotonic.

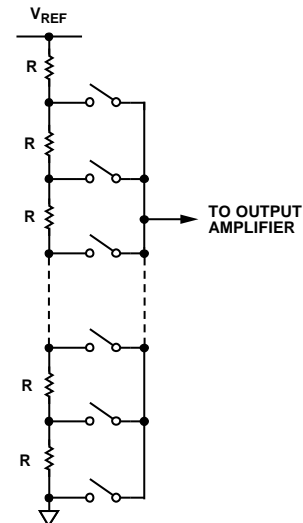


Figure 37. Resistor String Structure

Output Amplifiers

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD} . The actual range depends on the value of V_{REF} , the GAIN pin, offset error, and gain error. The GAIN pin selects the gain of the output.

- If this pin is tied to GND, all four outputs have a gain of 1, and the output range is 0 V to V_{REF} .
- If this pin is tied to V_{DD} , all four outputs have a gain of 2, and the output range is 0 V to $2 \times V_{REF}$.

These amplifiers are capable of driving a load of 1 k Ω in parallel with 2 nF to GND. The slew rate is 0.8 V/ μ s with a $\frac{1}{4}$ to $\frac{3}{4}$ scale settling time of 5 μ s.

SERIAL INTERFACE

The AD5686/AD5684 have a 3-wire serial interface (SYNC, SCLK, and SDIN) that is compatible with SPI, QSPI™, and MICROWIRE® interface standards as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence. The AD5686/AD5684 contain an SDO pin to allow the user to daisy-chain multiple devices together (see the Daisy-Chain Operation section) or for readback.

Input Shift Register

The input shift register of the AD5686/AD5684 is 24 bits wide. Data is loaded MSB first (DB23). The first four bits are the command bits, C3 to C0 (see Table 8), followed by the 4-bit DAC address bits, DAC A, DAC B, DAC C, and DAC D (see Table 9), and finally the bit data-word.

For the AD5686, the data-word comprises 16-bit input code (see Figure 38). For the AD5684, the data-word comprises 12-bit input code, followed by zero or four don't care bits (see Figure 39). These data bits are transferred to the input register on the 24 falling edges of SCLK and are updated on the rising edge of SYNC.

Commands can be executed on individual DAC channels, combined DAC channels, or on all DACs, depending on the address bits selected (see Table 9).

Table 8. Command Bit Definitions

| Command Bits | | | | Description |
|--------------|-----|-----|-----|---|
| C3 | C2 | C1 | C0 | |
| 0 | 0 | 0 | 0 | No operation |
| 0 | 0 | 0 | 1 | Write to Input Register n (dependent on LDAC) |
| 0 | 0 | 1 | 0 | Update DAC Register n with contents of Input Register n |
| 0 | 0 | 1 | 1 | Write to and update DAC Channel n |
| 0 | 1 | 0 | 0 | Power down/power up DAC |
| 0 | 1 | 0 | 1 | Hardware LDAC mask register |
| 0 | 1 | 1 | 0 | Software reset (power-on reset) |
| 0 | 1 | 1 | 1 | Reserved |
| 1 | 0 | 0 | 0 | Set up DCEN register (daisy-chain enable) |
| 1 | 0 | 0 | 1 | Set up readback register (readback enable) |
| 1 | 0 | 1 | 0 | Reserved |
| ... | ... | ... | ... | Reserved |
| 1 | 1 | 1 | 1 | Reserved |

Table 9. Address Bits and Selected DACs

| Address Bits | | | | Selected DAC Channel ¹ |
|--------------|-------|-------|-------|-----------------------------------|
| DAC D | DAC C | DAC B | DAC A | |
| 0 | 0 | 0 | 1 | DAC A |
| 0 | 0 | 1 | 0 | DAC B |
| 0 | 1 | 0 | 0 | DAC C |
| 1 | 0 | 0 | 0 | DAC D |
| 0 | 0 | 1 | 1 | DAC A and DAC B |
| 1 | 1 | 1 | 1 | All DACs |

¹ Any combination of DAC channels can be selected using the address bits.

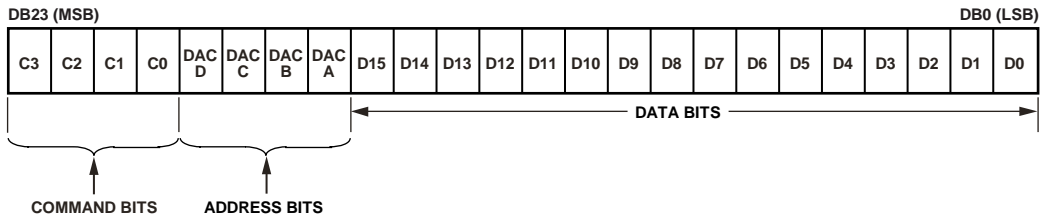


Figure 38. AD5686 Input Shift Register Contents

10797-054

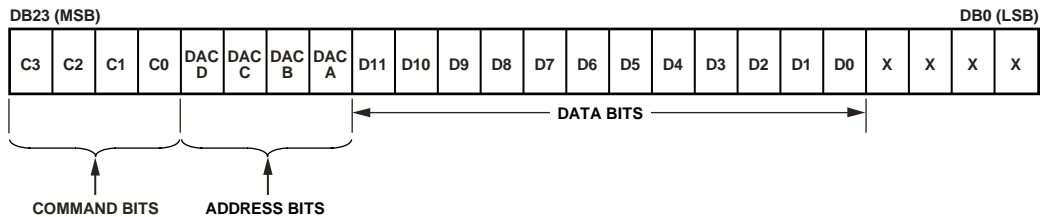


Figure 39. AD5684 Input Shift Register Contents

10797-056

STANDALONE OPERATION

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the SDIN line is clocked into the 24-bit input shift register on the falling edge of SCLK. After the last of 24 data bits is clocked in, $\overline{\text{SYNC}}$ should be brought high. The programmed function is then executed, that is, an LDAC-dependent change in DAC register contents and/or a change in the mode of operation. If $\overline{\text{SYNC}}$ is taken high at a clock before the 24th clock, it is considered a valid frame and invalid data may be loaded to the DAC. $\overline{\text{SYNC}}$ must be brought high for a minimum of 20 ns (single channel, see t_{S} in Figure 2) before the next write sequence so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence. $\overline{\text{SYNC}}$ should be idle at rails between write sequences for even lower power operation of the part. The $\overline{\text{SYNC}}$ line is kept low for 24 falling edges of SCLK, and the DAC is updated on the rising edge of $\overline{\text{SYNC}}$.

After data is transferred into the input register of the addressed DAC, all DAC registers and outputs can be updated by taking LDAC low while the $\overline{\text{SYNC}}$ line is high.

WRITE AND UPDATE COMMANDS

Write to Input Register *n* (Dependent on LDAC)

Command 0001 allows the user to write to each DAC's dedicated input register individually. When LDAC is low, the input register is transparent (if not controlled by the LDAC mask register).

Update DAC Register *n* with Contents of Input Register *n*

Command 0010 loads the DAC registers/outputs with the contents of the selected input registers and updates the DAC outputs directly.

Write to and Update DAC Channel *n* (Independent of LDAC)

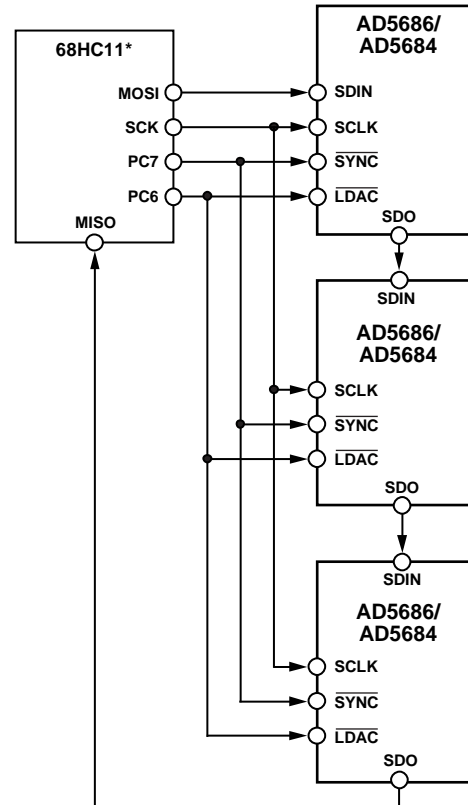
Command 0011 allows the user to write to the DAC registers and update the DAC outputs directly.

DAISY-CHAIN OPERATION

For systems that contain several DACs, the SDO pin can be used to daisy-chain several devices together. This function is enabled through a software executable daisy-chain enable (DCEN) command. Command 1000 is reserved for this DCEN function (see Table 8). The daisy-chain mode is enabled by setting Bit DB0 in the DCEN register. The default setting is standalone mode, where DB0 = 0. Table 10 shows how the state of the bit corresponds to the mode of operation of the device.

Table 10. Daisy-Chain Enable (DCEN) Register

| DB0 | Description |
|-----|---------------------------|
| 0 | Standalone mode (default) |
| 1 | DCEN mode |



*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 40. Daisy-Chaining the AD5686/AD5684

The SCLK pin is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the input shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO line to the SDIN input on the next DAC in the chain, a daisy-chain interface is constructed. Each DAC in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal $24 \times N$, where N is the total number of devices that are updated. If $\overline{\text{SYNC}}$ is taken high at a clock that is not a multiple of 24, it is considered a valid frame and invalid data may be loaded to the DAC. When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This latches the input data in each device in the daisy chain and prevents any further data from being clocked into the input shift register. The serial clock can be continuous or a gated clock. A continuous SCLK source can be used only if $\overline{\text{SYNC}}$ can be held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data.

READBACK OPERATION

Readback mode is invoked through a software executable readback command. If the SDO output is disabled via the daisy-chain mode disable bit in the control register, it is automatically enabled for the duration of the read operation, after which it is disabled again. Command 1001 is reserved for the readback function. This command, in association with selecting one of the address bits, DAC A to DAC D, selects the register to read. Note that only one DAC register can be selected during readback. The remaining three address bits must be set to Logic 0. The remaining data bits in the write sequence are don't care bits. If more than one or no bits are selected, DAC Channel A is read back by default. During the next SPI write, the data appearing on the SDO output contains the data from the previously addressed register.

For example, to read back the DAC register for Channel A, the following sequence should be implemented:

1. Write 0x900000 to the AD5686/AD5684 input register. This configures the part for read mode with the DAC register of Channel A selected. Note that all data bits, DB15 to DB0, are don't care bits.
2. Follow this with a second write, a NOP condition, 0x000000. During this write, the data from the register is clocked out on the SDO line. DB23 to DB20 contain undefined data, and the last 16 bits contain the DB19 to DB4 DAC register contents.

POWER-DOWN OPERATION

The AD5686/AD5684 provide three separate power-down modes (see Table 11). Command 0100 is designated for the power-down function (see Table 8). These power-down modes are software programmable by setting eight bits, Bit DB7 to Bit DB0, in the input shift register. Two bits are associated with each DAC channel. Table 11 shows how the state of the two bits corresponds to the mode of operation of the device.

Table 11. Modes of Operation

| Operating Mode | PDx1 | PDx0 |
|------------------|------|------|
| Normal Operation | 0 | 0 |
| Power-Down Modes | | |
| 1 kΩ to GND | 0 | 1 |
| 100 kΩ to GND | 1 | 0 |
| Three-State | 1 | 1 |

Any or all DACs (DAC A to DAC D) can be powered down to the selected mode by setting the corresponding bits. See Table 12 for the contents of the input shift register during the power-down/power-up operation.

When both Bit PDx1 and Bit PDx0 (where x is the channel selected) in the input shift register are set to 0, the parts work normally with their normal power consumption of 0.59 mA at 5 V. However, for the three power-down modes, the supply current falls to 4 μA at 5 V. Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different power-down options (see Table 11). The output is connected internally to GND through either a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 41.

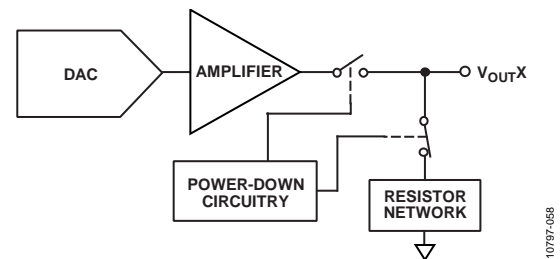


Figure 41. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the DAC registers are unaffected when in power-down. The DAC registers can be updated while the device is in power-down mode. The time required to exit power-down is typically 4.5 μs for V_{DD} = 5 V.

Table 12. 24-Bit Input Shift Register Contents for Power-Down/Power-Up Operation¹

| DB23 | DB22 | DB21 | DB20 | DB19 to DB16 | DB15 to DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 (LSB) |
|-------------------------|------|------|------|---------------------------|-------------|-------------------------|------|-------------------------|------|-------------------------|------|-------------------------|-----------|
| 0 | 1 | 0 | 0 | X | X | PDD1 | PDD0 | PDC1 | PDC0 | PDB1 | PDB0 | PDA1 | PDA0 |
| Command bits (C3 to C0) | | | | Address bits (don't care) | | Power-Down Select DAC D | | Power-Down Select DAC C | | Power-Down Select DAC B | | Power-Down Select DAC A | |

¹X = don't care.

LOAD DAC (HARDWARE $\overline{\text{LDAC}}$ PIN)

The AD5686/AD5684 DACs have double buffered interfaces consisting of two banks of registers: input registers and DAC registers. The user can write to any combination of the input registers. Updates to the DAC register are controlled by the $\overline{\text{LDAC}}$ pin.

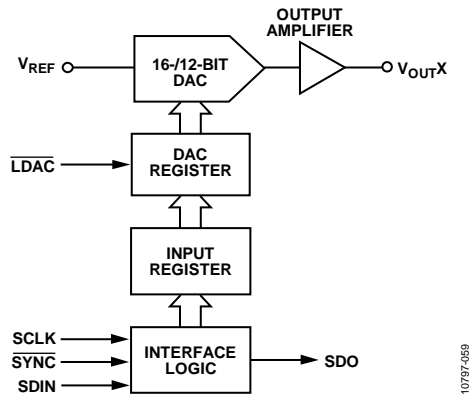


Figure 42. Simplified Diagram of Input Loading Circuitry for a Single DAC

Instantaneous DAC Updating ($\overline{\text{LDAC}}$ Held Low)

$\overline{\text{LDAC}}$ is held low while data is clocked into the input register using Command 0001. Both the addressed input register and the DAC register are updated on the rising edge of $\overline{\text{SYNC}}$ and the output begins to change (see Table 14).

Deferred DAC Updating ($\overline{\text{LDAC}}$ Is Pulsed Low)

$\overline{\text{LDAC}}$ is held high while data is clocked into the input register using Command 0001. All DAC outputs are asynchronously updated by taking $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ has been taken high. The update now occurs on the falling edge of $\overline{\text{LDAC}}$.

Table 14. Write Commands and $\overline{\text{LDAC}}$ Pin Truth Table¹

| Command | Description | Hardware $\overline{\text{LDAC}}$ Pin State | Input Register Contents | DAC Register Contents |
|---------|--|---|-------------------------|--------------------------------------|
| 0001 | Write to Input Register n (dependent on $\overline{\text{LDAC}}$) | V_{LOGIC} | Data update | No change (no update) |
| | | GND ² | Data update | Data update |
| 0010 | Update DAC Register n with contents of Input Register n | V_{LOGIC} | No change | Updated with input register contents |
| | | GND | No change | Updated with input register contents |
| 0011 | Write to and update DAC Channel n | V_{LOGIC} | Data update | Data update |
| | | GND | Data update | Data update |

¹ A high to low hardware $\overline{\text{LDAC}}$ pin transition always updates the contents of the DAC register with the contents of the input register on channels that are not masked (blocked) by the $\overline{\text{LDAC}}$ mask register.

² When $\overline{\text{LDAC}}$ is permanently tied low, the $\overline{\text{LDAC}}$ mask bits are ignored.

$\overline{\text{LDAC}}$ MASK REGISTER

Command 0101 is reserved for the software $\overline{\text{LDAC}}$ function. Address bits are ignored. Writing to the DAC using Command 0101 loads the 4-bit $\overline{\text{LDAC}}$ register (DB3 to DB0). The default for each channel is 0; that is, the $\overline{\text{LDAC}}$ pin works normally. Setting the bits to 1 forces this DAC channel to ignore transitions on the $\overline{\text{LDAC}}$ pin, regardless of the state of the hardware $\overline{\text{LDAC}}$ pin. This flexibility is useful in applications where the user wishes to select which channels respond to the $\overline{\text{LDAC}}$ pin.

The $\overline{\text{LDAC}}$ register gives the user extra flexibility and control over the hardware $\overline{\text{LDAC}}$ pin (see Table 13). Setting the $\overline{\text{LDAC}}$ bits (DB3 to DB0) to 0 for a DAC channel means that this channel's update is controlled by the hardware $\overline{\text{LDAC}}$ pin.

Table 13. $\overline{\text{LDAC}}$ Overwrite Definition

| Load $\overline{\text{LDAC}}$ Register | | $\overline{\text{LDAC}}$ Operation |
|--|------------------------------|---|
| $\overline{\text{LDAC}}$ Bits (DB3 to DB0) | $\overline{\text{LDAC}}$ Pin | |
| 0 | 1 or 0 | Determined by the $\overline{\text{LDAC}}$ pin. |
| 1 | X ¹ | DAC channels are updated and override the $\overline{\text{LDAC}}$ pin. DAC channels see $\overline{\text{LDAC}}$ as 1. |

¹ X = don't care.

HARDWARE RESET ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ is an active low reset that allows the outputs to be cleared to either zero scale or midscale. The clear code value is user selectable via the $\overline{\text{RESET}}$ select pin. It is necessary to keep $\overline{\text{RESET}}$ low for a minimum of 30 ns to complete the operation (see Figure 2). When the $\overline{\text{RESET}}$ signal is returned high, the output remains at the cleared value until a new value is programmed. The outputs cannot be updated with a new value while the $\overline{\text{RESET}}$ pin is low. There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0110 is designated for this software reset function (see Table 8). Any events on $\overline{\text{LDAC}}$ or $\overline{\text{RESET}}$ during power-on reset are ignored.

RESET SELECT PIN (RSTSEL)

The AD5686/AD5684 contain a power-on reset circuit that controls the output voltage during power-up. By connecting the RSTSEL pin low, the output powers up to zero scale. Note that this is outside the linear region of the DAC. By connecting the RSTSEL pin high, V_{OUT} powers up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC.

APPLICATIONS INFORMATION

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5686/AD5684 is via a serial bus that uses a standard protocol that is compatible with DSP processors and microcontrollers. The communications channel requires a 3- or 4-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The devices require a 24-bit data-word with data valid on the rising edge of SYNC.

AD5686/AD5684 TO ADSP-BF531 INTERFACE

The SPI interface of the AD5686/AD5684 is designed to be easily connected to industry-standard DSPs and microcontrollers. Figure 43 shows the AD5686/AD5684 connected to the Analog Devices, Inc., Blackfin® DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5686/AD5684.

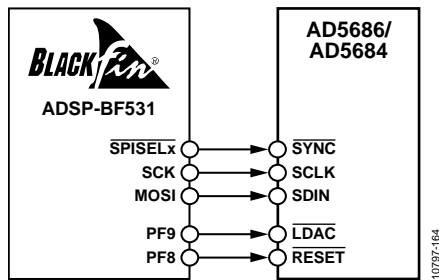


Figure 43. ADSP-BF531 Interface

AD5686/AD5684 TO SPORT INTERFACE

The Analog Devices ADSP-BF527 has one SPORT serial port. Figure 44 shows how one SPORT interface can be used to control the AD5686/AD5684.

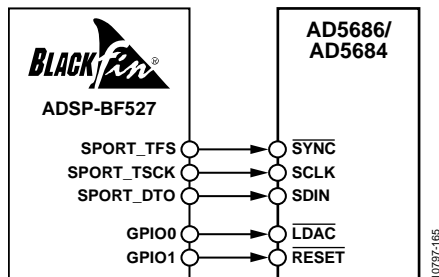


Figure 44. SPORT Interface

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The PCB on which the AD5686/AD5684 are mounted should be designed so that the AD5686/AD5684 lie on the analog plane.

The AD5686/AD5684 should have ample supply bypassing of 10 μF in parallel with 0.1 μF on each supply, located as close to the package as possible, ideally right up against the device. The 10 μF capacitors are the tantalum bead type. The 0.1 μF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

In systems where there are many devices on one board, it is often useful to provide some heat sinking capability to allow the power to dissipate easily.

The AD5686/AD5684 LFCSP models have an exposed pad beneath the device. Connect this pad to the GND supply for the part. For optimum performance, use special considerations to design the motherboard and to mount the package. For enhanced thermal, electrical, and board level performance, solder the exposed pad on the bottom of the package to the corresponding thermal land pad on the PCB. Design thermal vias into the PCB land pad area to further improve heat dissipation.

The GND plane on the device can be increased (as shown in Figure 45) to provide a natural heat sinking effect.

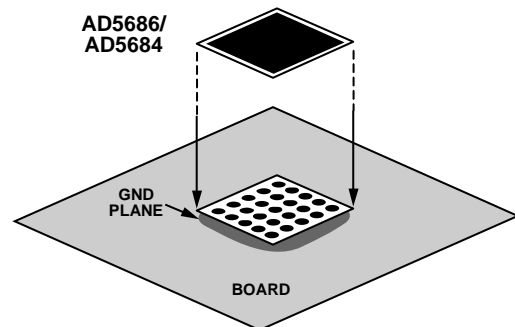
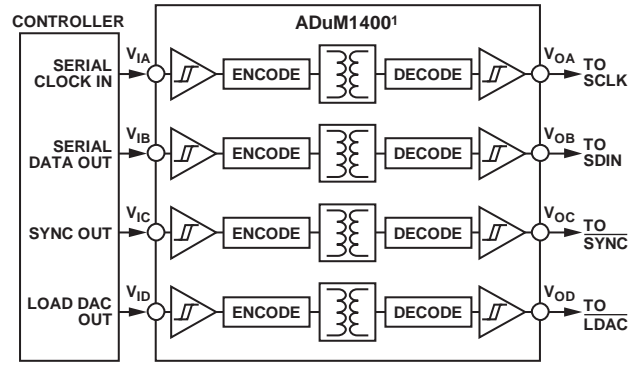


Figure 45. Pad Connection to Board

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur. *iCoupler*® products from Analog Devices provide voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5686/AD5684 makes the part ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 46 shows a 4-channel isolated interface to the AD5686/AD5684 using an ADuM1400. For more information, visit <http://www.analog.com/icouplers>.

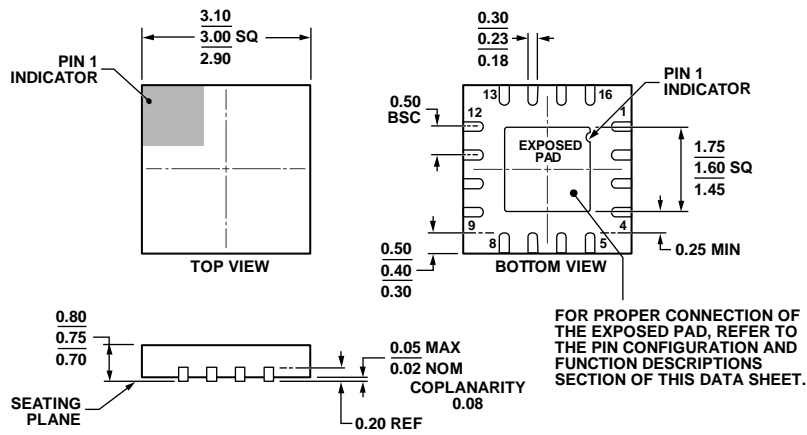


¹ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 46. Isolated Interface

10797-167

OUTLINE DIMENSIONS

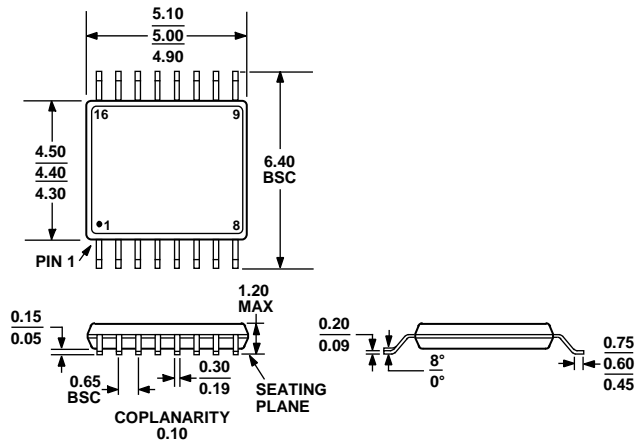


COMPLIANT TO JEDEC STANDARDS MO-220-WEED-6.

Figure 47. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm x 3 mm Body, Very Very Thin Quad
(CP-16-22)

Dimensions shown in millimeters

08-16-2010-E



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 48. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)

Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Resolution | Temperature Range | Accuracy | Package Description | Package Option | Branding |
|--------------------|------------|-------------------|------------|-------------------------|----------------|----------|
| AD5686ACPZ-RL7 | 16 Bits | -40°C to +105°C | ±8 LSB INL | 16-Lead LFCSP_WQ | CP-16-22 | DJH |
| AD5686BCPZ-RL7 | 16 Bits | -40°C to +105°C | ±2 LSB INL | 16-Lead LFCSP_WQ | CP-16-22 | DJJ |
| AD5686ARUZ | 16 Bits | -40°C to +105°C | ±8 LSB INL | 16-Lead TSSOP | RU-16 | |
| AD5686ARUZ-RL7 | 16 Bits | -40°C to +105°C | ±8 LSB INL | 16-Lead TSSOP | RU-16 | |
| AD5686BRUZ | 16 Bits | -40°C to +105°C | ±2 LSB INL | 16-Lead TSSOP | RU-16 | |
| AD5686BRUZ-RL7 | 16 Bits | -40°C to +105°C | ±2 LSB INL | 16-Lead TSSOP | RU-16 | |
| AD5684BCPZ-RL7 | 12 Bits | -40°C to +105°C | ±1 LSB INL | 16-Lead LFCSP_WQ | CP-16-22 | DJP |
| AD5684ARUZ | 12 Bits | -40°C to +105°C | ±2 LSB INL | 16-Lead TSSOP | RU-16 | |
| AD5684ARUZ-RL7 | 12 Bits | -40°C to +105°C | ±2 LSB INL | 16-Lead TSSOP | RU-16 | |
| AD5684BRUZ | 12 Bits | -40°C to +105°C | ±1 LSB INL | 16-Lead TSSOP | RU-16 | |
| AD5684BRUZ-RL7 | 12 Bits | -40°C to +105°C | ±1 LSB INL | 16-Lead TSSOP | RU-16 | |
| EVAL-AD5686RSDZ | | | | 16-Bit Evaluation Board | | |
| EVAL-AD5684RSDZ | | | | 12-Bit Evaluation Board | | |

¹ Z = RoHS Compliant Part.

NOTES