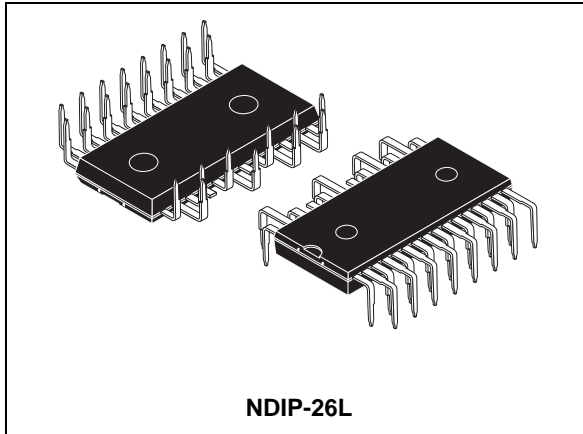


SLLIMM™-nano (small low-loss intelligent molded module) IPM, 3 A - 600 V 3-phase IGBT inverter bridge

Datasheet - production data



Features

- IPM 3 A, 600 V, 3-phase IGBT inverter bridge including control ICs for gate driving and freewheeling diodes
- Optimized for low electromagnetic interference
- $V_{CE(sat)}$ negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL input comparators with hysteresis and pull-down resistor
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Optimized pinout for easy board layout

Applications

- 3-phase inverters for motor drives
- Dish washers, refrigerator compressors, heating systems, air-conditioning fans, draining and recirculation pumps

Description

This intelligent power module implements a compact, high-performance AC motor drive in a simple, rugged design. It is composed of six IGBTs with freewheeling diodes and three half-bridge HVICs for gate driving, providing low electromagnetic interference (EMI) characteristics with optimized switching speed. The package is optimized for thermal performance and compactness in built-in motor applications, or other low power applications where assembly space is limited. SLLIMM™ is a trademark of STMicroelectronics.

Table 1. Device summary

Order code	Marking	Package	Packaging
STGIPN3H60A	GIPN3H60A	NDIP-26L	Tube

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1 Internal schematic diagram and pin configuration

Figure 1. Internal schematic diagram

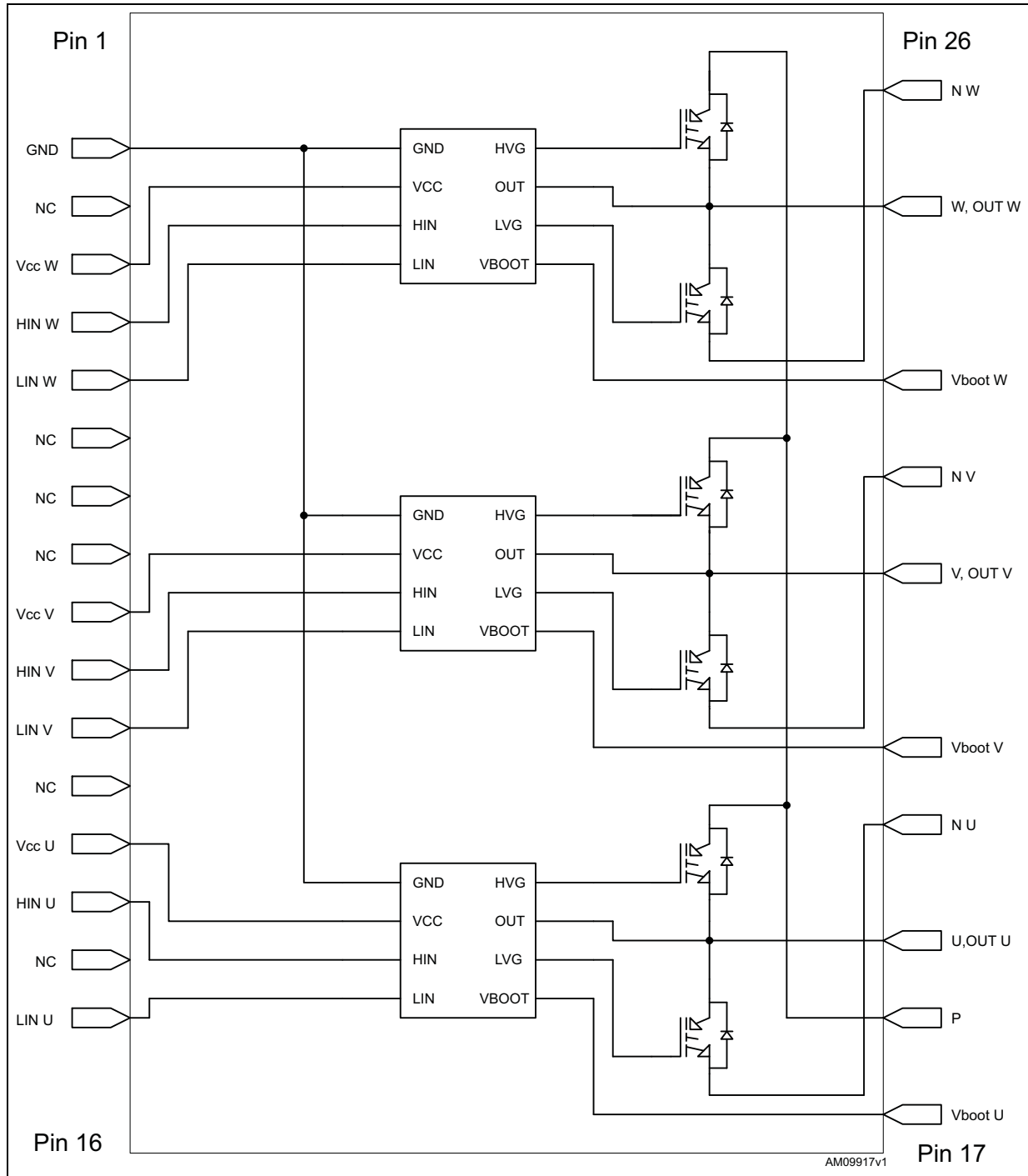
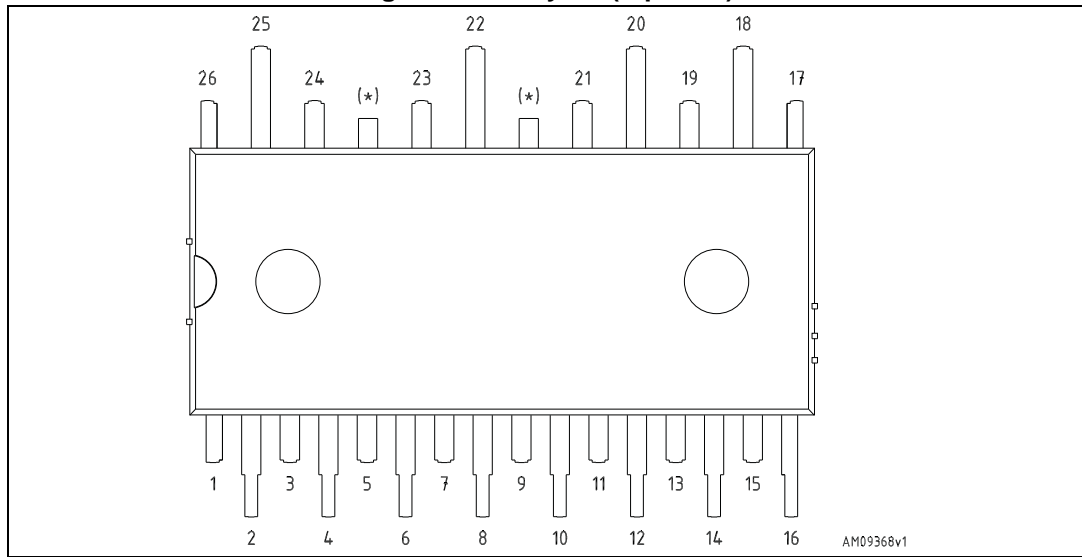


Table 2. Pin description

Pin	Symbol	Description
1	GND	Ground
2	NC	Not connected
3	V _{CC} W	Low voltage power supply W phase
4	HIN W	High side logic input for W phase
5	LIN W	Low side logic input for W phase
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	V _{CC} V	Low voltage power supply V phase
10	HIN V	High side logic input for V phase
11	LIN V	Low side logic input for V phase
12	NC	Not connected
13	V _{CC} U	Low voltage power supply for U phase
14	HIN U	High side logic input for U phase
15	NC	Not connected
16	LIN U	Low side logic input for U phase
17	V _{boot} U	Bootstrap voltage for U phase
18	P	Positive DC input
19	U	U phase output
20	N _U	Negative DC input for U phase
21	V _{boot} V	Bootstrap voltage for V phase
22	V	V phase output
23	N _V	Negative DC input for V phase
24	V _{boot} W	Bootstrap voltage for W phase
25	W	W phase output
26	N _W	Negative DC input for W phase

Figure 2. Pin layout (top view)



(*) Dummy pin internally connected to P (positive DC input).

2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{CES}	Each IGBT collector emitter voltage ($V_{IN}^{(1)} = 0$)	600	V
$\pm I_C^{(2)}$	Each IGBT continuous collector current at $T_C = 25\text{ °C}$	3	A
$\pm I_{CP}^{(3)}$	Each IGBT pulsed collector current	18	A
P_{TOT}	Each IGBT total dissipation at $T_C = 25\text{ °C}$	8	W

1. Applied between HIN_i , LIN_i and G_{ND} for $i = U, V, W$.
2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature.

Table 4. Control part

Symbol	Parameter	Min.	Max.	Unit
V_{OUT}	Output voltage applied between OUT_U , OUT_V , OUT_W - GND	$V_{boot} - 18$	$V_{boot} + 0.3$	V
V_{CC}	Low voltage power supply	- 0.3	18	V
V_{boot}	Bootstrap voltage	- 0.3	618	V
V_{IN}	Logic input voltage applied between HIN_i , LIN_i and G_{ND} for $i = U, V, W$	- 0.3	$V_{CC} + 0.3$	V
$\Delta V_{OUT/dT}$	Allowed output slew rate		50	V/ns

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, $t = 60\text{ sec.}$)	1000	V
T_J	Power chips operating junction temperature	-40 to 150	°C
T_C	Module case operating temperature	-40 to 125	°C

2.2 Thermal data

Table 6. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	50	°C/W

3 Electrical characteristics

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 7. Inverter part

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 - 5\text{ V}$, $I_C = 1\text{ A}$	-	2.15	2.6	V
		$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 - 5\text{ V}$, $I_C = 1\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$	-	1.65		
I_{CES}	Collector-cut off current ($V_{IN}^{(1)} = 0$ "logic state")	$V_{CE} = 550\text{ V}$, $V_{CC} = V_{Boot} = 15\text{ V}$	-		250	μA
V_F	Diode forward voltage	$V_{IN}^{(1)} = 0$ "logic state", $I_C = 1\text{ A}$	-		1.7	V
Inductive load switching time and energy						
t_{on}	Turn-on time	$V_{DD} = 300\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 - 5\text{ V}$, $I_C = 1\text{ A}$ (see Figure 4)	-	275		ns
$t_{c(on)}$	Crossover time (on)		-	90		
t_{off}	Turn-off time		-	890		
$t_{c(off)}$	Crossover time (off)		-	125		
t_{rr}	Reverse recovery time		-	50		
E_{on}	Turn-on switching losses		-	18		μJ
E_{off}	Turn-off switching losses	-	13			

1. Applied between HIN_i , \overline{LIN}_i and G_{ND} for $i = U, V, W$ (\overline{LIN}_i inputs are active-low).

Note: t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

Figure 3. Switching time test circuit

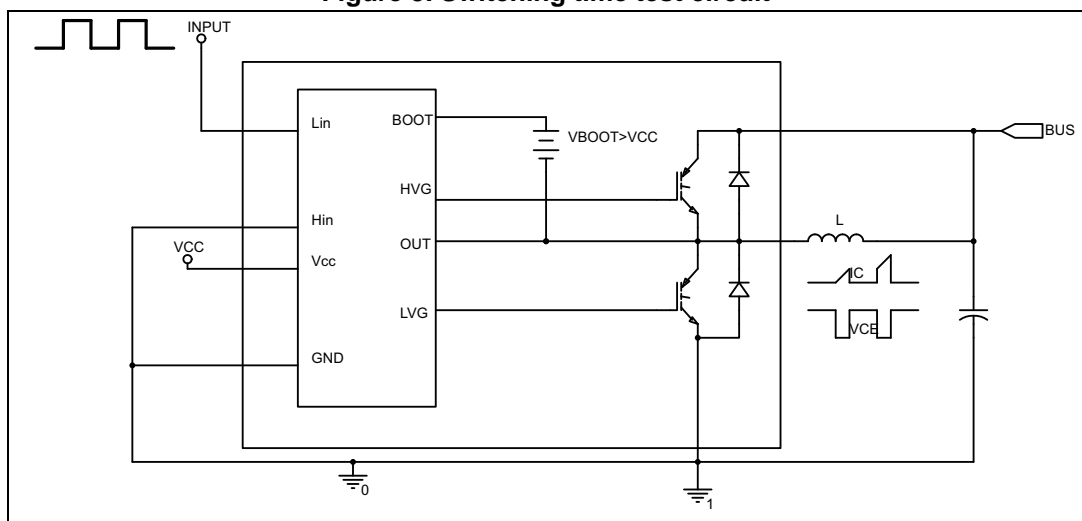
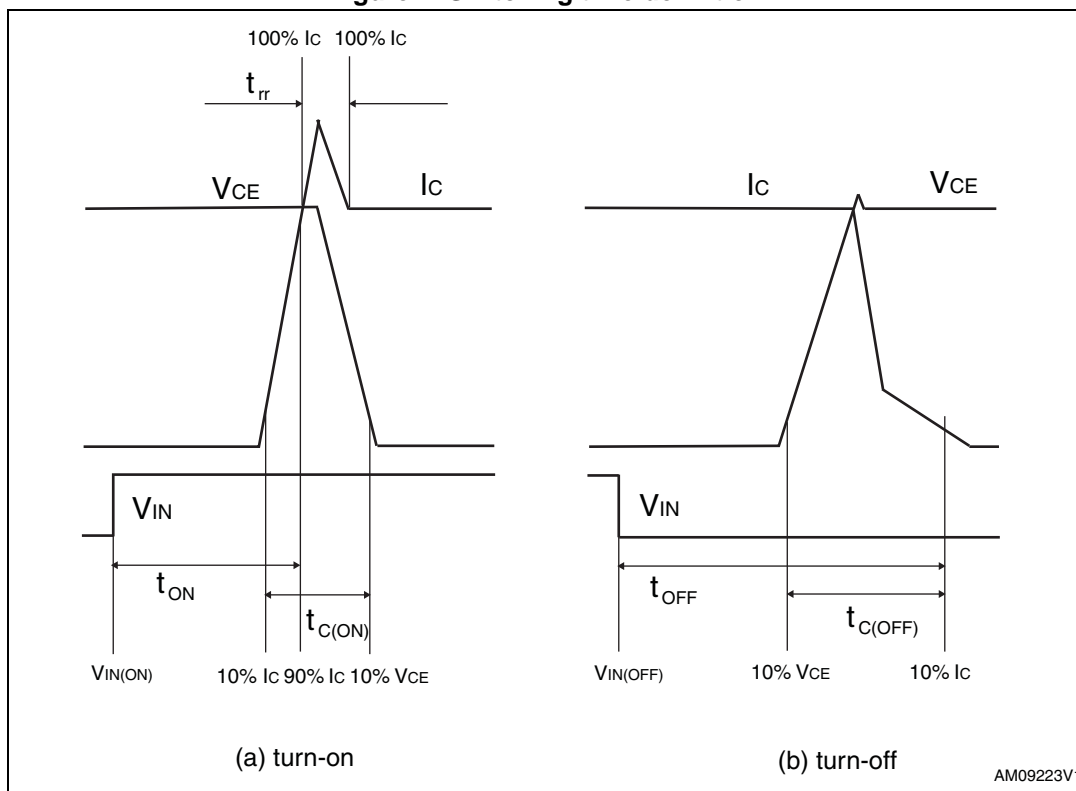


Figure 4. Switching time definition



3.1 Control part

Table 8. Low voltage power supply ($V_{CC} = 15\text{ V}$ unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CCthON}	Undervoltage turn-on threshold		9.1	9.6	10.1	V
$V_{CCthOFF}$	Undervoltage turn-off threshold		7.9	8.3	8.8	V
V_{CChys}	Undervoltage hystereses		0.9			V
I_{qccu}	Undervoltage quiescent supply current	$V_{CC} < 7.9\text{ V}$		250	330	μA
I_{qcc}	Quiescent current	$V_{CC} = 15\text{ V}$		350	450	μA

Table 9. Bootstrapped voltage ($V_{CC} = 15\text{ V}$ unless otherwise specified)

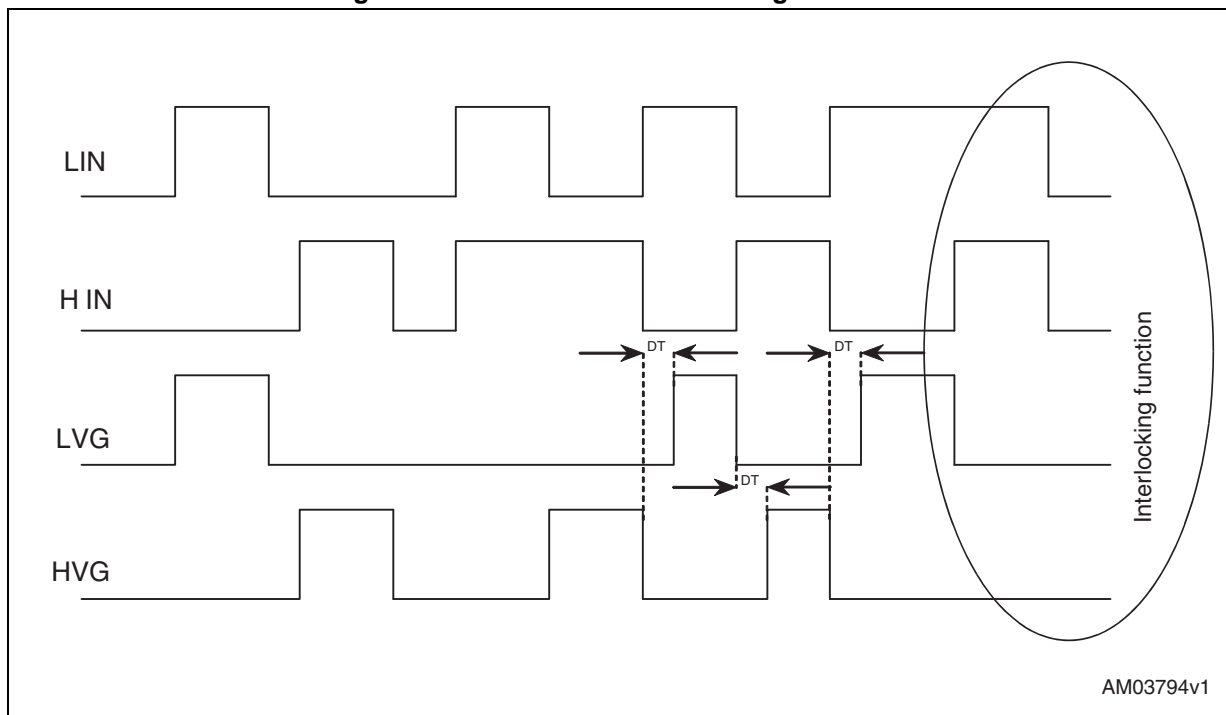
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{boot_thON}	Undervoltage turn-on threshold		8.5	9.5	10.5	V
V_{boot_thOFF}	Undervoltage turn-off threshold		7.2	8.3	9.2	V
V_{bootys}	Undervoltage hysteresis		0.9			V
I_{qboot}	Quiescent current				250	μA
$R_{DS(on)}$	Bootstrap driver on-resistance	$V_{CC} > 12.5\text{ V}$		125		Ω

Table 10. Logic inputs ($V_{CC} = 15\text{ V}$ unless otherwise specified) ⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low level logic input voltage				1.1	V
V_{ih}	High level logic input voltage		1.8			V
I_{il}	Low level logic input current	$V_{IN}^{(2)} = 0$	-1			μA
I_{ih}	High level logic input current	$V_{IN}^{(1)} = 15\text{ V}$		20	70	μA
Dt	Dead time			320		ns

1. See [Figure 5: Dead time and interlocking definition](#).
2. Applied between HIN_i , LIN_i and G_{ND} for $i = U, V, W$

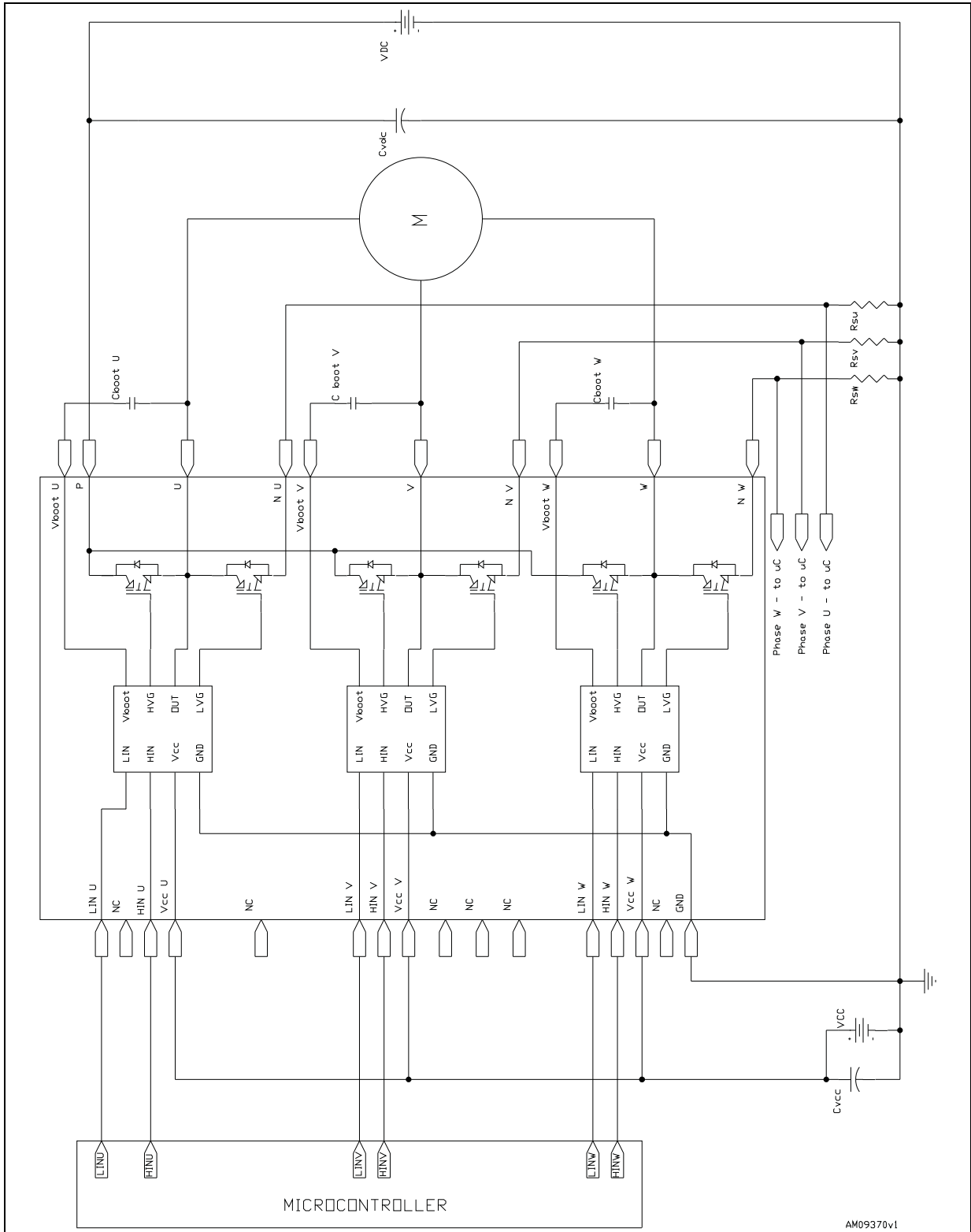
Figure 5. Dead time and interlocking definition



AM03794v1

4 Application information

Figure 6. Typical application circuit



4.1 Recommendations

- Input signals HIN, LIN are active-high logic. A 500 k Ω (typ.) pull-down resistor is built-in for each high side input. If an external RC filter is used for noise immunity, attention should be given to the variation of the input signal level.
- To prevent input signal oscillation, the wiring of each input should be as short as possible.
- By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an opto-coupler is possible.
- Each capacitor should be located as close as possible to the pins of the IPM.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitors mounted close to the module pins will further improve performance.

Table 11. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{PN}	Supply voltage	Applied between P-Nu, Nv, Nw		300	500	V
V _{CC}	Control supply voltage	Applied between V _{CC} -GND	12	15	17	V
V _{BS}	High side bias voltage	Applied between V _{BOOTi} -OUT _i for i = U, V, W	11.5		17	V
t _{dead}	Blanking time to prevent Arm-short	For each input signal	1.5			μ s
f _{PWM}	PWM input signal	-40°C < T _c < 100°C -40°C < T _j < 125°C			25	kHz
T _C	Case operation temperature				100	°C

Note: For further details refer to AN4043.

5 Package mechanical data

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Figure 7. NDIP-26L drawing

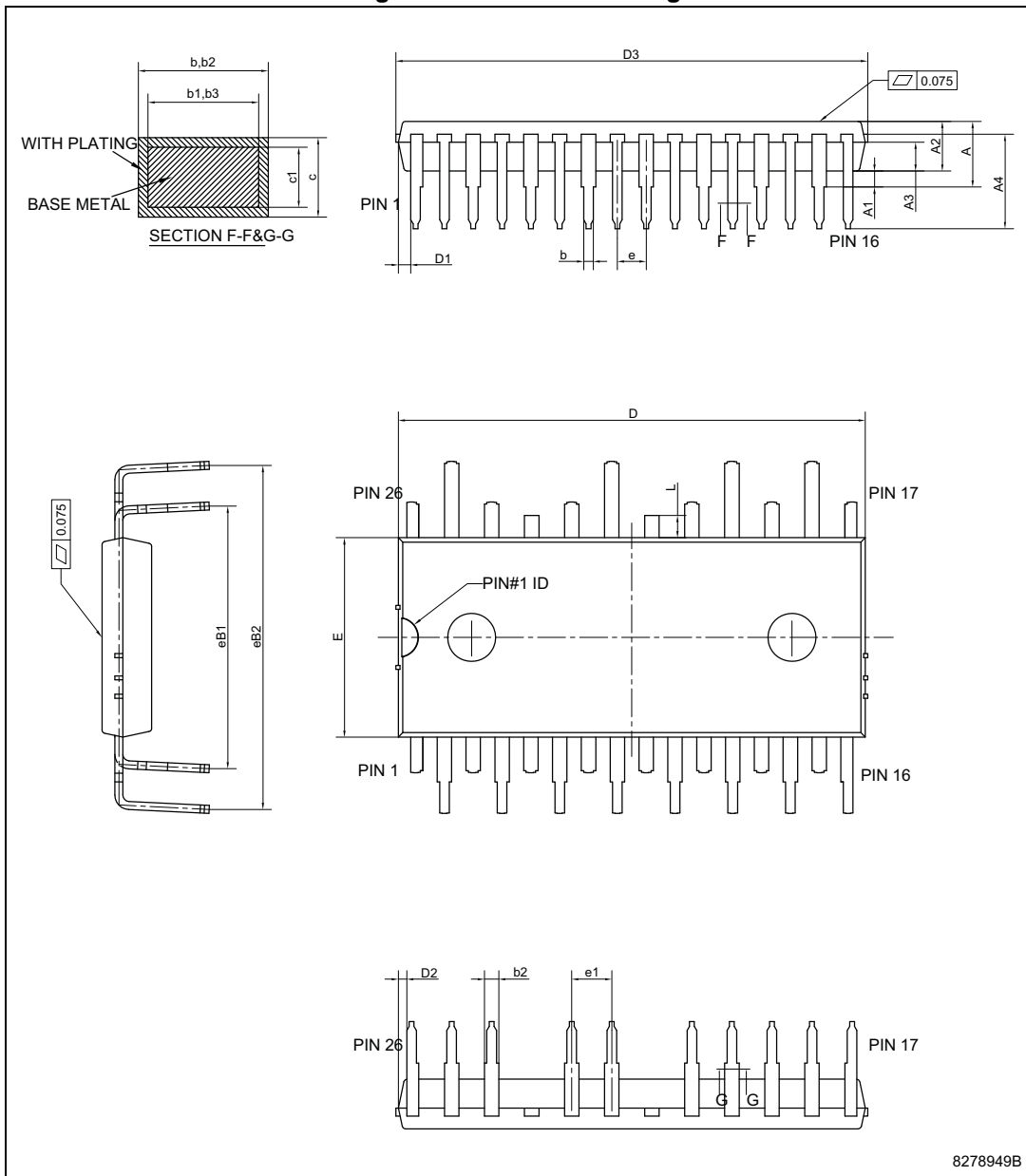


Table 12.NDIP-26L mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			4.40
A1	0.80	1.00	1.20
A2	3.00	3.10	3.20
A3	1.70	1.80	1.90
A4	5.70	5.90	6.10
b	0.53		0.72
b1	0.52	0.60	0.68
b2	0.83		1.02
b3	0.82	0.90	0.98
c	0.46		0.59
c1	0.45	0.50	0.55
D	29.05	29.15	29.25
D1	0.50	0.77	1.00
D2	0.35	0.53	0.70
D3			29.55
E	12.35	12.45	12.55
e	1.70	1.80	1.90
e1	2.40	2.50	2.60
eB1	16.10	16.40	16.70
eB2	21.18	21.48	21.78
L	1.24	1.39	1.54

6 Revision history

Table 13. Document revision history

Date	Revision	Changes
23-Jun-2011	1	Initial release.
09-Jan-2012	2	Document status promoted from preliminary data to datasheet. Added Figure 8 on page 15 .
03-Jul-2012	3	Modified: Min. and Max. value Table 4 on page 6 . Added: Table 11 on page 12 .
14-Mar-2014	4	Updated Figure 3: Switching time test circuit . Updated Section 5: Package mechanical data .

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