VS-VSKCS209/150

Vishay Semiconductors





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PRODUCT SUMMARY			
I _{F(AV)}	200 A		
V _R	150 V		
Package	ADD-A-PAK		
Circuit	Two diodes common cathodes		

MECHANICAL DESCRIPTION

The ADD-A-PAK generation VII, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

FEATURES

- 175 °C T_J operation
- Low forward voltage drop
- High frequency operation
- Low thermal resistance
- UL approved file E78996
- Designed and qualified for industrial level
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- High surge capability
- Easy mounting on heatsink

ELECTRICAL DESCRIPTION

The VS-VSKCS209.. Schottky rectifier common cathode has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature.

Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

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MAJOR RATINGS AND CHARACTERISTICS					
SYMBOL	CHARACTERISTICS	CHARACTERISTICS VALUES			
I _{F(AV)}	Rectangular waveform	200	A		
V _{RRM}		150	V		
I _{FSM}	t _p = 5 μs sine	11 300	А		
V _F	100 A _{pk} , T _J = 125 °C	0.85	V		
TJ	Range	-55 to 175	°C		

VOLTAGE RATINGS				
PARAMETER SYMBOL		VS-VSKCS209/150	UNITS	
Maximum DC reverse voltage	DC reverse voltage V _R		V	
Maximum working peak reverse voltage	V _{RWM}	150	v	

Pb-free RoHS

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ABSOLUTE MAXIMUM RATINGS						
PARAMETER		SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average	per module		50 % duty cycle at T _C = 113 °C, rectangular waveform		200	
forward current	per leg	I _{F(AV)}	30% duty cycle at $1^\circ_{\rm C} = 113\%$, rectangular wavelonn	100	
Maximum peak one cycle		5 µs sine or 3 µs rect. pulse	Following any rated load condition and with	11 300	A	
non-repetitive surge current		IFSM	10 ms sine or 6 ms rect. pulse	rated V_{RRM} applied	1600	
Non-repetitive avalanche energ	у	E _{AS}	$T_J = 25 \text{ °C}, I_{AS} = 1.8 \text{ A}, L = 10 \text{ mH}$ 15		mJ	
Repetitive avalanche current		I _{AR}	Current decaying linearly to zero in 1 μ s Frequency limited by T _J maximum V _A = 1.5 x V _R typical 1		А	

ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
	V _{FM}	100 A	T.I = 25 °C	1.01	V
Maximum forward voltage drop		200 A	1j=25 0	1.35	
Maximum forward voltage drop		100 A	T _J = 125 °C	0.85	
		200 A		1.13	
	I _{RM}	$T_J = 25 \ ^{\circ}C$	V _R = Rated V _R	6	mA
Maximum reverse leakage current		T _J = 125 °C		85	mA
Maximum junction capacitance	CT	V_{R} = 5 V_{DC} (test signal range 100 kHz to 1 MHz), 25 °C		3000	pF
Typical series inductance	L _S	Measured lead to lead 5 mm from package body		7.0	nH
Maximum voltage rate of change	dV/dt	Rated V _R		10 000	V/µs
Maximum RMS insulation voltage	V _{INS}	50 Hz		3000 (1 min) 3600 (1 s)	V

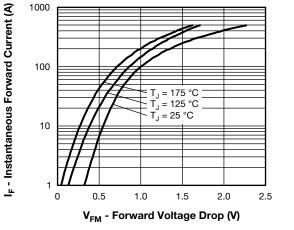
THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER		SYMBOL TEST CONDITIONS		VALUES	UNITS	
Maximum junction and storage temperature range	9	T _J , T _{Stg}		- 55 to 175	°C	
Maximum thermal resistance, junction to case per leg		R _{thJC}	DC operation	0.52	°C/W	
Typical thermal resistance, case to heatsink per module		R _{thCS}		0.1		
				75	g	
Approximate weight				2.7	oz.	
Mounting torque ± 10 %		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for	4	Nm		
	busbar		the spread of the compound.	3		
Case style			JEDEC®	TO-240AA co	mpatible	

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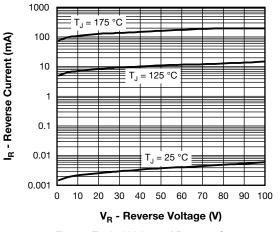
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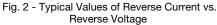


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Fig. 1 - Maximum Forward Voltage Drop Characteristics





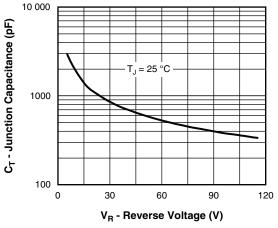


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

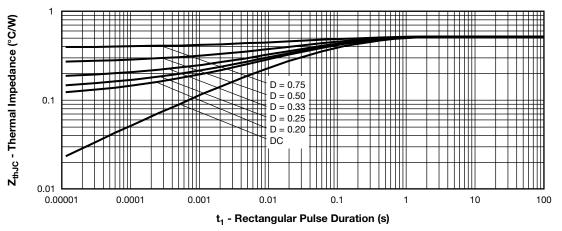
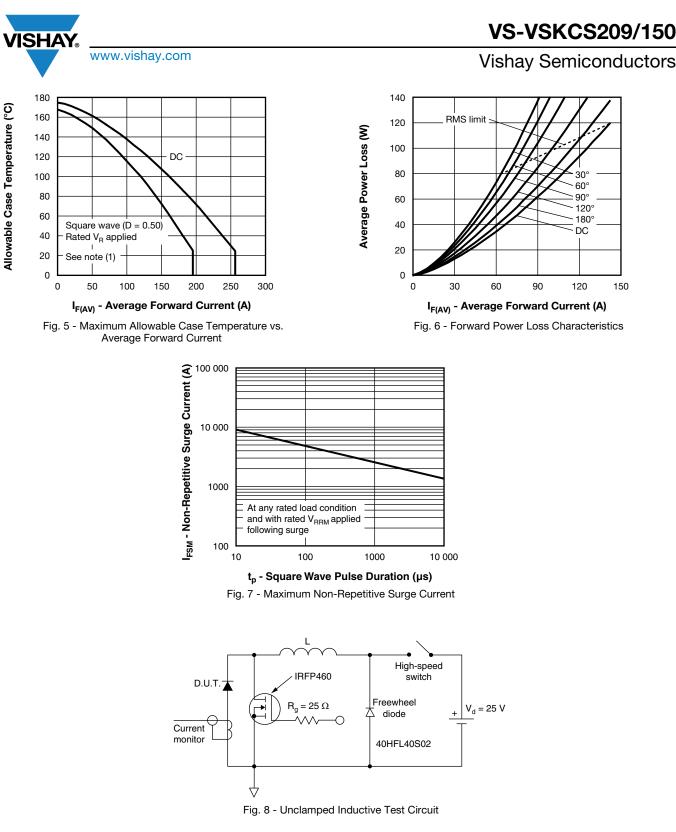


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

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Note

- ⁽¹⁾ Formula used: $T_C = T_J (Pd + Pd_{REV}) \times R_{thJC}$;
 - Pd = Forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6);
 - Pd_{REV} = Inverse power loss = $V_{R1} \times I_R (1 D)$; I_R at V_{R1} = 80 % rated V_R

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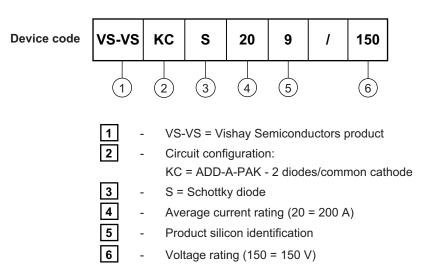
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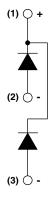
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ORDERING INFORMATION TABLE



CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS				
Dimensions	www.vishay.com/doc?95369			



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