

TIP100, TIP101, TIP102 (NPN); TIP105, TIP106, TIP107 (PNP)

TIP101, TIP102, TIP106 and TIP107 are Preferred Devices

Plastic Medium-Power Complementary Silicon Transistors

Designed for general-purpose amplifier and low-speed switching applications.

Features

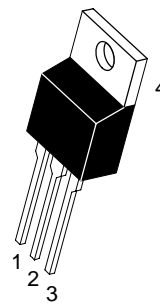
- High DC Current Gain –
 $h_{FE} = 2500$ (Typ) @ I_C
 $= 4.0$ Adc
- Collector–Emitter Sustaining Voltage – @ 30 mAdc
 $V_{CEO(sus)} = 60$ Vdc (Min) – TIP100, TIP105
 $= 80$ Vdc (Min) – TIP101, TIP106
 $= 100$ Vdc (Min) – TIP102, TIP107
- Low Collector–Emitter Saturation Voltage –
 $V_{CE(sat)} = 2.0$ Vdc (Max) @ I_C
 $= 3.0$ Adc
 $= 2.5$ Vdc (Max) @ $I_C = 8.0$ Adc
- Monolithic Construction with Built-in Base–Emitter Shunt Resistors
- Pb–Free Packages are Available*



ON Semiconductor®

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DARLINGTON 8 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60–80–100 VOLTS, 80 WATTS



MARKING DIAGRAM



TO-220AB
CASE 221A
STYLE 1

TIP10x = Device Code
x = 0, 1, 2, 5, 6, or 7
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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MAXIMUM RATINGS

Rating	Symbol	TIP100, TIP105	TIP101, TIP106	TIP102, TIP107	Unit
Collector – Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector – Base Voltage	V_{CB}	60	80	100	Vdc
Emitter – Base Voltage	V_{EB}	5.0			Vdc
Collector Current – Continuous – Peak	I_C	8.0 15			Adc
Base Current	I_B	1.0			Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	80 0.64			W W/ $^\circ\text{C}$
Unclamped Inductive Load Energy (1)	E	30			mJ
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2.0 0.016			W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.56	$^\circ\text{C/W}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. $I_C = 1.1\text{ A}$, $L = 50\text{ mH}$, P.R.F. = 10 Hz, $V_{CC} = 20\text{ V}$, $R_{BE} = 100\ \Omega$

ORDERING INFORMATION

Device	Package	Shipping
TIP100	TO–220	50 Units / Rail
TIP100G	TO–220 (Pb–Free)	50 Units / Rail
TIP101	TO–220	50 Units / Rail
TIP101G	TO–220 (Pb–Free)	50 Units / Rail
TIP102	TO–220	50 Units / Rail
TIP102G	TO–220 (Pb–Free)	50 Units / Rail
TIP105	TO–220	50 Units / Rail
TIP105G	TO–220 (Pb–Free)	50 Units / Rail
TIP106	TO–220	50 Units / Rail
TIP106G	TO–220 (Pb–Free)	50 Units / Rail
TIP107	TO–220	50 Units / Rail
TIP107G	TO–220 (Pb–Free)	50 Units / Rail

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) ($I_C = 30\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	60 80 100	– – –	Vdc
Collector Cutoff Current ($V_{CE} = 30\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 40\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 50\text{ Vdc}$, $I_B = 0$)	I_{CEO}	– – –	50 50 50	μA
Collector Cutoff Current ($V_{CB} = 60\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 80\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 100\text{ Vdc}$, $I_E = 0$)	I_{CBO}	– – –	50 50 50	μA
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	8.0	mA
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 3.0\text{ A}$, $V_{CE} = 4.0\text{ Vdc}$) ($I_C = 8.0\text{ A}$, $V_{CE} = 4.0\text{ Vdc}$)	h_{FE}	1000 200	20,000 –	–
Collector–Emitter Saturation Voltage ($I_C = 3.0\text{ A}$, $I_B = 6.0\text{ mA}$) ($I_C = 8.0\text{ A}$, $I_B = 80\text{ mA}$)	$V_{CE(sat)}$	– –	2.0 2.5	Vdc
Base–Emitter On Voltage ($I_C = 8.0\text{ A}$, $V_{CE} = 4.0\text{ Vdc}$)	$V_{BE(on)}$	–	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Small–Signal Current Gain ($I_C = 3.0\text{ A}$, $V_{CE} = 4.0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	h_{fe}	4.0	–	–
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	– –	300 200	pF

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

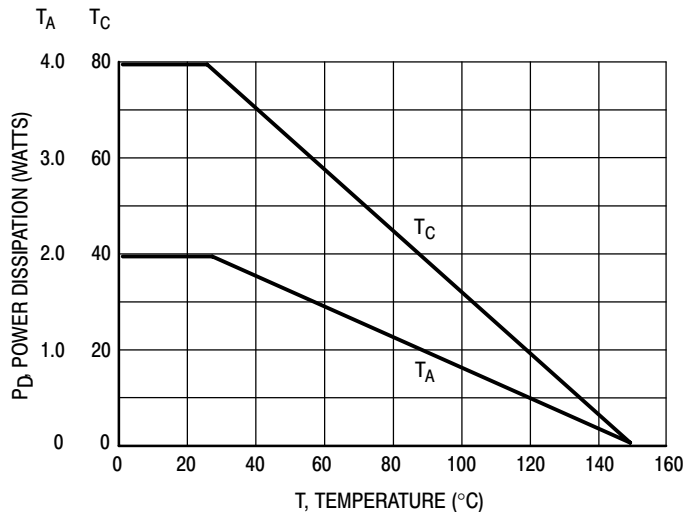


Figure 1. Power Derating

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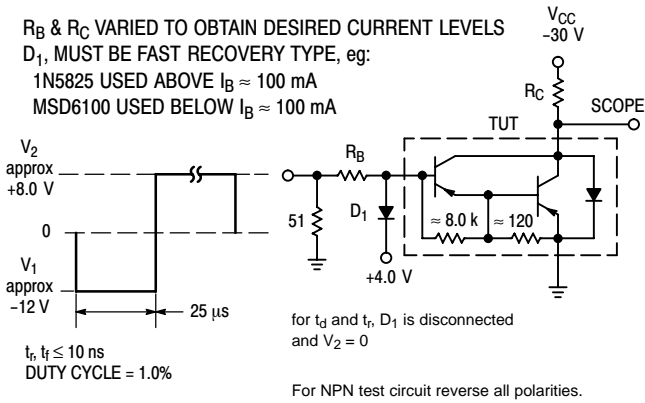


Figure 2. Switching Times Test Circuit

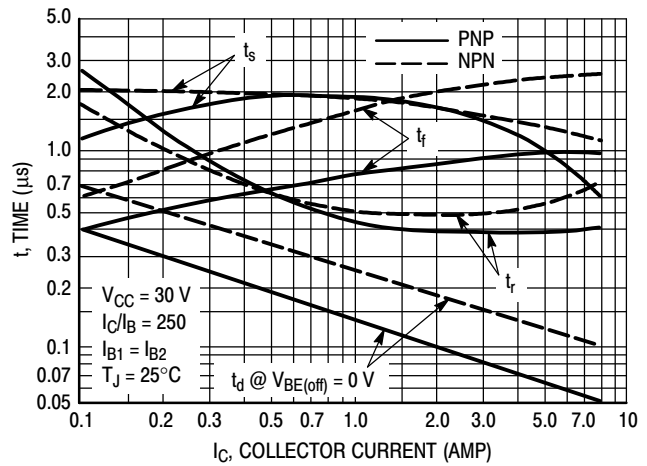


Figure 3. Switching Times

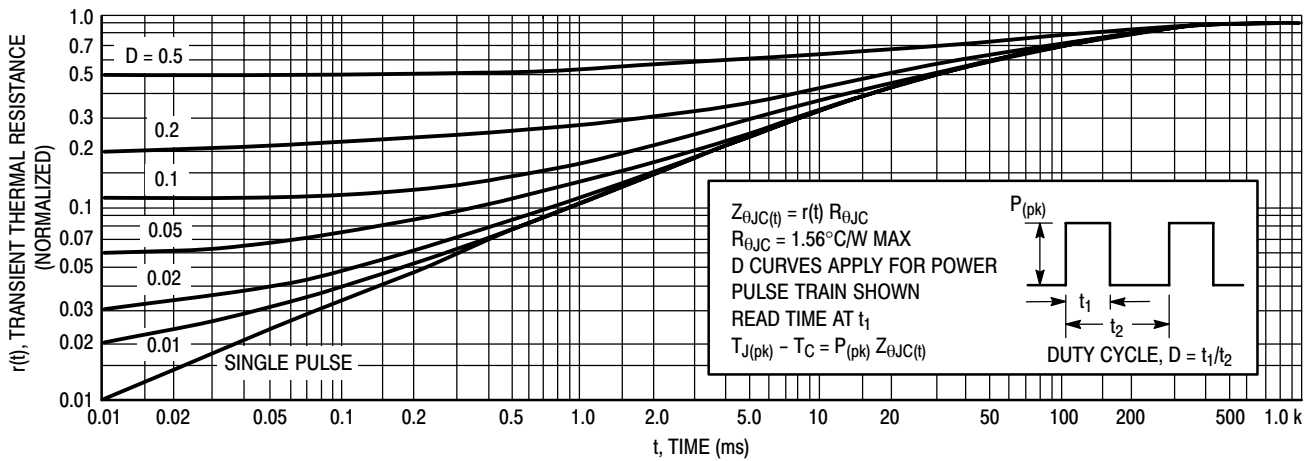


Figure 4. Thermal Response

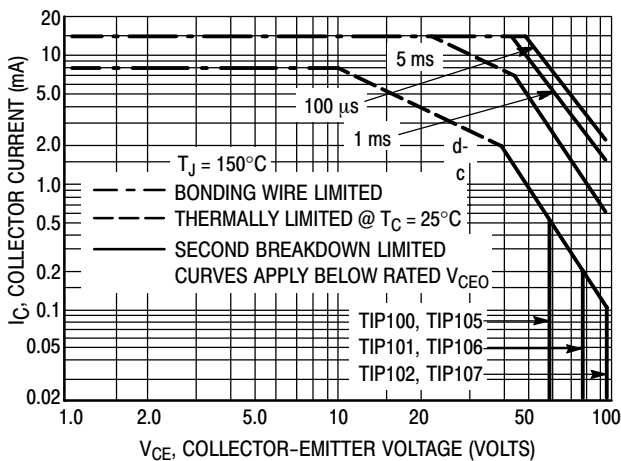


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown

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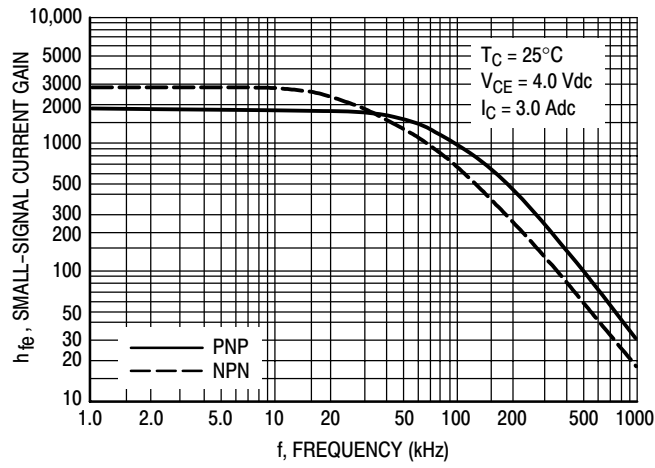


Figure 6. Small-Signal Current Gain

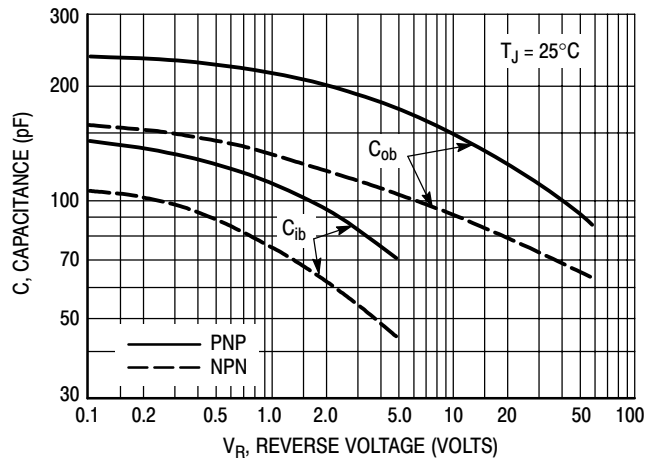


Figure 7. Capacitance

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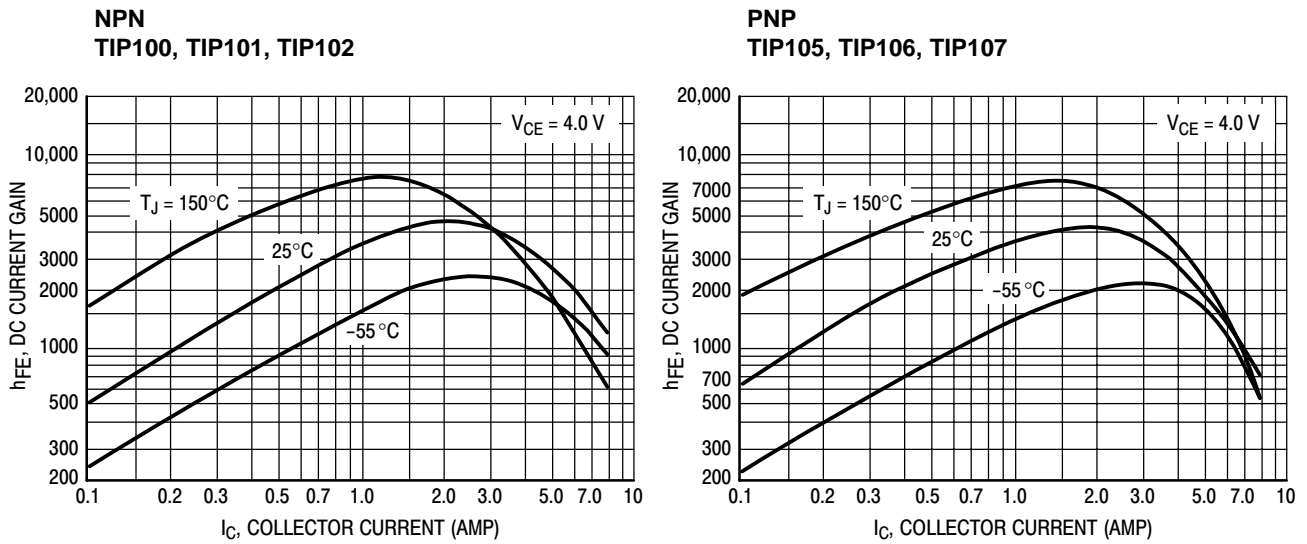


Figure 8. DC Current Gain

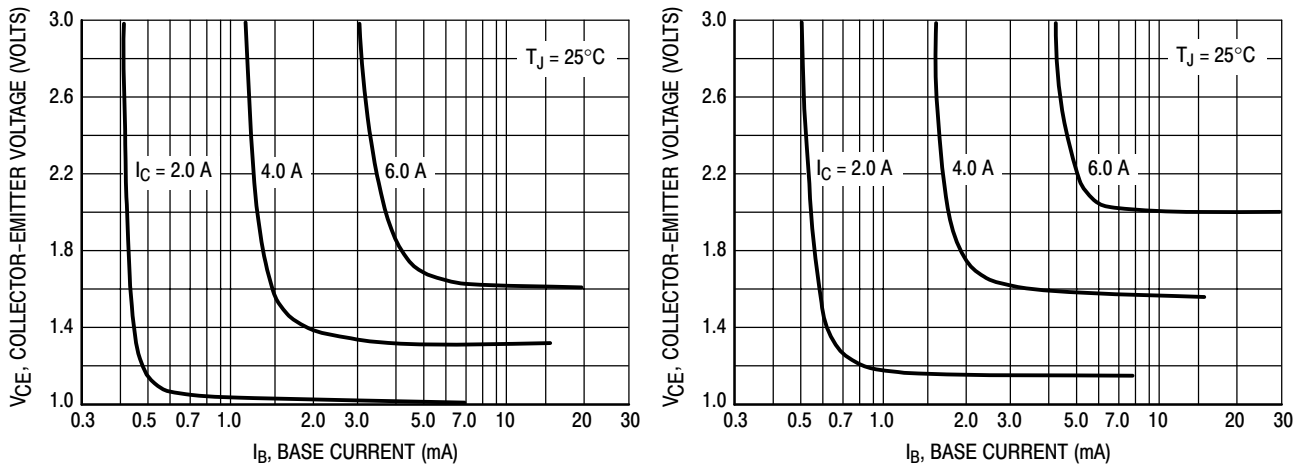


Figure 9. Collector Saturation Region

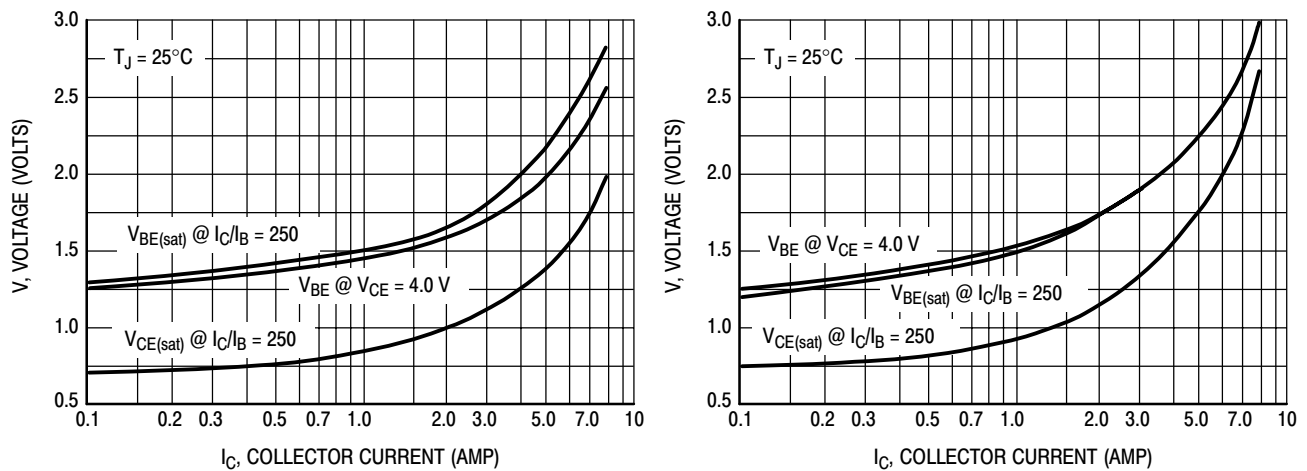
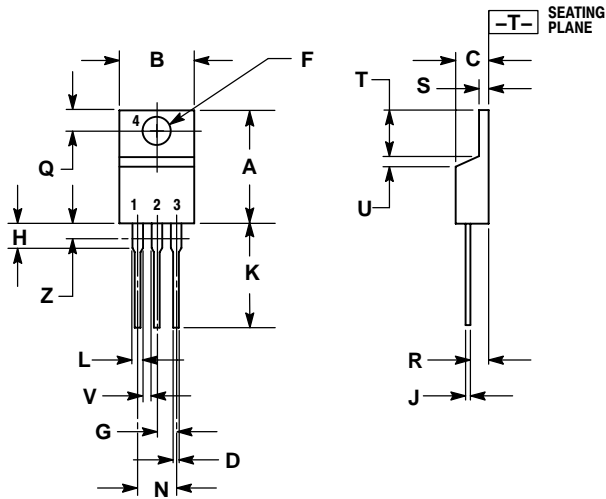


Figure 10. "On" Voltages

TIP100, TIP101, TIP102 (NPN); TIP105, TIP106, TIP107 (PNP)

PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AA




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

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