DATA SHEET

PEMD48; PUMD48

NPN/PNP resistor-equipped transistors;
R1 = 47 kΩ, R2 = 47 kΩ
and R1 = 2.2 kΩ, R2 = 47 kΩ

Product specification
Supersedes data of 2004 Jun 02

2004 Jun 24

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NPN/PNP resistor-equipped transistors; R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

PEMD48; PUMD48

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- Low current peripheral driver
- Replacement of general purpose transistors in digital applications
- Control of IC inputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	–	50	V
I_{CM}	peak collector current	–	100	mA
Transistor TR1 (NPN)				
R1	bias resistor	47	–	kΩ
R2	bias resistor	47	–	kΩ
Transistor TR2 (PNP)				
R1	bias resistor	2.2	–	kΩ
R2	bias resistor	47	–	kΩ

DESCRIPTION

NPN/PNP resistor-equipped transistors (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP/PNP COMPLEMENT	NPN/NPN COMPLEMENT
	PHILIPS	EIAJ			
PEMD48	SOT666	–	48	–	–
PUMD48	SOT363	SC-88	4*8(1)	–	–

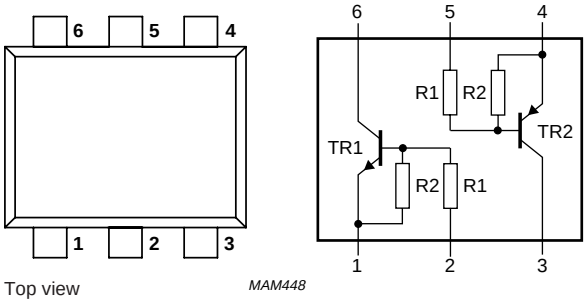
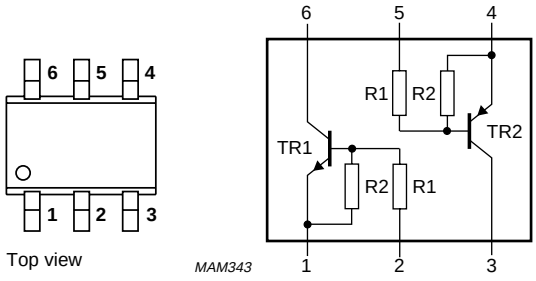
Note

1. * = p: Made in Hong Kong.
   * = t: Made in Malaysia.
   * = W: Made in China.

NPN/PNP resistor-equipped transistors; R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

PEMD48; PUMD48

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PEMD48		1 2 3 4 5 6	emitter TR1 base TR1 collector TR2 emitter TR2 base TR2 collector TR1
PUMD48		1 2 3 4 5 6	emitter TR1 base TR1 collector TR2 emitter TR2 base TR2 collector TR1

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PEMD48	–	plastic surface mounted package; 6 leads	SOT666
PUMD48	–	plastic surface mounted package; 6 leads	SOT363

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity					
V_{CBO}	collector-base voltage	open emitter	–	50	V
V_{CEO}	collector-emitter voltage	open base	–	50	V
V_{EBO}	emitter-base voltage	open collector	–	10	V
V_I	input voltage TR1				
	positive		–	+40	V
	negative		–	–10	V
	input voltage TR2				
	positive		–	+5	V
	negative		–	–12	V
I_O	output current (DC)		–	100	mA
I_{CM}	peak collector current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
	SOT363	note 1	–	200	mW
	SOT666	notes 1 and 2	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
	SOT363	note 1	–	300	mW
	SOT666	notes 1 and 2	–	300	mW

Notes

1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
2. The only recommended soldering method is reflow soldering.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per transistor				
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25$ °C		
	SOT363	note 1	625	K/W
	SOT666	notes 1 and 2	625	K/W
Per device				
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25$ °C		
	SOT363	note 1	416	K/W
	SOT666	notes 1 and 2	416	K/W

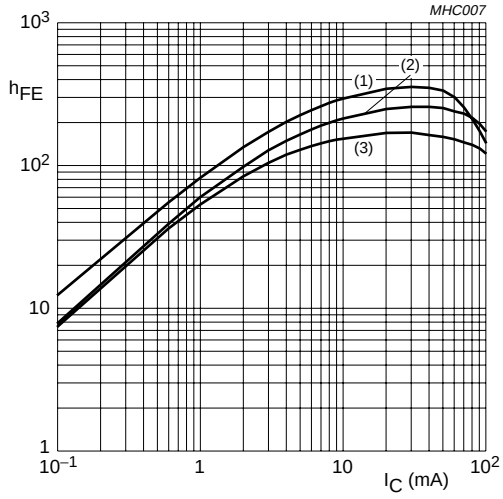
Notes

1. Transistor mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
2. The only recommended soldering method is reflow soldering.

CHARACTERISTICS

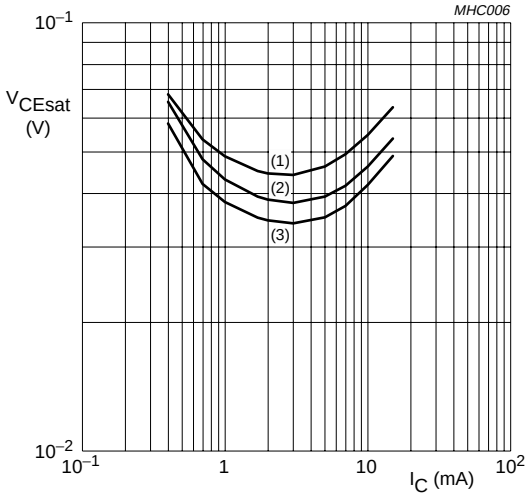
T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A	–	–	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A	–	–	1	μA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C	–	–	50	μA
Transistor TR1 (NPN)						
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A	–	–	90	μA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 5 mA	80	–	–	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA	–	–	150	mV
$V_{i(off)}$	input-off voltage	I_C = 100 μA; V_{CE} = 5 V	–	1.2	0.8	V
$V_{i(on)}$	input-on voltage	I_C = 2 mA; V_{CE} = 0.3 V	3	1.6	–	V
R1	input resistor		33	47	61	kΩ
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$I_E = i_e$ = 0 A; V_{CB} = 10 V; f = 1 MHz	–	–	2.5	pF
Transistor TR2 (PNP)						
I_{EBO}	emitter-base cut-off current	V_{EB} = –5 V; I_C = 0 A	–	–	–180	μA
h_{FE}	DC current gain	V_{CE} = –5 V; I_C = –10 mA	100	–	–	
V_{CEsat}	collector-emitter saturation voltage	I_C = –5 mA; I_B = –0.25 mA	–	–	–100	mV
$V_{i(off)}$	input-off voltage	I_C = –100 μA; V_{CE} = –5 V	–	–0.6	–0.5	V
$V_{i(on)}$	input-on voltage	I_C = –5 mA; V_{CE} = –0.3 V	–1.1	–0.75	–	V
R1	input resistor		1.54	2.2	2.86	kΩ
$\frac{R2}{R1}$	resistor ratio		17	21	26	
C_c	collector capacitance	$I_E = i_e$ = 0 A; V_{CB} = –10 V; f = 1 MHz	–	–	3	pF



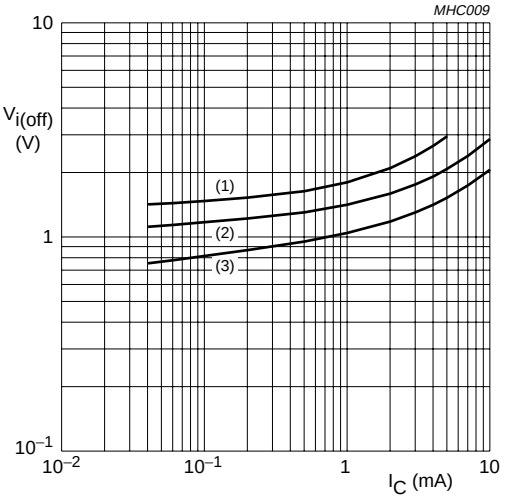
TR1 (NPN); V_{CE} = 5 V.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = –40 °C.

Fig.1 DC current gain as a function of collector current; typical values.



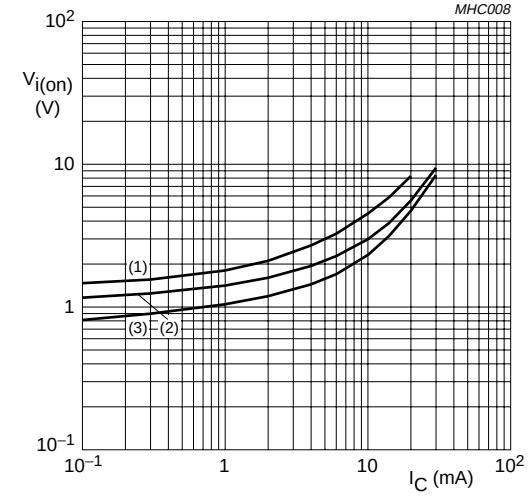
TR1 (NPN); I_C/I_B = 20.
(1) T_{amb} = 100 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = –40 °C.

Fig.2 Collector-emitter saturation voltage as a function of collector current; typical values.



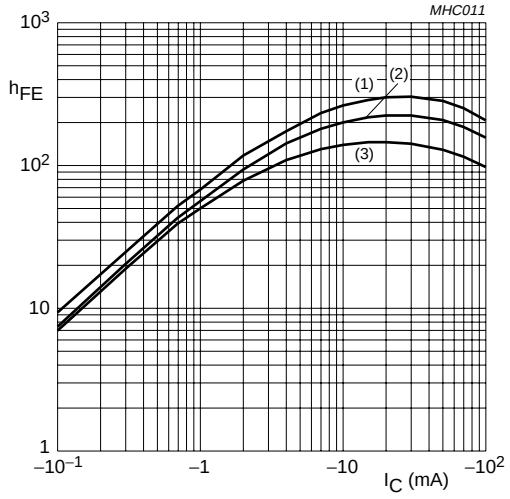
TR1 (NPN); V_{CE} = 5 V.
(1) T_{amb} = –40 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = 100 °C.

Fig.3 Input-off voltage as a function of collector current; typical values.



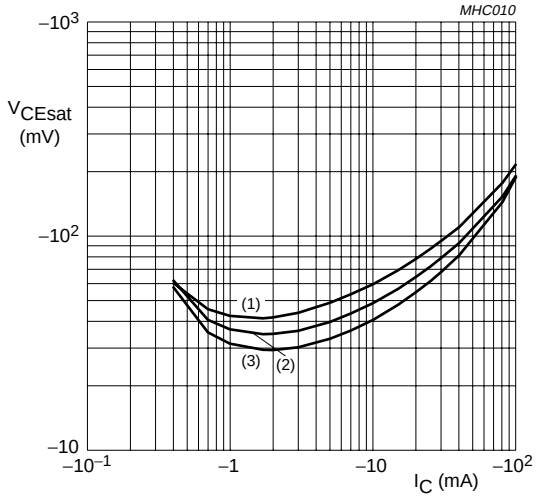
TR1 (NPN); V_{CE} = 0.3 V.
(1) T_{amb} = –40 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = 100 °C.

Fig.4 Input-on voltage as a function of collector current; typical values.



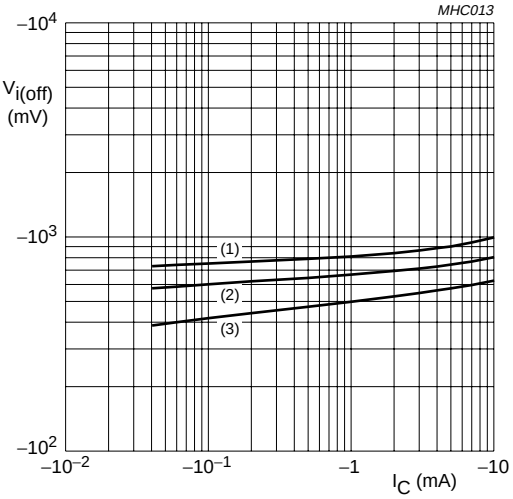
TR2 (PNP); V_{CE} = −5 V.
(1) T_{amb} = 150 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = −40 °C.

Fig.5 DC current gain as a function of collector current; typical values.



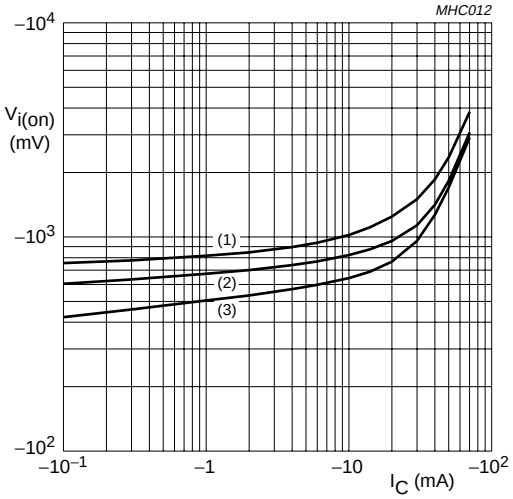
TR2 (PNP); I_C/I_B = 20.
(1) T_{amb} = 100 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = −40 °C.

Fig.6 Collector-emitter saturation voltage as a function of collector current; typical values.



TR2 (PNP); V_{CE} = −5 V.
(1) T_{amb} = −40 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = 100 °C.

Fig.7 Input-off voltage as a function of collector current; typical values.

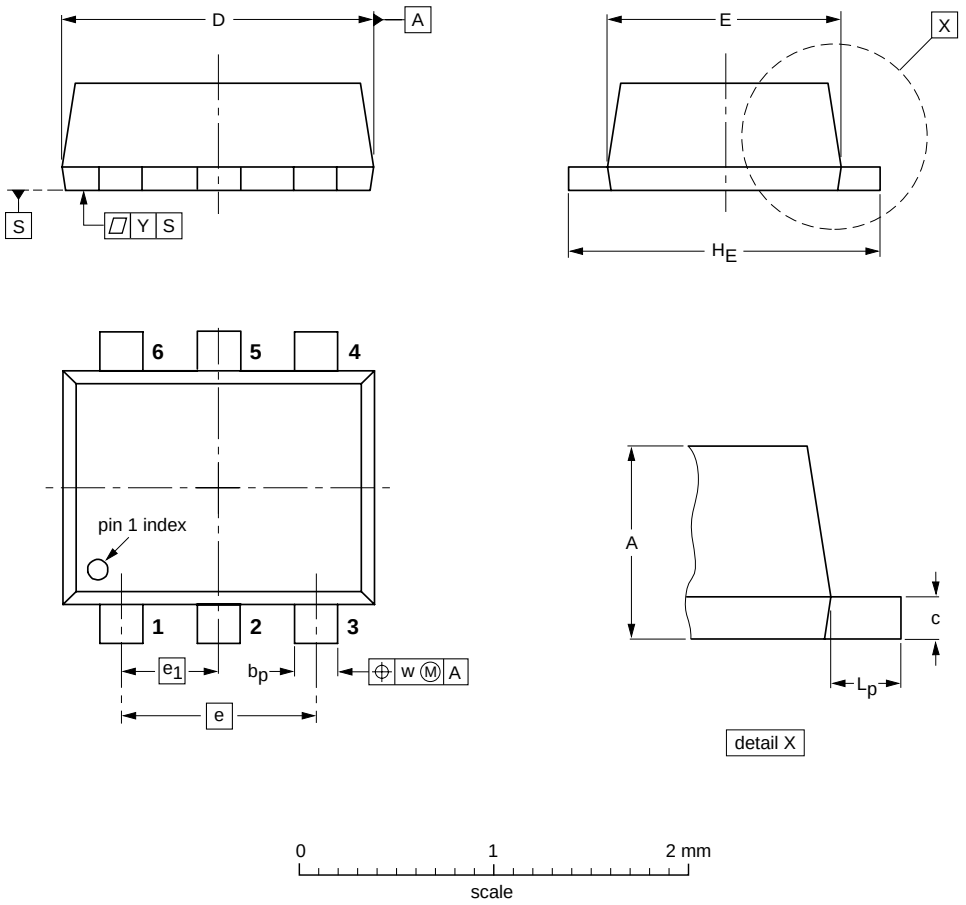


TR2 (PNP); V_{CE} = −0.3 V.
(1) T_{amb} = −40 °C.
(2) T_{amb} = 25 °C.
(3) T_{amb} = 100 °C.

Fig.8 Input-on voltage as a function of collector current; typical values.

PACKAGE OUTLINES

Plastic surface mounted package; 6 leads **SOT666**

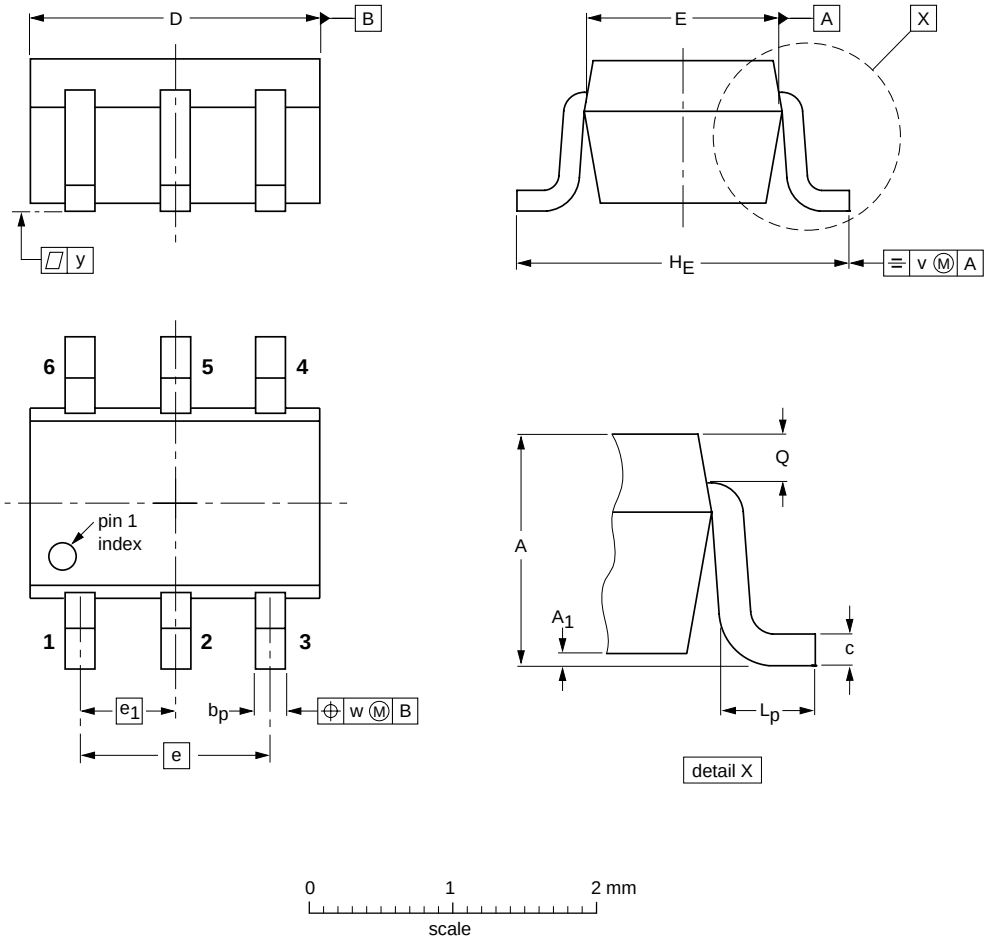


DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						~~01-01-04~~ 01-08-27

Plastic surface mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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