50 MHz–1000 MHz Quadrature Demodulator

AD8348

FEATURES

Integrated I/Q demodulator with IF VGA amplifier
Operating IF frequency 50 MHz to 1000 MHz
(3 dB IF BW of 500 MHz driven from R_S = 200 Ω)
Demodulation bandwidth 75 MHz
Linear-in-dB AGC range 44 dB
Third order intercept
IIP3 +28 dBm @ min gain (F_{IF} = 380 MHz)
IIP3 –8 dBm @ max gain (F_{IF} = 380 MHz)
Quadrature demodulation accuracy
Phase accuracy 0.5°
Amplitude balance 0.25 dB
Noise figure 11 dB @ max gain (F_{IF} = 380 MHz)
LO input –10 dBm
Single supply 2.7 V to 5.5 V
Power-down mode
Compact 28-lead TSSOP package

APPLICATIONS

QAM/QPSK demodulator
W-CDMA/CDMA/GSM/NADC
Wireless local loop
LMDS

PRODUCT OVERVIEW

The AD8348 is a broadband quadrature demodulator with an integrated intermediate frequency (IF), variable gain amplifier (VGA), and integrated baseband amplifiers. It is suitable for use in communications receivers, performing quadrature demodulation from IF directly to baseband frequencies. The baseband amplifiers have been designed to directly interface with dual-channel ADCs, such as the AD9201, AD9283, and AD9218, for digitizing and postprocessing.

The IF input signal is fed into two Gilbert cell mixers through an X-AMP® VGA. The IF VGA provides 44 dB of gain control. A precision gain control circuit sets a linear-in-dB gain characteristic for the VGA and provides temperature compensation. The LO quadrature phase splitter employs a divide-by-two frequency divider to achieve high quadrature accuracy and amplitude balance over the entire operating frequency range.

FUNCTIONAL BLOCK DIAGRAM

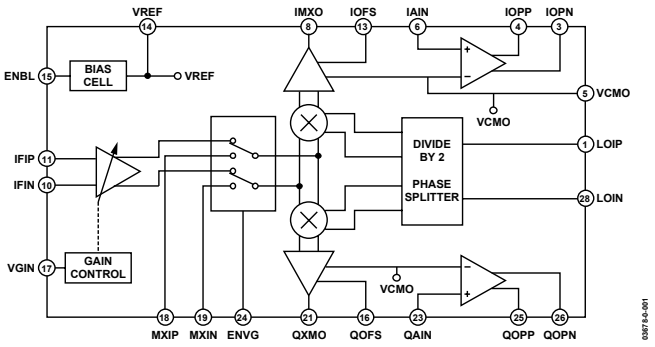

Figure 1.

Optionally, the IF VGA can be disabled and bypassed. In this mode, the IF signal is applied directly to the quadrature mixer inputs via the MXIP and MXIN pins.

Separate I and Q channel baseband amplifiers follow the baseband outputs of the mixers. The voltage applied to the VCMO pin sets the dc common-mode voltage level at the baseband outputs. Typically VCMO is connected to the internal VREF voltage, but it can also be connected to an external voltage. This flexibility allows the user to maximize the input dynamic range to the ADC. Connecting a bypass capacitor at each offset compensation input (IOFS and QOFS) nulls dc offsets produced in the mixer. Offset compensation can be overridden by applying an external voltage at the offset compensation inputs.

The mixers' outputs are brought off-chip for optional filtering before final amplification. Inserting a channel selection filter before each baseband amplifier increases the baseband amplifiers' signal handling range by reducing the amplitude of high level, out-of-channel interferers before the baseband signal is fed into the I/Q baseband amplifiers. The single-ended mixer output is amplified and converted to a differential signal for driving ADCs.

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

SPECIFICATIONS

Table 1. V_S = 5 V, T_A = 25°C, F_{LO} = 380 MHz, F_{IF} = 381 MHz, P_{LO} = −10 dBm, R_S (LO) = 50 Ω, R_S (IFIP and MXIP/MXIN) = 200 Ω, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO Frequency Range	External Input = 2× LO Frequency	100		2000	MHz
IF Frequency Range		50		1000	MHz
Baseband Bandwidth			75		MHz
LO Input Level	50 Ω Source	−12	−10	0	dBm
V_{SUPPLY} (V_S)		2.7		5.5	V
Temperature Range		−40		+85	°C
IF FRONT END WITH VGA	IFIP to IMXO (QMXO)				
	ENVG = 5 V				
Input Impedance			200||1.1		Ω||pF
Gain Control Range			44		dB
Maximum Conversion Gain	VGIN = 0.2 V (Maximum Voltage Gain)		25.5		dB
Minimum Conversion Gain	VGIN = 1.2 V (Minimum Voltage Gain)		−18.5		dB
3 dB Bandwidth			500		MHz
Gain Control Linearity	VGIN = 0.4 V (+21 dB) to 1.1 V (−14 dB)		±0.5		dB
IF Gain Flatness	F_{IF} = 380 MHz ±5% (VGIN = 1.2 V)		0.1		dB p-p
	F_{IF} = 900 MHz ±5% (VGIN = 1.2 V)		1.3		dB p-p
Input P1dB	VGIN = 0.2 V (Maximum Gain)		−22		dBm
	VGIN = 1.2 V (Maximum Gain)		+13		dBm
Second Order Input Intercept (IIP2)	IF1 = 385 MHz, IF2 = 386 MHz				
	+3 dBm Each Tone from 200 Ω Source		65		dBm
	VGIN = 1.2 V (Minimum Gain)				
	−42 dBm Each Tone from 200 Ω Source		18		dBm
	VGIN = 0.2 V (Maximum Gain)				
Third Order Input Intercept (IIP3)	IF1 = 381 MHz, IF2 = 381.02 MHz				
	Each Tone 10 dB below P1dB from 200 Ω Source		28		dBm
	VGIN = 1.2 V (Minumum Gain)				
	Each Tone 10 dB Below P1dB from 200 Ω Source		−8		dBm
	VGIN = 0.2 V (Maximum Gain)				
LO Leakage	Measured at IFIP, IFIN		−80		dBm
	Measured at IMXO/QMXO (LO = 50 MHz)		−60		dBm
Demodulation Bandwidth	Small Signal 3 dB Bandwidth		75		MHz
Quadrature Phase Error	LO = 380 MHz (LOIP/LOIN 760 MHz)	−2	±0.5	+2	Degrees
I/Q Amplitude Imbalance			0.25		dB
Noise Figure	Maximum Gain, from 200 Ω Source, F_{IF} = 380 MHz		10.75		dB
Mixer Output Impedance			40		Ω
Capacitive Load	Shunt from IMXO, QMXO to VCMO	0		10	pF
Resistive Load	Shunt from IMXO, QMXO to VCMO	200	1.5 k		Ω
Mixer Peak Output Current			2.5		mA

Parameter	Condition	Min	Typ	Max	Unit
IF FRONT END WITHOUT VGA	From MXIP, MXIN to IMXO (QMXO)				
	ENVG = 0 V, IMXO/QMXO Load = 1.5 kΩ				
Input Impedance	Measured Differentially Across MXIP/MXIN		200||1.5		Ω||pF
Conversion Gain			10.5		dB
3 dB Output Bandwidth			75		MHz
IF Gain Flatness	F_{IF} = 380 MHZ ±5%		0.1		dB p-p
	F_{IF} = 900 MHZ ±5%		0.15		dB p-p
Input P1dB			–4		dBm
Third Order Input Intercept (IIP3)	IF1 = 381 MHz, IF2 = 381.02 MHz		14		dBm
	Each Tone 10 dB below P1dB from 200 Ω Source				
LO Leakage	Measured at MXIP/MXIN		–70		dBm
	Measured at IMXO, QMXO		–60		dBm
Demodulation Bandwidth	Small Signal 3 dB Bandwidth		75		MHz
Quadrature Phase Error	LO = 380 MHz (LOIP/LOIN 760 MHz, Single-Ended)	–2	±0.5	+2	Degrees
I/Q Amplitude Imbalance			0.25		dB
Noise Figure	From 200 Ω Source, F_{IF} = 380 MHz		21		dB
I/Q BASEBAND AMPLIFIER	From IAIN to IOPP/IOPN and QAIN to QOPP/QOPN, R_{LOAD} = 2 kΩ Single-Ended to Ground				
Gain			20		dB
Bandwidth	10 pF Differential Load		125		MHz
Output DC Offset (Differential)	LO Leakage Offset Corrected Using 500 pF Capacitor on IOFS, QOFS ($V_{IOPP} - V_{IOPN}$)	–50	±12	+50	mV
Output Common-Mode Offset	$(V_{IOPP} + V_{IOPN})/2$ – VCMO	–75	±35	+75	mV
Group Delay Flatness	0 MHz–50 MHz		3		ns p-p
Input Referred Noise Voltage	Frequency = 1MHz		8		nV/√Hz
Output Swing Limit (Upper)		V_S –1			V
Output Swing Limit (Lower)				0.5	V
Peak Output Current			1		mA
Input Impedance			50||1		kΩ||pF
Input Bias Current			2		µA
RESPONSE FROM IF AND MX INPUTS TO BASEBAND AMPLIFIER OUTPUT	IMXO and QMXO Connected Directly to IAIN and QAIN, Respectively				
Gain	From MXIP/MXIN		30.5		dB
	From IFIP/IFIN, VGIN = 0.2 V		45.5		dB
	From IFIP/IFIN, VGIN = 1.2 V		1.5		dB
CONTROL INPUT/OUTPUTS					
VCMO Input Range	V_S = 5 V	0.5	1	4	V
	V_S = 2.7 V	0.5	1	1.7	V
VREF Output Voltage		0.95	1	1.05	V
Gain Control Voltage Range	VGIN	0.2		1.2	V
Gain Slope		–55	–50	–45	dB/V
Gain Intercept	Linear Extrapolation Back to Theoretical Gain at VGIN = 0 V	55	61	67	dB
Gain Control Input Bias Current			1		µA
LO Inputs					
LOIP Input Return Loss	LOIN AC-Coupled to Ground (760 MHz Applied to LOIP)		–6		dB

Parameter	Condition	Min	Typ	Max	Unit
POWER-UP CONTROL					
ENBL Threshold Low	Low = Standby	0	$V_S/2$	1	V
ENBL Threshold High	High = Enable	$+V_S - 1$	$V_S/2$	$+V_S$	V
Input Bias Current			2		µA
Power-Up Time	Time for Final Baseband Amplifiers to Be within 90% of Final Amplitude		45		µs
Power-Down Time	Time for Supply Current to be <10% of Enabled Value.		700		ns
POWER SUPPLIES	VPOS1, VPOS2, VPOS3				
Voltage		2.7		5.5	V
Current (Enabled)	V_{POS} = 5 V	38	48	58	mA
Current (Standby)	V_{POS} = 5 V		75		µA

ABSOLUTE MAXIMUM RATINGS

Table 2. AD8348 Absolute Maximum Ratings

Parameter	Rating
Supply Voltage VPOS1, VPOS2, VPOS3	5.5 V
LO Input Power	10 dBm (re: 50 Ω)
IF Input Power	18 dBm (re: 200 Ω)
Internal Power Dissipation	450 mW
θ_{JA}	68°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

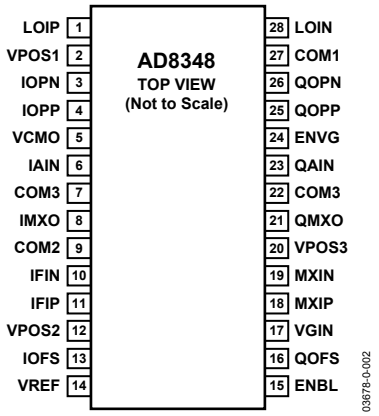

Figure 2. 28-Lead TSSOP

Table 3. Pin Function Descriptions—28-Lead TSSOP

Pin No.	Mnemonic	Description	Equivalent Circuit
1, 28	LOIP, LOIN	LO Input. For optimum performance, these inputs should be ac-coupled and driven differentially. Differential drive from single-ended sources can be achieved via a balun. To obtain a broadband 50 Ω input impedance, connect a 60.4 Ω shunt resistor between LOIP and LOIN. Typical input drive level is equal to −10 dBm.	A
2, 12, 20	VPOS1, VPOS2, VPOS3	Positive Supply for LO, IF, and Biasing and Baseband Sections, respectively. These pins should be decoupled with 0.1 µF and 100 pF capacitors.	
3, 4, 25, 26	IOPN, IOPP, QOPP, QOPN	I-Channel and Q-Channel Differential Baseband Outputs. Typical output swing is equal to 2 V p-p differential. The dc common-mode voltage level on these pins is set by the voltage on VCMO.	B
5	VCMO	Baseband DC Common-Mode Voltage. The voltage applied to this pin sets the dc common-mode levels for all the baseband outputs and inputs (IMXO, QMXO, IOPP, IOPN, QOPP, QOPN, IAIN, and QAIN). This pin can either be connected to VREF or to a reference voltage from another device (typically an ADC).	C
6, 23	IAIN, QAIN	I-Channel and Q-Channel Baseband Amplifier Input. The single-ended signals on these pins are referenced to VCMO and must have a dc bias equal to the dc voltage on the VCMO pin. If IMXO (QMXO) is dc-coupled to IAIN (QAIN), biasing will be provided by IMXO (QMXO). If an ac-coupled filter is placed between IMXO and IAIN, these pins can be biased from the source driving VCMO through a 1 kΩ resistor. The gain from IAIN/QAIN to the differential outputs (IOPP/IOPN and QOPP/QOPN) is 20 dB.	D
7, 22	COM3	Ground for Biasing and Baseband Sections.	
8, 21	IMXO, QMXO	I-Channel and Q-Channel Mixer Baseband Outputs. These are low impedance (40 Ω) outputs whose bias level is set by the voltage applied to the VCMO pin. These pins are typically connected to IAIN and QAIN, respectively, either directly or through a filter. Each output can drive a maximum current of 2.5 mA.	H
9	COM2	IF Section Ground.	
10, 11	IFIN, IFIP	IF Input. IFIN should be ac-coupled to ground. The single-ended IF input signal should be ac-coupled into IFIP. The nominal differential input impedance of these pins is 200 Ω. For a broadband 50 Ω input impedance, a minimum loss L pad should be used; R_{SERIES} = 174 Ω, R_{SHUNT} = 57.6 Ω. This will provide a 200 Ω source impedance to the IF input. However, the AD8348 does not necessarily require a 200 Ω source impedance, and a single shunt 66.7 Ω resistor may be placed between IFIP and IFIN.	E
13, 16	IOFS, QOFS	I-Channel and Q-Channel Offset Nulling Inputs. DC offsets on the I-channel mixer output (IMXO) can be nulled by connecting a 0.1 µF capacitor from IOFS to ground. Driving IOFS with a fixed voltage (typically a DAC calibrated such that the offset at IOPP/IOPN is nulled) can extend the operating frequency range to include dc. The QOFS pin can likewise be used to null offsets on the Q-channel mixer output (QMXO).	F

Pin No.	Mnemonic	Description	Equivalent Circuit
14	VREF	Reference Voltage Output. This output voltage (1 V) is the main bias level for the device and can be used to externally bias the inputs and outputs of the baseband amplifiers. The typical maximum drive current for this output is 2 mA.	G
15	ENBL	Chip Enable Input. Active high. Threshold is equal to $+V_S/2$.	D
17	VGIN	Gain Control Input. The voltage on this pin controls the gain on the IF VGA. The gain control voltage range is from 0.2 V to 1.2 V and corresponds to a conversion gain range from +25.5 dB to −18.5 dB. This is the gain to the output of the mixers (i.e., IMXO and QMXO). There is an additional 20 dB of fixed gain in the final baseband amplifiers (IAIN to IOPP/IOPN and QAIN to QOPP/QOPN). Note that the gain control function has a negative sense (i.e., increasing voltage decreases gain).	D
18, 19	MXIP, MXIN	Auxiliary Mixer Inputs. If ENVG is low, then the IFIP and IFIN inputs are disabled and MXIP and MXIN are enabled, allowing the VGA to be bypassed. These are fully differential inputs that should be ac-coupled to the signal source.	I
24	ENVG	Active High VGA Enable. When ENVG is high, IFIP and IFIN inputs are enabled and MXIP and MXIN inputs are disabled. When ENVG is low, MXIP and MXIN inputs are enabled and IFIP and IFIN inputs are disabled.	D
27	COM1	LO Section Ground.	

EQUIVALENT CIRCUITS

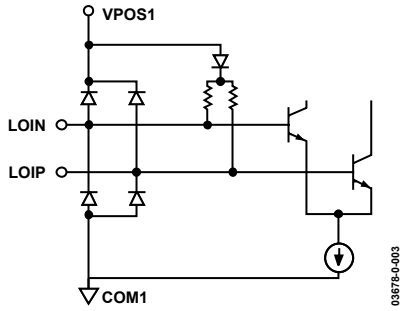

Figure 3. Circuit A

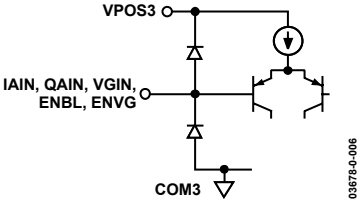

Figure 6. Circuit D

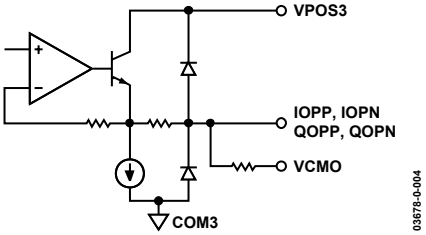

Figure 4. Circuit B

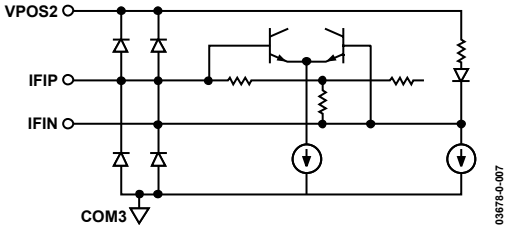

Figure 7. Circuit E

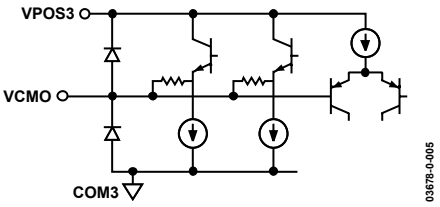

Figure 5. Circuit C

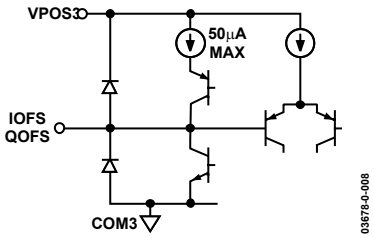

Figure 8. Circuit F

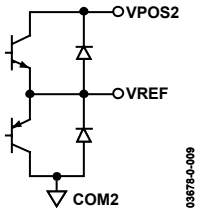

Figure 9. Circuit G

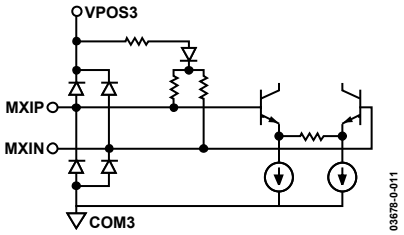

Figure 11. Circuit I

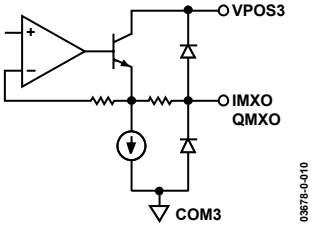

Figure 10. Circuit H

TYPICAL PERFORMANCE CHARACTERISTICS

VGA AND DEMODULATOR

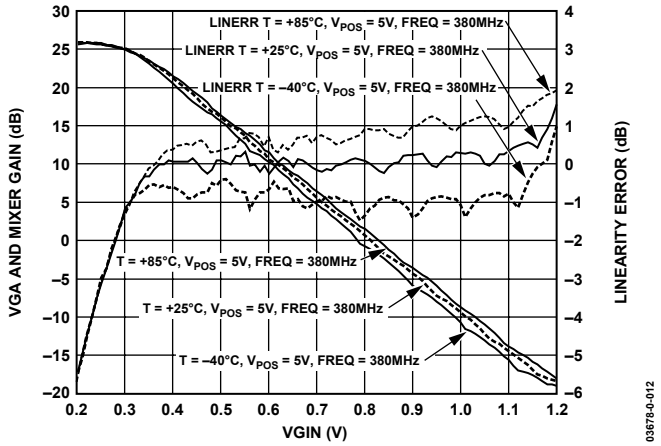

Figure 12.Mixer Gain and Linearity Error vs. VGIN, V_{POS} = 5 V, F_{IF} = 380 MHz, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

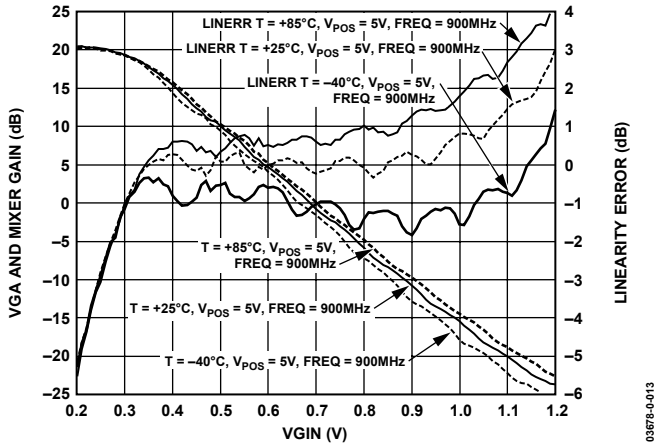

Figure 13. Mixer Gain and Linearity Error vs. VGIN, V_{POS} = 5 V, F_{IF} = 900 MHz, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

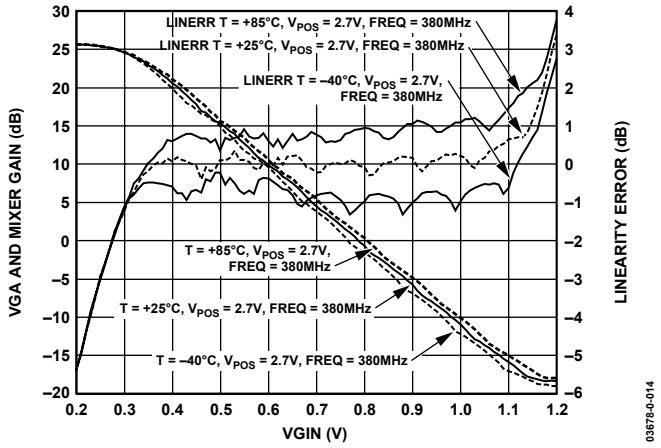

Figure 14. Mixer Gain and Linearity Error vs. VGIN, V_{POS} = 2.7 V, F_{IF} = 380 MHz, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

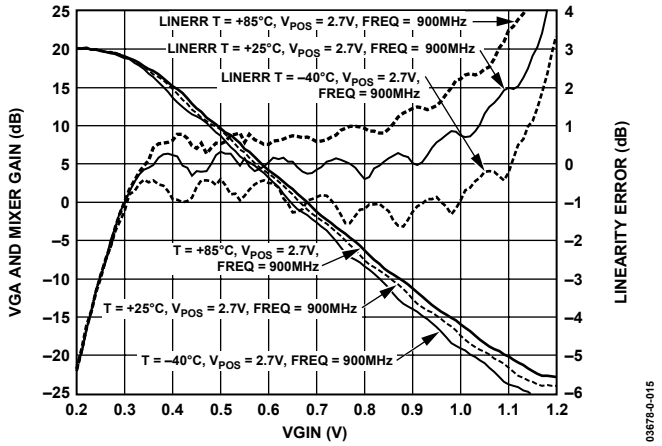

Figure 15. Mixer Gain and Linearity Error vs. VGIN, V_{POS} = 2.7 V, F_{IF} = 900 MHz, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

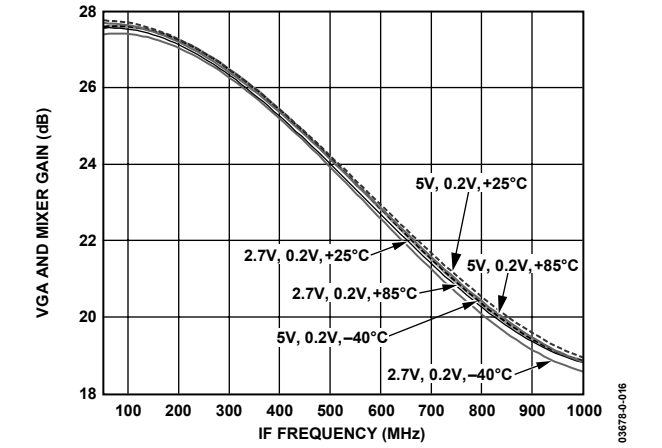

Figure 16. Gain vs. F_{IF}, VGIN = 0.2 V, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

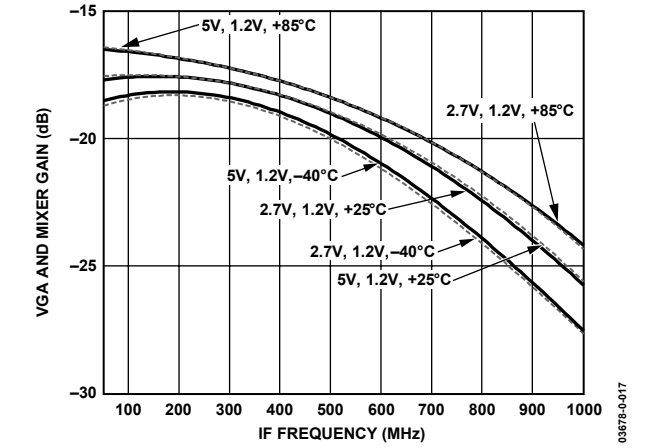

Figure 17. Gain vs. F_{IF}, VGIN = 1.2 V, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

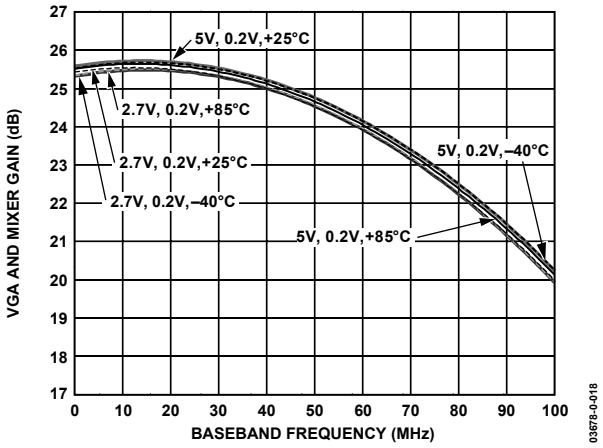

Figure 18. Gain vs. F_{BB}, VGIN = 0.2 V, F_{IF} = 380 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

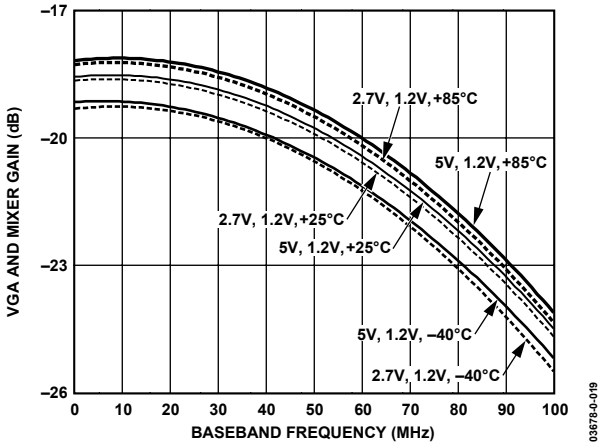

Figure 19. Gain vs. F_{BB}, VGIN = 1.2 V, F_{IF} = 380 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

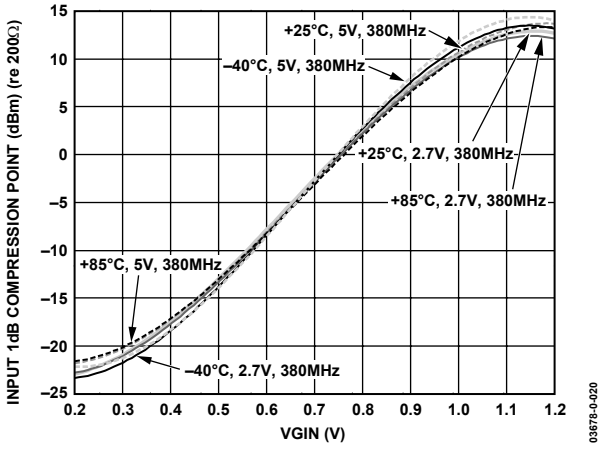

Figure 20. Input 1 dB Compression Point (IP1dB) vs. VGIN, F_{IF} = 380 MHz, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

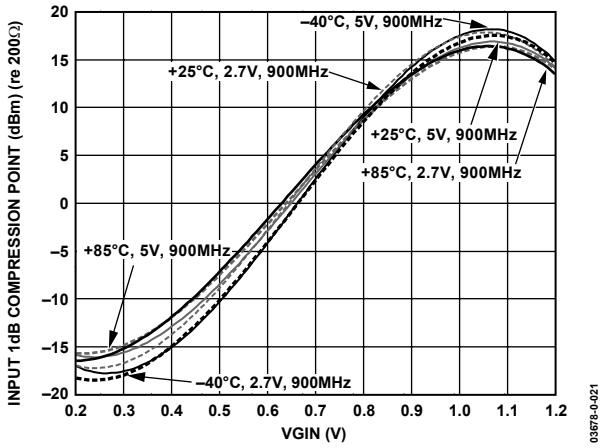

Figure 21. Input 1 dB Compression Point (IP1dB) vs. VGIN, F_{IF} = 900 MHz, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

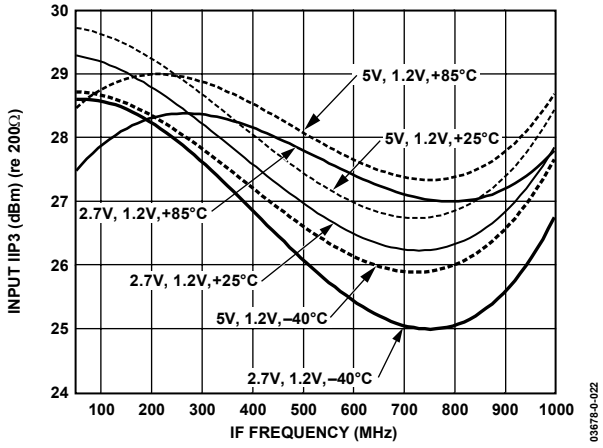

Figure 22. IIP3 vs. F_{IF}, VGIN = 1.2 V, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C, Tone Spacing = 20 kHz

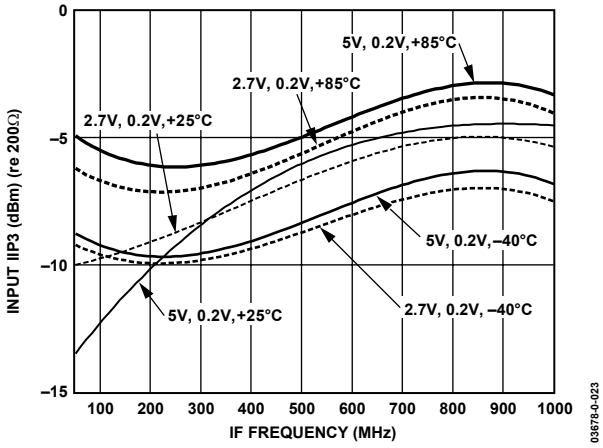

Figure 23. IIP3 vs. F_{IF}, VGIN = 0.2 V, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

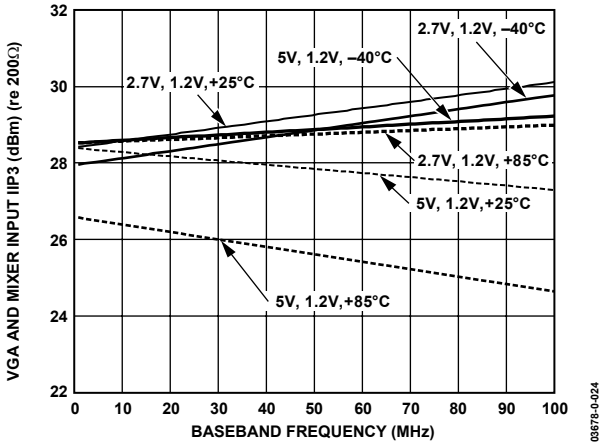

Figure 24. IIP3 vs. F_{BB}, VGIN = 1.2 V, F_{IF} = 380 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

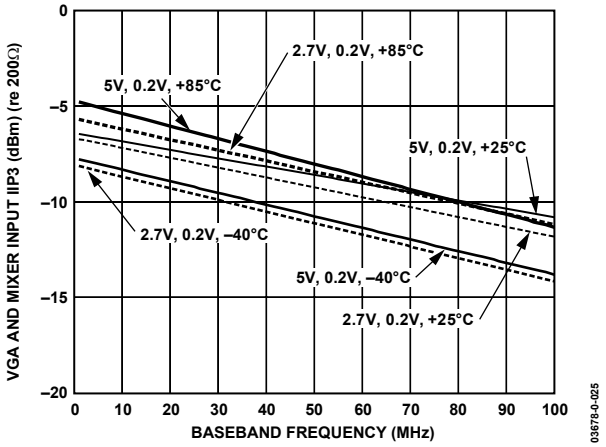

Figure 25. IIP3 vs. F_{BB}, VGIN = 0.2 V, F_{IF} = 380 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

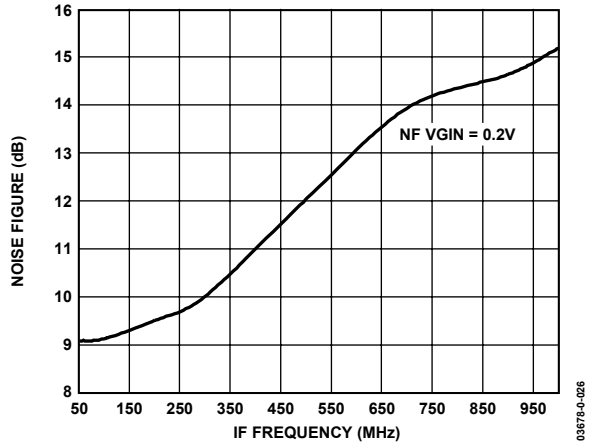

Figure 26. Noise Figure vs. F_{IF}, T = 25°C, VGIN = 0.2 V, F_{BB} = 1 MHz

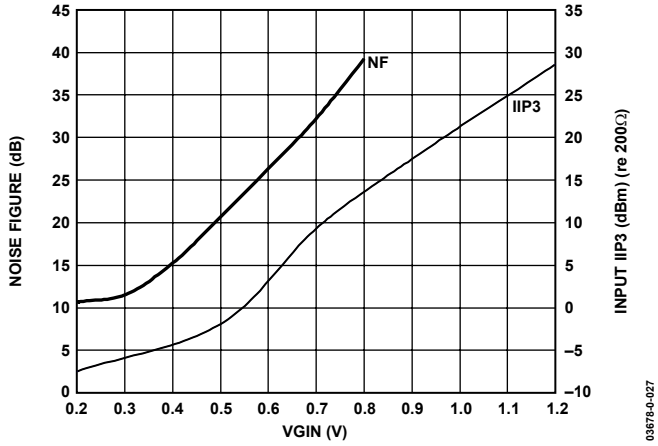

Figure 27. Noise Figure and IIP3 vs. VGIN, T = 25°C, F_{IF} = 380 MHz, F_{BB} = 1 MHz, V_{POS} = 2.7 V

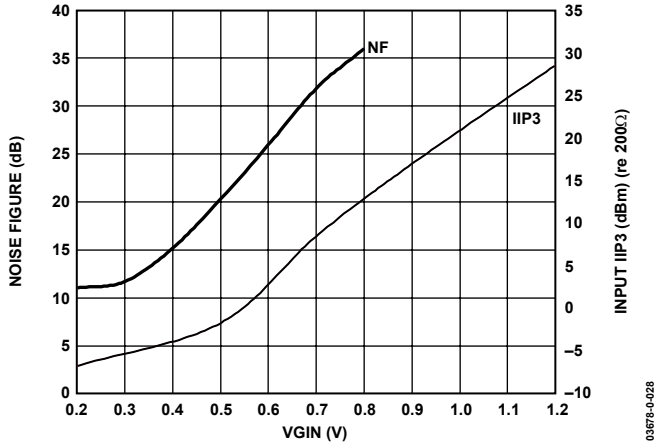

Figure 28. Noise Figure and IIP3 vs. VGIN, T = 25°C, F_{IF} = 380 MHz, F_{BB} = 1 MHz, V_{POS} = 5 V

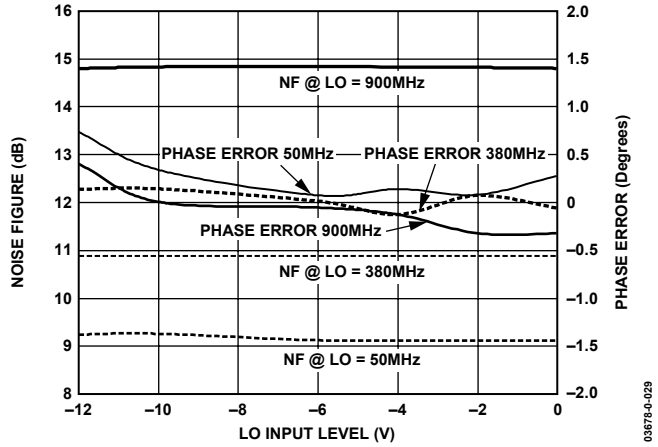

Figure 29. Noise Figure and Quadrature Phase Error IMXO-QMXO vs. LO Input Level, T = 25°C, VGIN = 0.2 V, V_{POS} = 5 V for F_{IF} = 50 MHz, 380 MHz, and 900 MHz

DEMODULATOR USING MXIP AND MXIN

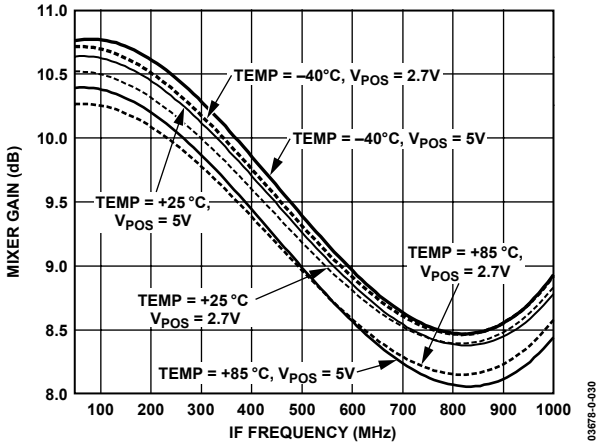

Figure 30. Mixer Gain vs. F_{IF}, V_{POS} = 2.7 V, 5 V, F_{BB} = 1 MHz, Temperature = –40°C, +25°C, +85°C

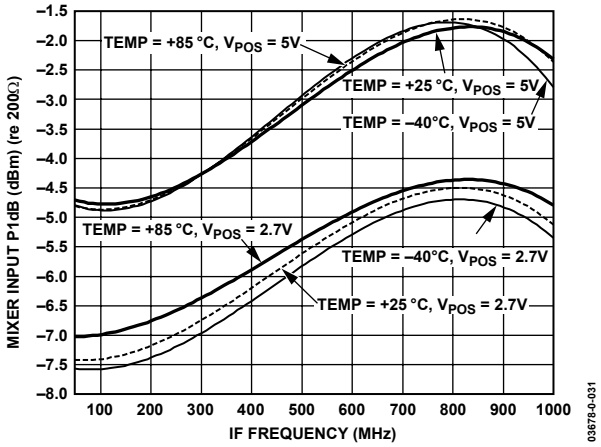

Figure 31. Input 1 dB Compression Point vs. F_{IF}, F_{BB} = 1 MHz, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

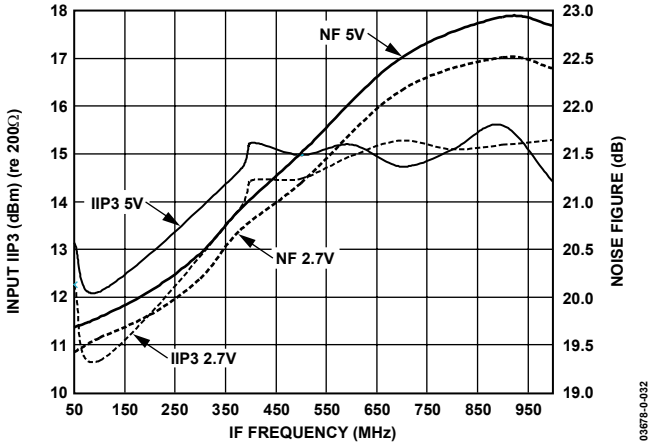

Figure 32. IIP3 and Noise Figure vs. F_{IF}, V_{POS} = 2.7 V, 5 V, Temperature 25°C

FINAL BASEBAND AMPLIFIERS

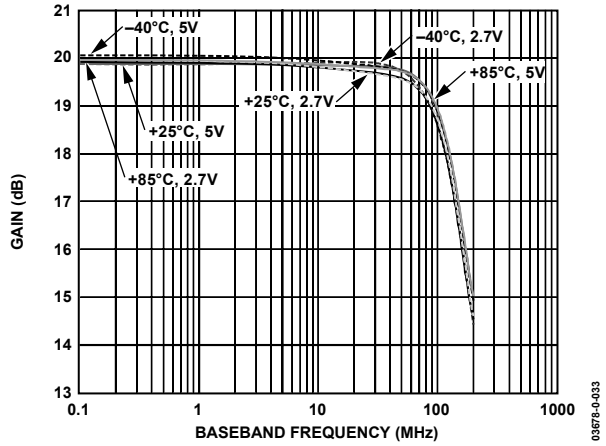

Figure 33. Gain vs. F_{BB}, V_{VCMO} = VREF = 1 V, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

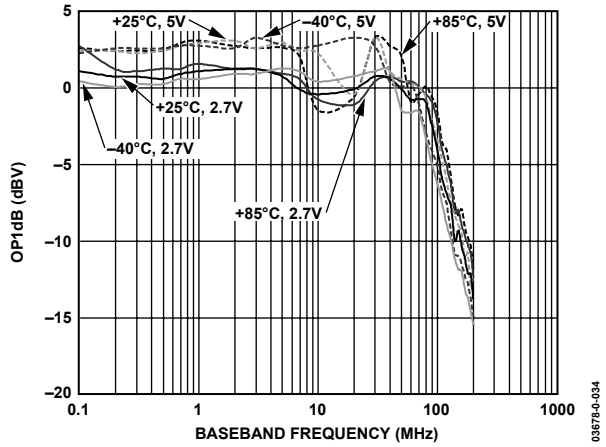

Figure 34. OPIdB Compression vs. F_{BB}, V_{VCMO} = VREF = 1 V, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

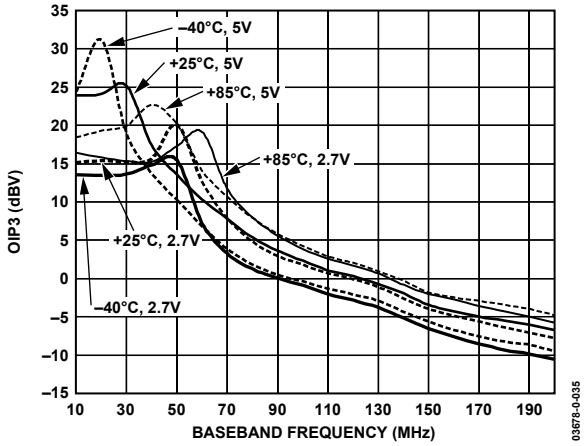

Figure 35. OPI3 vs. F_{BB}, V_{VCMO} = VREF = 1 V, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

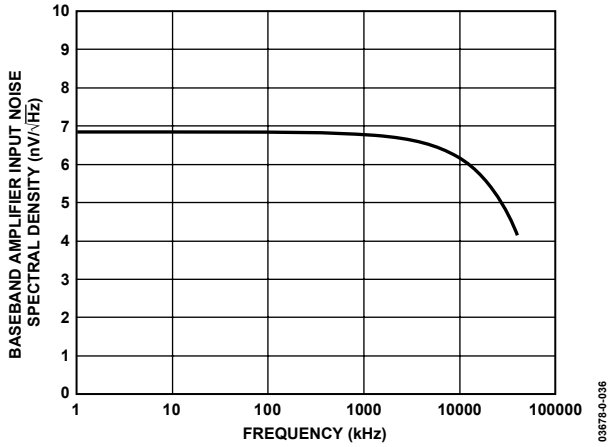

Figure 36. Noise Spectral Density

VGA/DEMODULATOR AND BASEBAND AMPLIFIER

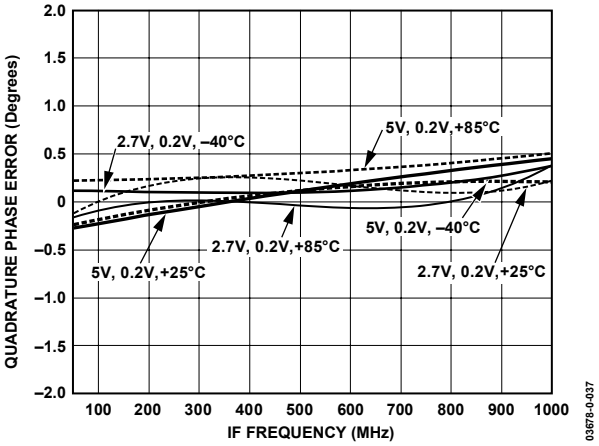

Figure 37. Quadrature Phase Error vs. F_{IF}, VGIN = 0.7 V, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C

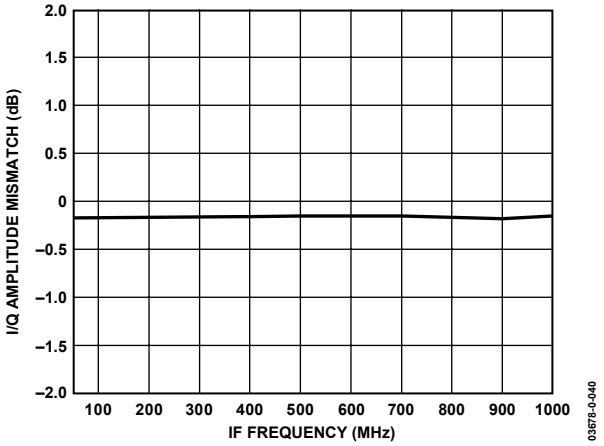

Figure 40. I/Q Amplitude Imbalance vs. F_{IF}, T = 25°C, V_{POS} = 5 V

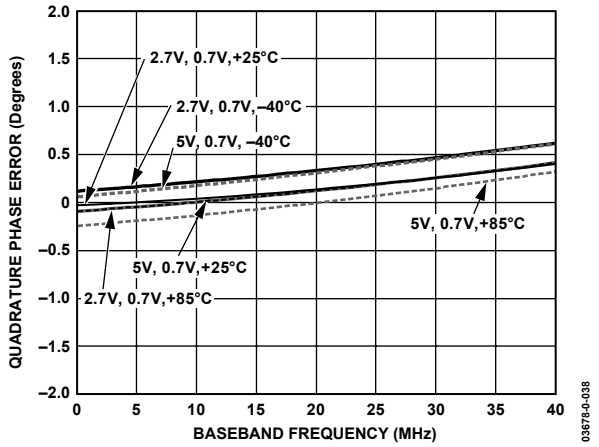

Figure 38. Quadrature Phase Error vs. F_{BB}, VGIN = 0.7 V, V_{POS} = 2.7 V, 5 V, Temperature = –40°C, +25°C, +85°C, F_{IF} = 380 MHz

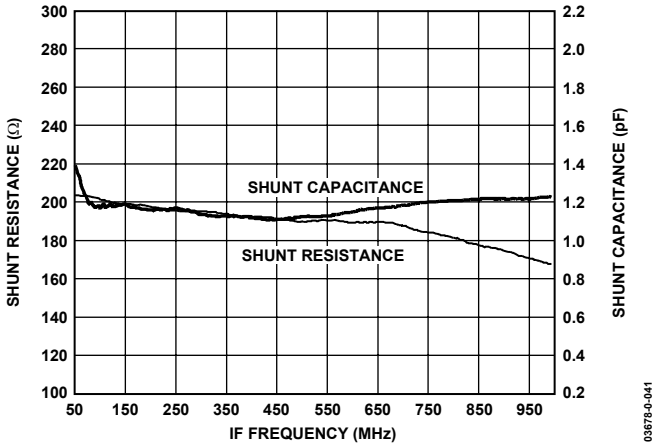

Figure 41. Input Impedance of IF Input vs. F_{IF}, VGIN = 0.7 V, V_{POS} = 5 V

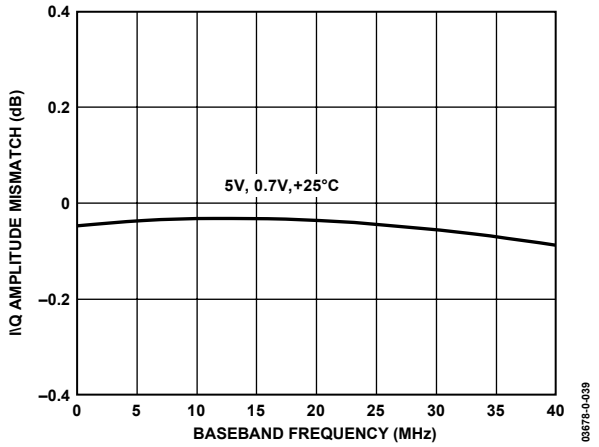

Figure 39. I/Q Amplitude Imbalance vs. F_{BB}, T = 25°C, V_{POS} = 5 V

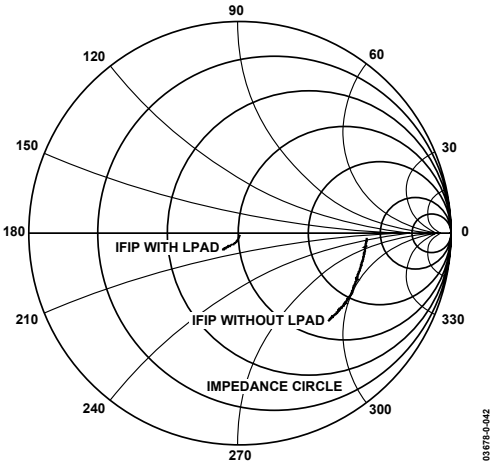

Figure 42. S11 of IF Input vs. F_{IF}, F_{IF} = 50 MHz to 1 GHz, VGIN = 0.7 V, V_{POS} = 5 V (with L Pad, with No Pad, Normalized to 50 Ω)

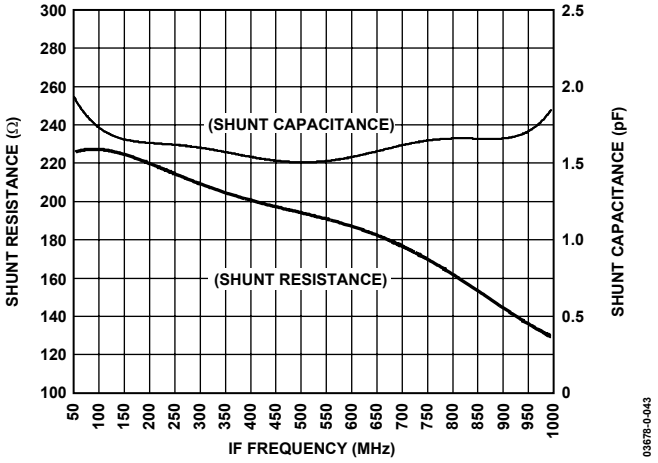

Figure 43. Input Impedance of Mixer Input vs. F_{IF}, VGIN = 0.7 V, V_{POS} = 5 V

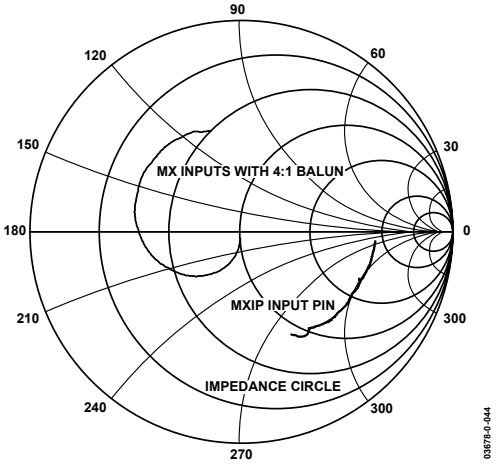

Figure 44. S11 of Mixer Input vs. F_{IF}, F_{IF} = 50 MHz to 1 GHz, VGIN = 0.7 V, V_{POS} = 5 V (With and Without Balun)

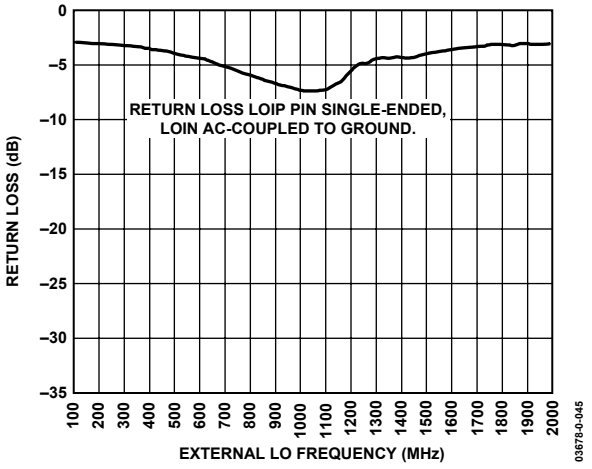

Figure 45.Return Loss of LOIP Input vs. External LO Frequency

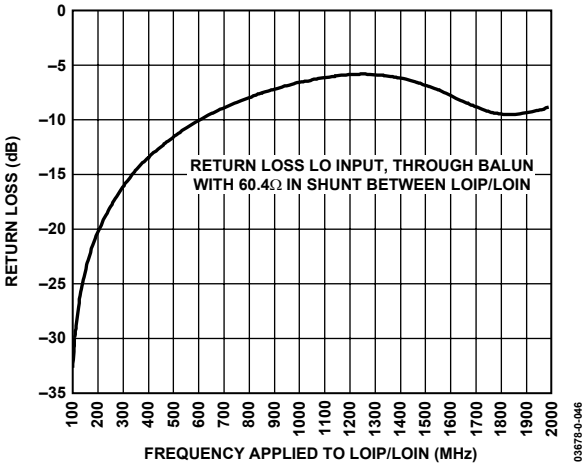

Figure 46. Return Loss of LO Input vs. External LO Frequency Through Balun, with Termination Resistor

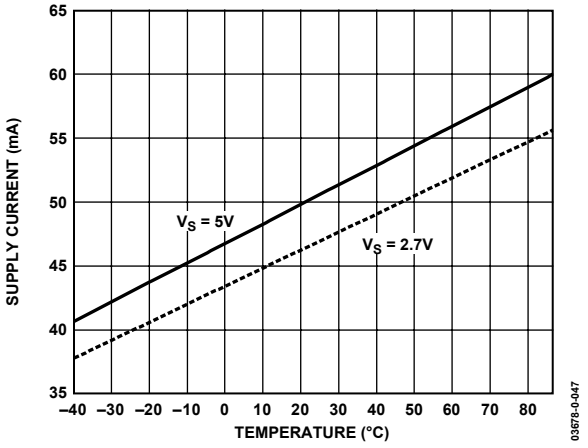

Figure 47.Supply Current vs. Temperature

THEORY OF OPERATION

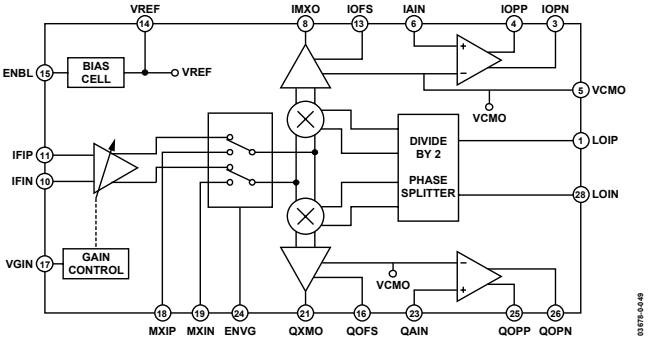

Figure 48. Functional Block Diagram

VGA

The VGA is implemented using the patented X-AMP architecture. The single-ended IF signal is attenuated in eight discrete 6 dB steps by a passive R-2R ladder. Each discrete attenuated version of the IF signal is applied to the input of a transconductance stage. The current outputs of all transconductance stages are summed together and drive a resistive load at the output of the VGA. Gain control is achieved by smoothly turning on and off the relevant transconductance stages with a temperature compensated interpolation circuit. This scheme allows the gain to continuously vary over a 44 dB range with linear-in-dB gain control. This configuration also keeps the relative dynamic range constant (e.g., IIP3 – NF in dB) over gain setting. The absolute intermodulation intercepts and noise figure, however, vary directly with gain. The analog voltage VGIN sets the gain. VGIN = 0.2 V is the maximum gain setting, and VGIN = 1.2 V is the minimum voltage gain setting.

DOWNCONVERSION MIXERS

The output of the VGA drives two (I and Q) double-balanced Gilbert cell downconversion mixers. Alternatively, driving the ENVG pin low can disable the VGA and the mixers can be externally driven directly via the MXIP and MXIN port. At the input of the mixer, a degenerated differential pair performs linear voltage-to-current conversion. The differential output current feeds into the mixer core where it is downconverted by the mixing action of the Gilbert cell. The phase splitter provides quadrature LO signals that drive the LO ports of the in-phase and quadrature mixers.

Buffers at the output of each mixer drive the IMXO and QMXO pins. These linear, low output impedance buffers drive 40 Ω temperature-stable, passive resistors in series with each of the output pins (IMXO and QMXO). This 40 Ω should be considered when calculating the reverse termination if an external filter is inserted between IMXO (QMXO) and IAIN (QAIN). The VCMO pin sets the dc output level of the buffer. This can be set externally or connected to the on-chip 1.0 V reference VREF.

PHASE SPLITTER

Quadrature generation is achieved using a divide-by-two frequency divider. Unlike a polyphase filter that achieves quadrature over a limited frequency range, the divide-by-two approach maintains quadrature over a broad frequency range and does not attenuate the LO. The user, however, must provide an external signal XLO that is twice the frequency of the desired LO frequency. XLO drives the clock inputs of two flip-flops that divide down the frequency by a factor of two. The outputs of the two flip-flops are one half period of XLO out of phase. Equivalently, the outputs are one-quarter period (90°) of the desired LO frequency out of phase. Because the transitions on XLO define the phase difference at the outputs, deviation from 50% duty cycle translates directly to quadrature phase errors.

If the user generates *XLO* from a 1× frequency (f_{REF}) and a frequency doubling circuit ($XLO = 2 \times f_{REF}$), fundamentally there is a 180° phase uncertainty between f_{REF} and the AD8348 internal quadrature LO. The phase relationship between I and Q LO, however, will always be 90°.

I/Q BASEBAND AMPLIFIERS

Two (I and Q) fixed gain (20 dB), single-ended-to-differential amplifiers are provided to amplify the demodulated signal after off-chip filtering. The amplifiers use voltage feedback to linearize the gain over the demodulation bandwidth. These amplifiers can be used to maximize the dynamic range at the input of an ADC following the AD8348.

The input to the baseband amplifiers IAIN (QAIN) feeds into the base of a bipolar transistor with an input impedance of roughly 50 kΩ. The baseband amplifiers sense the single-ended difference between IAIN (QAIN) and VCMO. IAIN (QAIN) can be dc biased by terminating with a shunt resistor to VCMO, such as when an external filter is inserted between IMXO (QMXO) and IAIN (QAIN). Alternatively, any dc connection to IMXO (QXMO) can provide appropriate bias via the offset-nulling loop.

ENABLE

A master biasing cell that can be disabled using the ENBL pin controls the biasing for the chip. If the ENBL pin is held low, the entire chip will power down to a low power sleep mode, typically consuming 75 μA at 5 V.

BASEBAND OFFSET CANCELLATION

A low output current integrator senses the output voltage offset at IOPP, IOPN (QOPP, QOPN) and injects a nulling current into the signal path. The integration time constant of the offset nulling loop is set by capacitor COFS from IOFS (QOFS) to

VCMO. This forms a high-pass response for the baseband signal path with a lower 3 dB frequency of

$$f_{PASS} = \frac{1}{2\pi \times 2650\ \Omega \times COFS}$$

Alternatively, the user can externally adjust the dc offset by driving IOFS (QOFS) with a digital-to-analog converter or other voltage source. In this case, the baseband circuit will operate all the way down to dc (f_{PASS} = 0 Hz). The integrator output current is only 50 μA and can be easily overridden with an external voltage source. The nominal voltage level applied to IOFS (QOFS) to produce a 0 V differential offset at the baseband outputs is 900 mV.

The IOFS (QOFS) pin must be connected to either a bypass capacitor (>0.1 μF) or an external voltage source to prevent the feedback loop from oscillating.

The feedback loop will be broken at dc if an ac-coupled baseband filter is placed between the mixer outputs and the baseband amplifier inputs. If an ac-coupled filter is implemented, the user must handle the offset compensation via some external means.

APPLICATIONS

BASIC CONNECTIONS

Figure 49 shows the basic connections schematic for the AD8348.

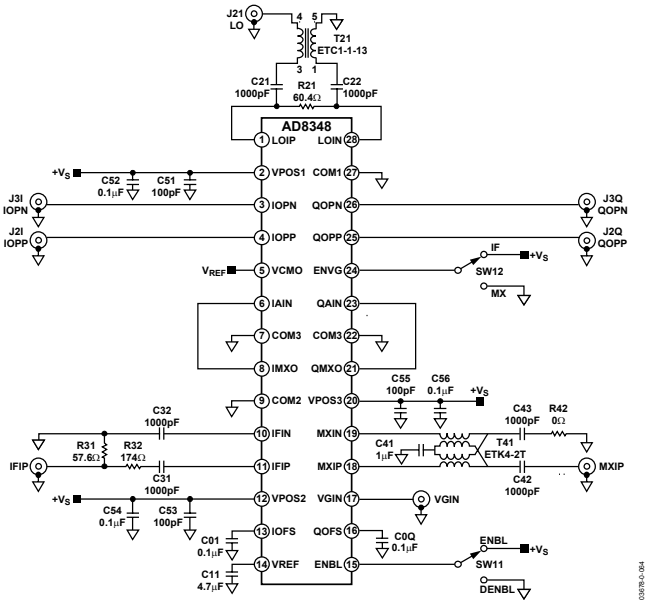

Figure 49. Basic Connections Schematic

POWER SUPPLY

The voltage supply for the AD8348, between 2.7 V and 5 V, should be provided to the +VPOSx pins and ground should be connected to the COMx pins. Each of the supply pins should be decoupled separately using two capacitors whose recommended values are 100 pF and 0.1 μF (values close to these may also be used).

DEVICE ENABLE

To enable the device, the ENBL pin should be driven to $+V_S$. Grounding the ENBL pin will disable the device.

VGA ENABLE

Driving the voltage on the ENVG pin to $+V_S$ enables the VGA. In this mode, the MX inputs are disabled and the IF inputs are used. Grounding the ENVG pin will disable the VGA and the IF inputs. When the VGA is disabled, the MX inputs should be used.

GAIN CONTROL

When the VGA is enabled, the voltage applied to the VGIN pin sets the gain. The gain control voltage range is between 0.2 V and 1.2 V. This corresponds to a gain range between +25.5 dB and –18.5 dB.

LO INPUT

For optimum performance, the local oscillator port should be driven differentially through a balun. The recommended balun is M/A-COM ETC1-1-13. The LO inputs to the device should be ac-coupled, unless an ac-coupled transformer is being used. For a broadband match to a 50 Ω source, a 60.4 Ω resistor should be placed between the LOIP and LION pins.

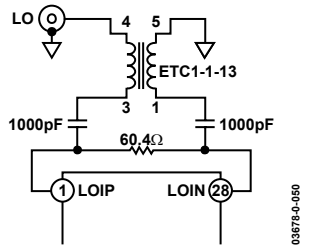

Figure 50. Differential LO Drive with Balun

Alternatively, the LO port can be driven single-ended without a balun (Figure 51). The LO signal is ac-coupled directly into the LOIP pin via an ac coupling capacitor and the LOIN pin is ac-coupled to ground. Driving the LO port single-ended will result in an increase in both quadrature phase error and LO leakage.

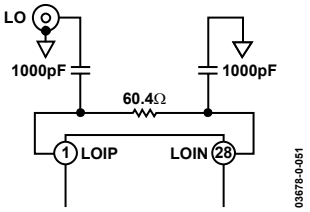

Figure 51. Single-Ended LO Drive.

The recommended LO drive level is between –12 dBm and 0 dBm. The LO frequency at the input to the device should be twice that of the desired LO frequency at the mixer core. The applied LO frequency range is between 100 MHz and 2 GHz.

IF INPUT

The IF inputs have an input impedance of 200 Ω. A broadband 50 Ω match can be achieved via the use of a minimum loss L Pad. Figure 42 shows the S11 of the IF input with and without the L Pad.

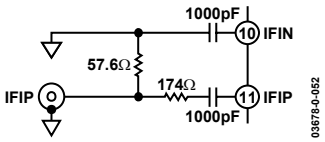

Figure 52. Minimum Loss L Pad for 50 Ω IF Input

MX INPUT

The mixer inputs MXIP and MXIN have a nominal impedance of 200 Ω and should be driven differentially. When driven from a differential source, the input should be ac-coupled to the source via capacitors, as shown in Figure 53.

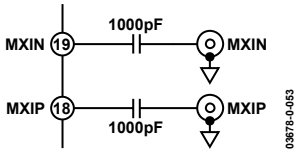

Figure 53. Differential Drive of MX Inputs

If the MX inputs are to be driven from a single-ended 50 Ω source, a 4:1 balun can be used to transform the 200 Ω impedance of the inputs to 50 Ω while performing the required single-ended-to-differential conversion. The recommended transformer is the M/A-COM ETK4-2T.

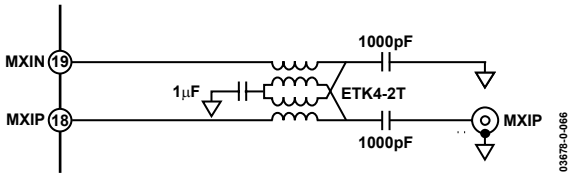

Figure 54. Driving the MX Inputs from a Single-Ended 50 Ω Source

BASEBAND OUTPUTS

The baseband amplifier outputs IOPP, IOPN, QOPP, and QOPN should be presented with loads of at least 2 kΩ (single-ended to ground). They are not designed to drive 50 Ω loads directly. The typical swing for these outputs is 2 V p-p differential (1 V p-p single-ended), but larger swings are possible as long as care is taken to ensure that the signals remain within the limits of the output swing (V_S – 1 V and 0.5 V). To achieve a larger swing, it is necessary to adjust the common-mode bias of the baseband output signals. Increasing the swing can have the benefit of improving the signal-to-noise ratio of the baseband amplifier output.

When connecting the baseband outputs to other devices, care should be taken to ensure that the outputs are not heavily capacitively loaded (approximately 20 pF and above). Doing so could potentially overload the output or induce oscillations. The effect of capacitive loading on the baseband amplifier outputs can be mitigated by inserting series resistors (approximately 200 Ω).

OUTPUT DC BIAS LEVEL

The dc bias of the mixer outputs and the baseband amplifier inputs and outputs is determined by the voltage that is driven onto the VCMO pin. The range of this voltage is typically between 500 mV and 4 V when operating with a 5 V supply.

To achieve maximum voltage swing from the baseband amplifiers, VCMO should be driven at 2.25 V; this will allow for a swing of up to 7 V p-p differential (3.5 V p-p single-ended).

INTERFACING TO DETECTOR FOR AGC OPERATION

The AD8348 can be interfaced with a detector such as the AD8362 rms-to-dc converter to provide an automatic signal leveling function for the baseband outputs.

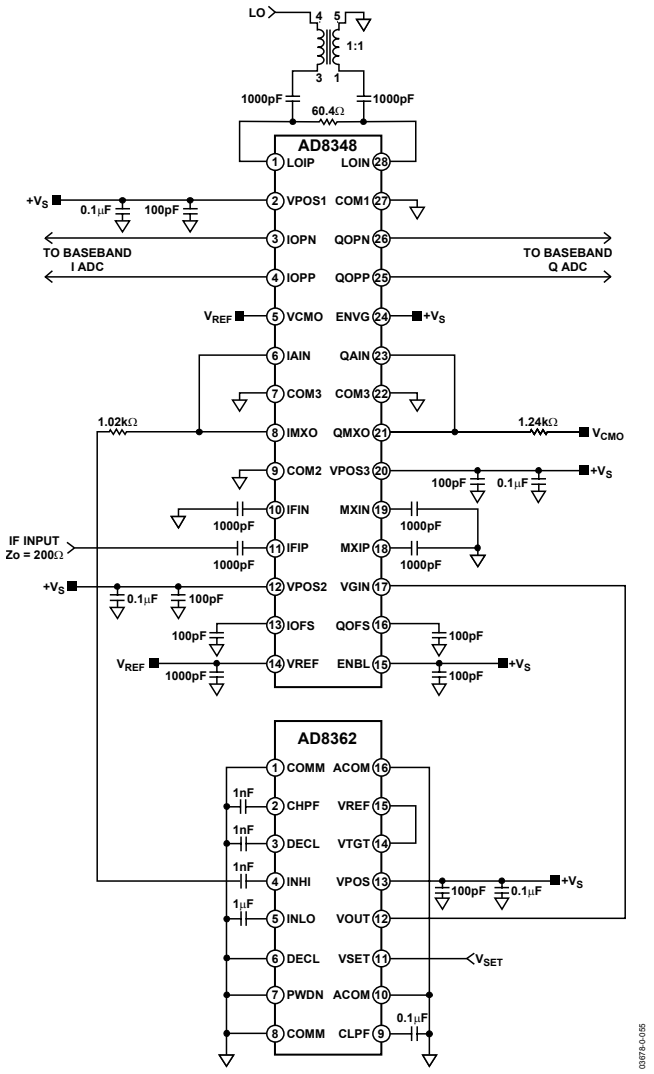

Figure 55. AD8362 Configuration for AGC Operation

Assuming the I and Q channels have the same rms power, the mixer output (or the output of the baseband filter) of one channel can be used as the input of the AD8362. The AD8362 should be operated in a region where its linearity error is small. Also, a voltage divider should be implemented with an external resistor in series with the 200 Ω input impedance of the AD8362's input. This will attenuate the AD8348's mixer output so that the AD8362's input is not overdriven. The size of the resistor between the mixer output and the AD8362 input should be chosen so that the peak signal level at the input of the AD8362 is about 10 dB down from the top of the AD8362's dynamic range, which occurs at approximately 10 dBm.

The other side of the AD8348's baseband output should be loaded with a resistance equal to the series resistance of the attenuating resistor in series with the AD8362's 200 Ω input impedance. This resistor should be tied to the source driving VCMO so that there is no dc current drawn from the mixer output.

The level of the mixer output (or the output of the baseband filter) can then be set by varying the setpoint voltage fed to Pin 11 (VSET) of the AD8362.

Care should be taken to ensure that blockers (unwanted signals in the band of interest that get demodulated together with the desired signal) do not dominate the rms power of the AD8362's input. This will cause an undesired reduction in the level of the mixer output. To overcome this, baseband filtering can be implemented to filter out the undesired signals. The signal to the AD8362 should then be taken after the filter.

Figure 56 shows the effectiveness of the AGC loop in maintaining a baseband amplifier output amplitude with less than 0.5 dB of amplitude error over an IF input range of 40 dB while demodulating a QPSK modulated signal at 380 MHz. The AD8362 has the benefit of being insensitive to crest factor variations and as such will provide similar performance regardless of the modulation of the incoming signal.

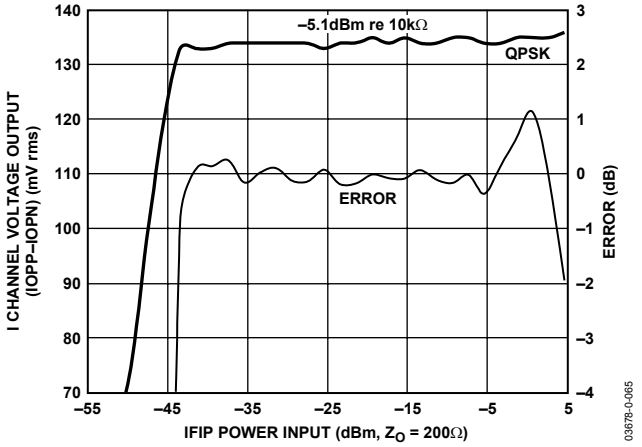

Figure 56. AD8348 Baseband Amplifier Output vs. IF Input Power with AD8362 AGC Loop

BASEBAND FILTERS

Baseband low-pass or band-pass filtering can be conveniently performed between the mixer outputs (IMXO/QMXO) and the input to the baseband amplifiers. Consideration should be given to the output impedance of the mixers (40 Ω).

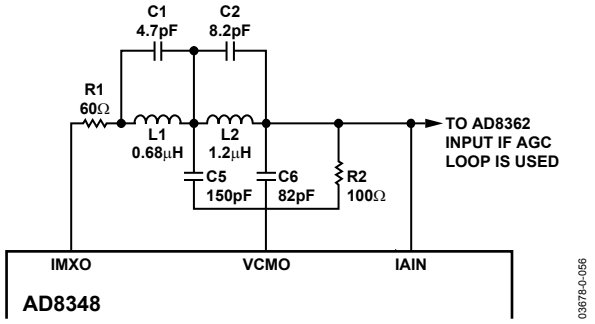

Figure 57. Baseband Filter Schematic

Figure 57 shows the schematic for a 100 Ω, fourth order elliptic low-pass filter with a 3 dB cutoff frequency of 20 MHz. Source and load impedances of approximately 100 Ω ensure that the filter sees a matched source and load. This also ensures that the mixer output is driving an overall load of 200 Ω. Note that the shunt termination resistor is tied to the source driving VCMO and not to ground. This ensures that the input to the baseband amplifier is biased to the proper reference level. VCMO is not an output pin and must be biased by a low impedance source.

The frequency response and group delay of this filter are shown in Figure 58 and Figure 59.

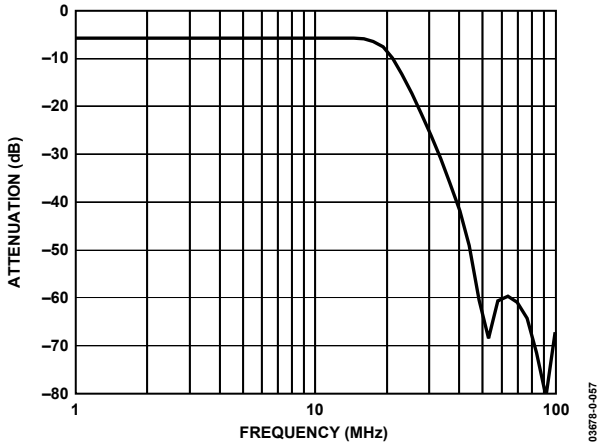

Figure 58. Baseband Filter Response

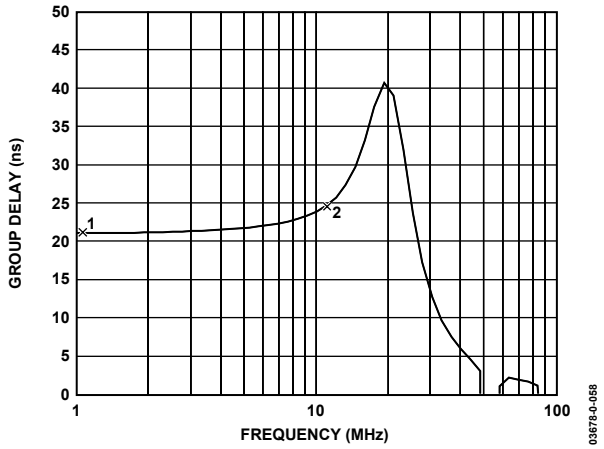

Figure 59. Baseband Filter Group Delay

LO GENERATION

Analog Devices has a line of PLLs that can be used for generating the LO signal. Table 4 lists the PLLs together with their maximum frequency and phase noise performance.

Table 4. ADI PLL Selection Table

ADI Model	Frequency F_{IN} (MHz)	@ 1 KHz ΦN dBc/Hz, 200 kHz PFD
ADF4001BRU	165	–99
ADF4001BCP	165	–99
ADF4110BRU	550	–91
ADF4110BCP	550	–91
ADF4111BRU	1200	–78
ADF4111BCP	1200	–78
ADF4112BRU	3000	–86
ADF4112BCP	3000	–86
ADF4116BRU	550	–89
ADF4117BRU	1200	–87
ADF4118BRU	3000	–90

ADI also offers the ADF4360 fully integrated synthesizer and VCO on a single chip that offers differential outputs for driving the local oscillator input of the AD8348. This means that the user can eliminate the use of the balun necessary for the single-ended-to-differential conversion. The ADF4360 comes as a family of chips with six operating frequency ranges. One can be chosen depending on the local oscillator frequency required. Table 5 below shows the options available.

Table 5. ADF4360 Family Operating Frequencies

ADI Model	Output Frequency Range (MHz)
ADF4360-1	2150/2450
ADF4360-2	1800/2150
ADF4360-3	1550/1950
ADF4360-4	1400/1800
ADF4360-5	1150/1400
ADF4360-6	1000/1250
ADF4360-7	Lower frequencies set by external L

EVALUATION BOARD

Figure 60 shows the schematic for the AD8348 evaluation board. Note that uninstalled components are indicated with the OPEN designation. The board is powered by a single supply in the range of 2.7 V to 5.5 V. Table 6 details the various configuration options of the evaluation board. Table 7 shows the various jumper configurations for operating the evaluation board with different signal paths.

Power to operate the board can be fed to a single $+V_S$ test point located near the LO input port at the top of the evaluation board. A GND test point is conveniently provided next to the $+V_S$ test point for the return path.

The device is enabled by moving Switch SW11 (at the bottom left of the evaluation board) to the ENBL position. The device is disabled by moving SW11 to the DENBL position. If desired, the device can be enabled and disabled from an external source that can be fed into the ENBL SMA connector or the VENB test point, in which case SW11 should be placed in the DENBL position.

The IF and MX inputs are selected via SW12. The switch should be moved in the direction of the desired input.

For convenience, a potentiometer, R15, is provided to allow for changes in gain without the need for an additional dc voltage source. To use the potentiometer, the SW13 switch must be set to the POT position. Alternatively, an external voltage applied to either the test point or SMA connector labeled VGIN can set the gain. SW13 must be set to the EXT position when an external gain control voltage is used.

The local oscillator signal should be fed to the SMA connector J21. This port is terminated in 50 Ω. The LO power input range is from –12 dBm to 0 dBm and at a frequency equal to double that of the IF/MX frequency.

The IF input should be fed into the SMA connector IFIP. The VGA must be enabled when this port is used (SW12 in the IF position).

The evaluation board is by default set for differential MX drive through a balun (T41) from a single-ended source fed into the MXIP SMA connector. To change to a differential driving source, T41 should be removed along with Resistor R42. The 0 Ω Resistors R43 and R44 should be installed in place of T41 to bridge the gap in the input traces. This will present a nominal differential impedance of 200 Ω (100 Ω each side). The differential inputs should then be fed into SMA connectors MXIP and MXIN.

The baseband outputs are made available at the IOPP, IOPN, QOPP, and QOPN test points and SMA connectors. These outputs are not designed to be connected directly to 50 Ω loads and should be presented with loads of approximately 2 kΩ or greater.

The dc bias level of the baseband amplifier outputs are by default tied to VREF through LK11. If desired, the dc bias level can be changed by removing LK11 and driving a dc voltage onto the VCMO test point.

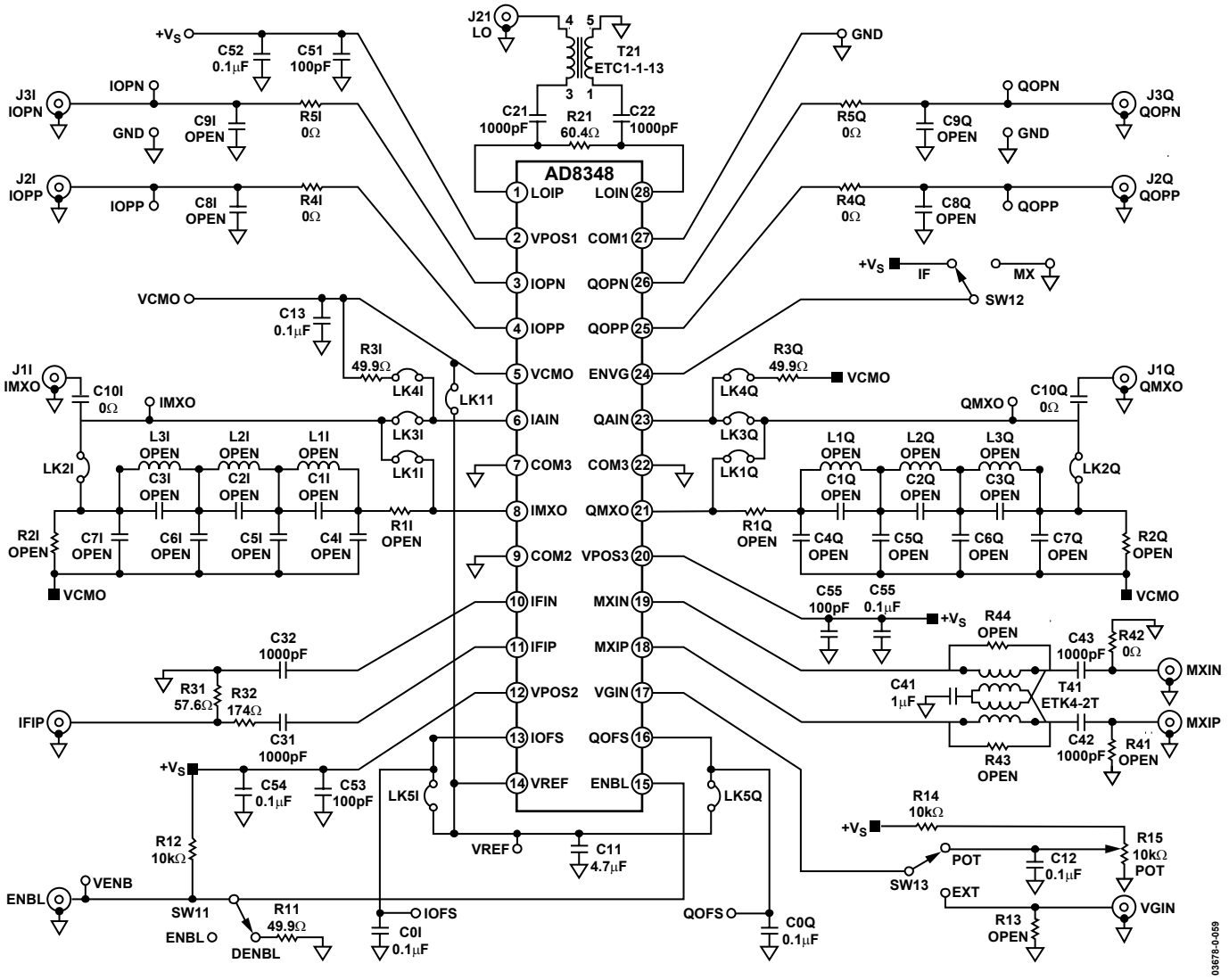

Figure 60. Evaluation Board Schematic

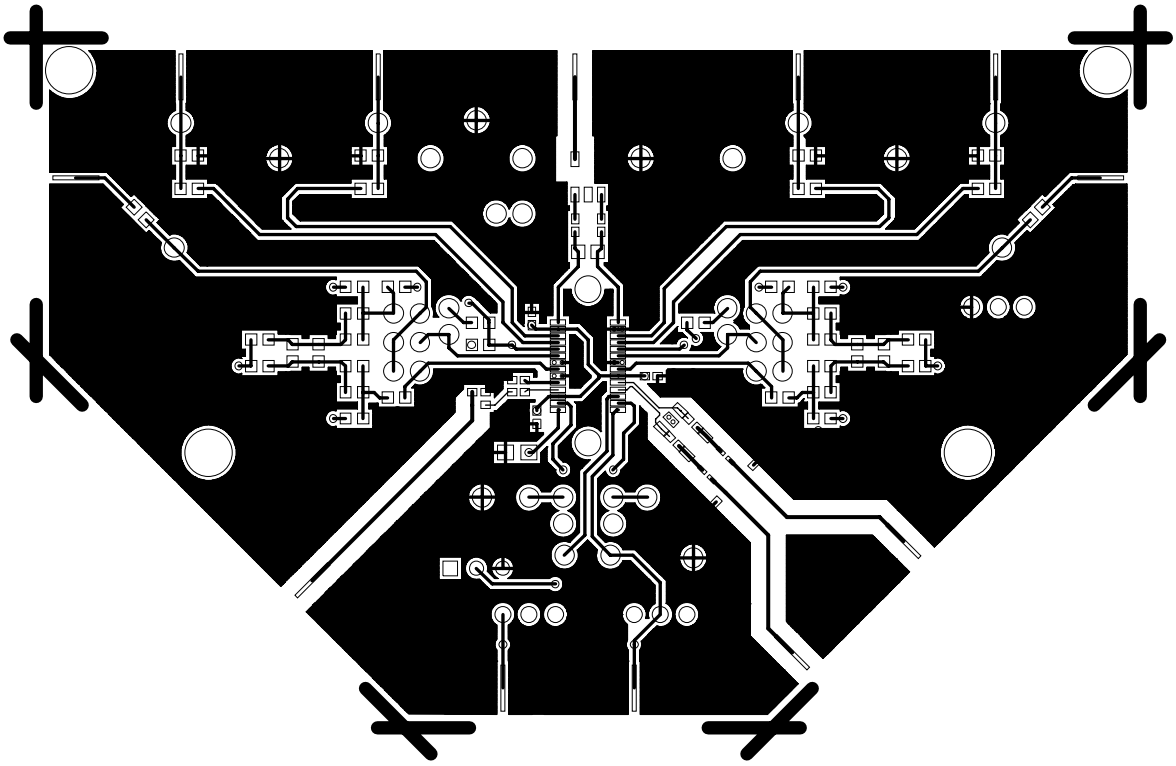

Figure 61. Evaluation Board Top Layer

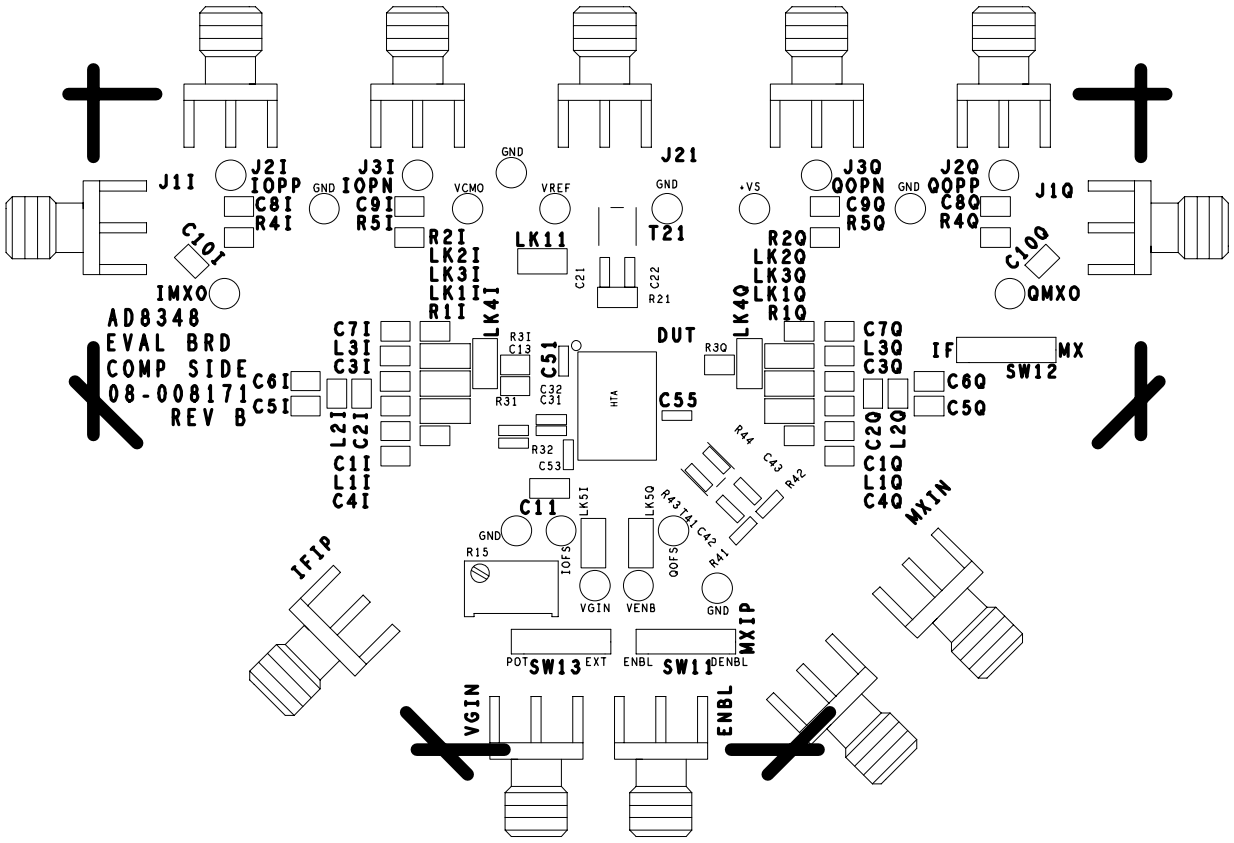

Figure 62. Evaluation Board Top Silkscreen

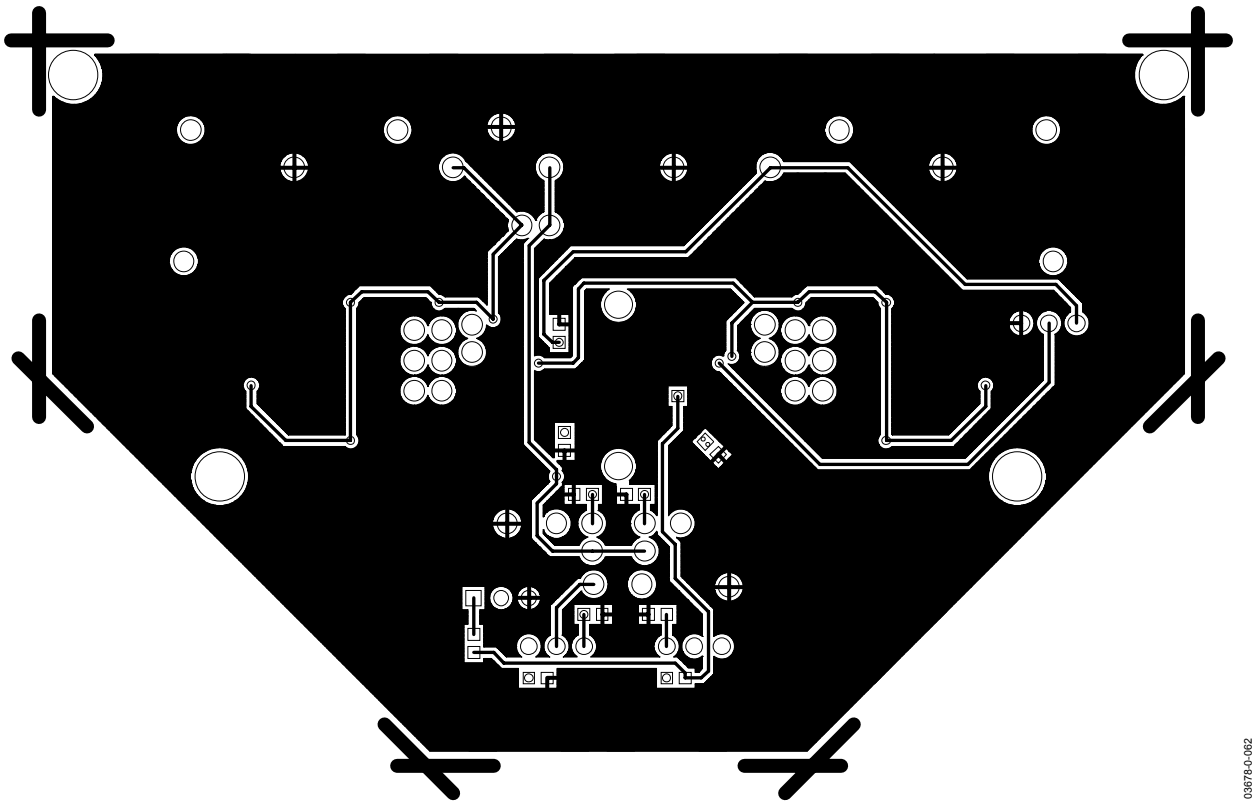

Figure 63. Evaluation Board Bottom Layer

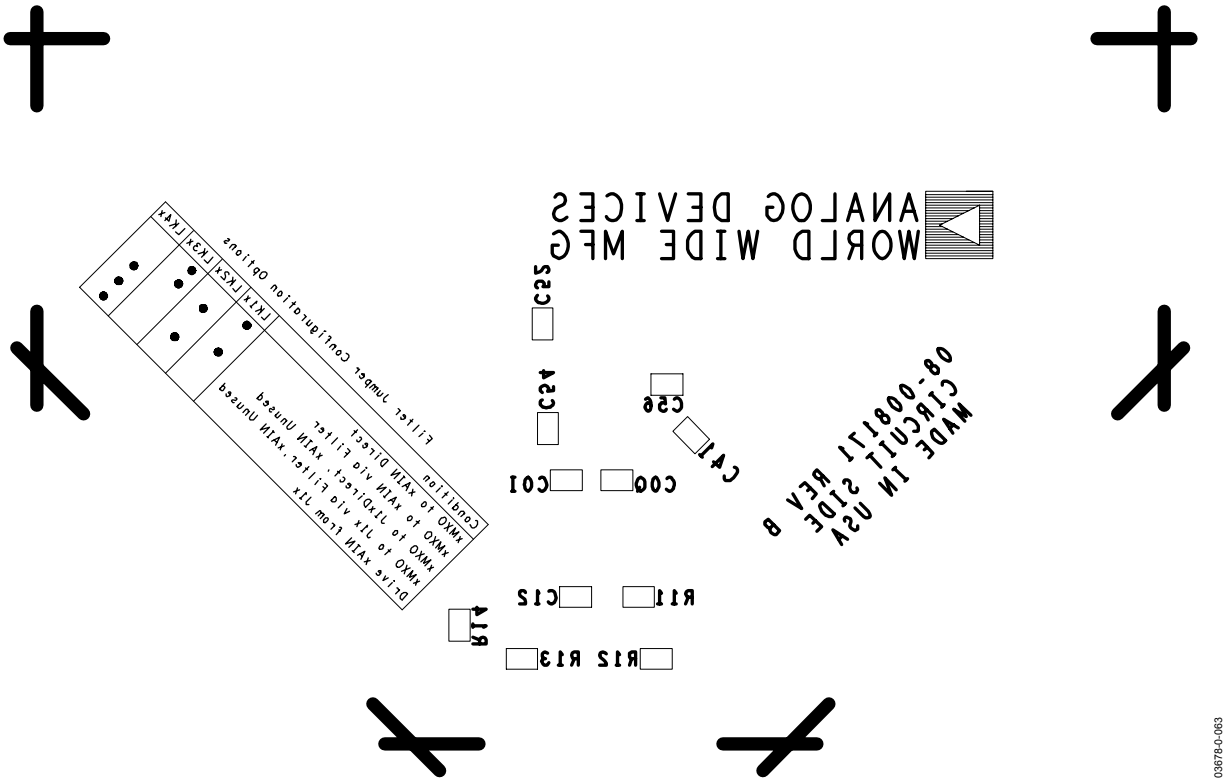

Figure 64. Evaluation Board Bottom Silkscreen

Table 6. Evaluation Board Configuration Options

Component	Function	Default Condition
$+V_S$, GND	**Power Supply and Ground Vector Pins**.	Not Applicable
SW11, ENBL	**Device Enable**: Place SW11 in the ENBL position to connect the ENBL pin to $+V_S$. Place SW11 in the DENBL position to disable the device by grounding the pin ENBL through a 50 Ω pull-down resistor. The device may also be enabled via an external voltage applied to ENBL or VENB.	SW11 = ENBL
SW13, R15, VGIN	**Gain Control Selection**: With SW13 in the POT position, the gain of the VGA can be set using the R15 potentiometer. With SW13 in the EXT position, the VGA gain can be set by an external voltage to the SMA connector VGIN. For VGA operation, the VGA must first be enabled by setting SW12 to the IF position.	SW2 = POT
SW12	**VGA Enable Selection**: With SW12 in the IF position, the ENVG pin is connected to $+V_S$ and the VGA is enabled. The IF input should be used when SW12 is in the IF position. With SW12 in the MX position, the ENVG pin is grounded and the VGA is disabled. The MX inputs should be used when SW12 is in the MX position.	SW12 = IF
IFIP, R31, R32	**IF Input**: The single-ended IF signal should be connected to this SMA connector. R31 and R32 form an L Pad that presents a 50 Ω termination to the input.	R31 = 57.6 Ω R32 = 174 Ω
MXIP, MXIN T41, R41, R42, C42, C43	**Mixer Inputs**: These inputs can be configured for either differential or single-ended operation. The evaluation board is by default set for differential MX drive through a balun (T41) from a single-ended source fed into the MXIP SMA connector. To change to a differential driving source, T41 should be removed along with Resistor R42. The 0 Ω resistors R43 and R44 should be installed in place of T41 to bridge the gap in the input traces. This will present a nominal differential impedance of 200 Ω (100 Ω each side). The differential inputs should then be fed into SMA connectors MXIP and MXIN.	T41 = M/A-COM ETK4-2T R41, C42, C43 = OPEN R42 = 0 Ω
LK11, VCMO	**Baseband Amplifier Output Bias**: Installing LK11 connects VREF to VCMO. This sets the bias level on the baseband amplifiers to VREF, which is equal to approximately 1 V. Alternatively, with LK11 removed, the bias level of the baseband amplifiers can be set by applying an external voltage to the VCMO test point.	LK11 Installed
C8, C9, R4, R5 (I and Q)	**Baseband Amplifier Outputs and Output Filter**: Additional low-pass filtering can be provided at the baseband output with these filters.	R4, R5 = 0 Ω
C10 (I and Q)	**Mixer Output DC Blocking Capacitors**: The mixer outputs are biased to VCMO. To prevent damage to test equipment that cannot tolerate dc biases, C10 is provided to block the dc component, thus protecting the test equipment.	C10 = 0 Ω
C1–C7 R1, R2 L1–L3 (I and Q)	**Baseband Filter**: These components are provided for baseband filtering between the mixer outputs and the baseband amplifier inputs. The baseband amplifier input impedance is high and the filter termination impedance is set by R2. See Table 7 for the jumper settings.	All = OPEN
LK5 (I and Q)	**Offset Compensation Loop Disable**: Installing these jumpers will disable the offset compensation loop for the corresponding channel.	LK5x = OPEN

Table 7. Filter Jumper Configuration Options

Condition	LK1x	LK2x	LK3x	LK4x
xMXO to xAIN Direct	•		•	
xMXO to xAIN via Filter		•	•	
xMXO to J1x Direct, xAIN Unused	•			•
xMXO to J1x via Filter, xAIN Unused		•		•
Drive xAIN from J1x				•

OUTLINE DIMENSIONS

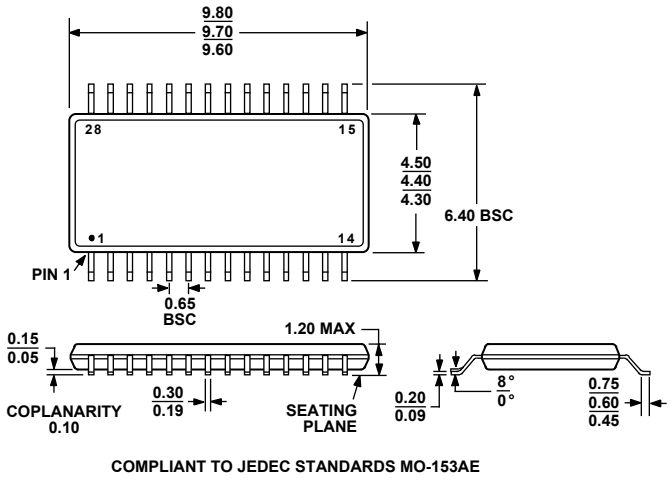

Figure 65. 28-Lead Thin Shrink Small Outline Package [TSSOP] (RU-28)
Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

AD8348 Products	Temperature Range	Package Description	Package Option
AD8348ARU	–40°C to +85°C	Thin Shrink Small Outline Package (28-Lead TSSOP)	RU-28
AD8348ARU-REEL7	–40°C to +85°C	7″ Tape and Reel	RU-28
AD8348-EVAL		Evaluation Board	