Si720x Switch/Latch Hall Effect Magnetic Position Sensor Data Sheet

The Si7201/2/3/4/5/6 family of Hall effect magnetic sensors and latches from Silicon Labs combines a chopper-stabilized Hall element with a low-noise analog amplifier, 13-bit analog-to-digital converter, and flexible comparator circuit. Leveraging Silicon Labs' proven CMOS design techniques, the Si720x family incorporates digital signal processing to provide precise compensation for temperature and offset drift.

Compared with existing Hall effect sensors, the Si720x family offers industry-leading sensitivity, which enables use with larger air gaps and smaller magnets. For battery-powered applications, the Si720x family offers very low power consumption to improve operating life. For automotive applications, the Si720x family is AEC-Q100 qualified.

The Si720x devices are offered in 3-pin SOT23 and TO-92 packages, with power, ground, and a single output pin that goes high or low as the magnetic field increases. With the three-pin package, tamper indication is by the pin going back to its zero field level at high magnetic field.

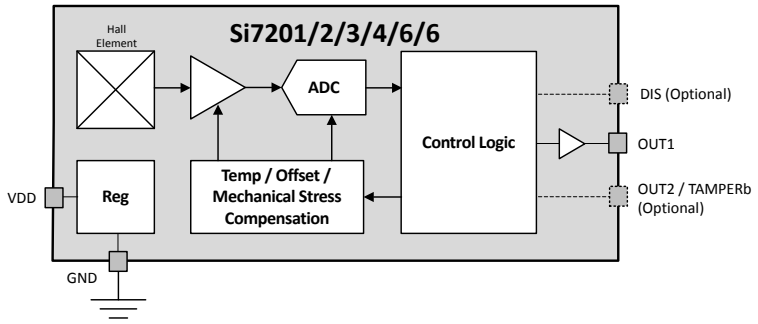
In the 5-pin SOT23 and 8-pin DFN packages, pins are available for both sleep mode activation and separate tamper indication.

Applications:

- Replacement of reed switches in consumer, automotive, and security applications
- Automotive position sensing of HVAC valve, head rest, seat track, side mirrors, sunroof, door locks, and other mechanical devices
- BLDC motor control
- Camera image stabilization, zoom, and autofocus
- Fluid level sensing
- Control knobs and selector switches
- General-purpose mechanical position sensing

FEATURES

- High-Sensitivity Hall Effect Sensor
  - Maximum B_{OP} operating point/minimum field strength of <1.1 mT
  - Omnipolar or unipolar operation
  - Integrated digital signal processing for temperature and offset drift compensation
- Low 400 nA Typical Current Consumption
- Selectable / Programmable Sensitivity, Hysteresis, Output Polarity and Sample Rate
- Sensitivity Drift < ±3% over Temperature
- Wide Power Supply Voltage
  - 1.7 to 5.5 V
  - 3.3 to 26.5 V
- AEC-Q100 Qualified for Automotive Applications
- Selectable Output Options
  - Open-drain output
  - Digital high/low output
  - 2-wire current source
- Industry-Standard Packaging
  - Surface mount SOT-23 (3 or 5 pin)
  - Through hole TO-92 (3-pin) (coming soon)
  - 1.4 x 1.6 mm 8-pin DFN package (coming soon)



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1. Electrical Specifications

Unless otherwise specified, all min/max specifications apply over the recommended operating conditions.

Table 1.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply	V_{DD}	Si7201/2/3/4	1.71		5.5[1]	V
Power Supply	V_{DD}	Si7205/6	3.3		26.5	V
Temperature	T_A	I grade	-40		+125[2]	°C

Note:
1. 3.6 V for most sensitive parts (see 5. Ordering Guide).
2. 0-70°C for most sensitive parts (F grade) (see 5. Ordering Guide).

Table 1.2. General Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage High	V_{IH}	DIS pin	0.7 x V_{DD}	-	-	V
Input Voltage Low	V_{IL}	DIS pin	-	-	0.3 x V_{DD}	V
Input voltage Range	V_{IN}	DIS pin	0		V_{DD}	V
Input Leakage	I_{IL}	DIS pin			1	µA
Output Voltage Low	V_{OL}	TAMPERb pin I_{OL} = 3 mA V_{DD} > 2 V			0.4	V
		TAMPERb pin I_{OL} = 2 mA V_{DD} > 1.7 V			0.2	V
		TAMPERb pin I_{OL} = 6 mA V_{DD} > 2 V			0.6	V
Output Voltage High	V_{OH}	TAMPERb pin I_{OH} = 2 mA V_{DD} > 2.25 V	V_{DD} – 0.4			V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current Consumption	I_{DD}	Conversion in progress:				mA
		V_{DD} = 1.8 V		3.5	4.5	
		V_{DD} = 3.3 V		5	6	
		V_{DD} = 5 V		6.8	8.5	
		High voltage parts (V_{DD} = 3.3 to 26.5 V)		6.5	8.5	mA
		Sleep mode		50	1000	nA
		Idle mode (Si7210/2/3/4)		360	700	µA
		Idle mode (Si7205/06)		860	1200	µA
		Sleep timer enabled average at V_{DD} = 3.3 V and 200 msec sleep time		0.4		µA
Conversion Time	T_{CONV}	First conversion when waking from sleep or idle		11		µs
		Additional conversions in a burst		8.8		µs
Sleep Time[2]	T_{SLEEP}	Factory configurable from 1 to 200 msec ±20%				
Idle Time[3]	T_{IDLE}	Minimum	11.9	13.2	14.5	usec
		Maximum	185	206	227	msec
Wake Up Time	T_{WAKE}	Time from V_{DD} > 1.7 V to first measurement			1	msec

Note:

1. TAMPERb and DIS pin specifications apply when the pin is present. These functions are only supported for the V_{DD} range of 1.7 – 5.5 V (Si7203/4).
2. Parts go to sleep or idle mode between measurements. Sleep time can be factory programmed from 0.875 msec to 254 msec nominal with accuracy of ±30%. Typically, sleep time is set to 100 msec and the sleep time counter is adjusted to give accuracy within ±10%.
3. Idle time can be factory programmed from 13.2 µsec to 206 msec ±10% or set to zero in which case conversions are done every 8.8 µsec. Normally idle time is only used at higher sample speeds.
4. For high voltage parts (V_{DD} = 26.5 V maximum), the power on ramp should be faster than 10 V per second in the start-up region from 2 to 3 V.

Table 1.3. Output Pin Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si7201/2/3/4						
Output Voltage Low Open Drain or Push Pull	V_{OL}	I_{OL} = 3 mA V_{DD} > 2 V			0.4	V
		I_{OL} = 2 mA V_{DD} > 1.7 V			0.2	V
		I_{OL} = 6 mA V_{DD} > 2 V			0.6	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage Output High Output Pin Open Drain	I_{OH}				1	µA
Output Voltage High Output Pin Push Pull	V_{OH}	I_{OH} = 2 mA V_{DD} > 2.25 V	V_{DD} – 0.4			V
Slew Rate	T_{SLEW}			5		$\%V_{DD}$/nS
Si7205/6						
Output Voltage Low	V_{OL}	I_{OL} = 11.4 mA V_{DD} > 6 V			0.4	V
Safe Continuous Sink Current					20	mA
Leakage Output High Output Pin Open Drain	I_{OH}				1	µA
Slew Rate Digital Output Mode	T_{SLEW}			5		$\%V_{DD}$/nS
Output Pin Shorted to V_{DD}	I_{SHORT}	V_{DD} = 12 V Average current as pin cycles		4		mA

The Si7205 and Si7206 can be configured to signal the status equivalent to output high or low by modulating the power supply current. If configured in this way, the following are the specifications for the amount of current that will be drawn for the “output high” state.

Table 1.4. I_{DD} Signaling

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I_{DD} Signaling Current	I_{DO}	V_{DDH} > 6 V	8	10	12	mA

Table 1.5. Magnetic Sensor[2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset[1]	B_{OFF}	20 mT scale V_{DD} = 1.71 to 3.6 V 0-70°C		±150	±250	µT
		20 mT scale V_{DD} = 1.71 to 5.5 V Full temperature range		±250	+450, -350	µT
Gain Accuracy		0-70°C			5	%
		Full temperature range			10	%
RMS Noise[3]		Room temp, 20 mT range, V_{DD} = 5 V		30		µT rms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. See the 5. Ordering Guide to determine Bop/Brp for various OPNs.
2. See the 5. Ordering Guide for operating a release points. These are defined as maximum operating point and minimum release point -40 °C to +150 °C and do not include the effect of noise.
3. For a single conversion. This can be reduced by the square root of N by filtering over N samples. See ordering guide for samples taken per measurement.

Table 1.6. Temperature Compensation

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Bop and Brp vs Temperature		No compensation 0-70°C		< ±0.05		%/°C
		Neodymium compensation		-0.12		%/°C
		Ceramic compensation		-0.2		%/°C

Table 1.7. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Air Thermal Resistance	θ_{JA}	JEDEC 4 layer board no airflow SOT23-5	212.8	°C/W
Junction to Board Thermal Resistance	θ_{JB}	JEDEC 4 layer board no airflow SOT23-5	45	°C/W
Junction to Air Thermal Resistance	θ_{JA}	JEDEC 4 layer board no airflow SOT23-3	254.6	°C/W
Junction to Board Thermal Resistance	θ_{JB}	JEDEC 4 layer board no airflow SOT23-3	54.8	°C/W

Table 1.8. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature Under Bias			-55		125	°C
Storage Temperature			-65		150	°C
Si7201/2/3/4						
Voltage on I/O Pins			-0.3		V_{DD}+0.3	V
Voltage on V_{DD} with Respect to Ground			-0.3		6	V
ESD Tolerance		HBM			2	kV
		CDM			500	V
Si7205/6						
Voltage on Ouput pin[2]			-21		40	V
Voltage on V_{DD} with Respect to Ground[3]			-21		40	V
ESD Tolerance		HBM			8	kV
		CDM			500	V

Note:

1. Absolute maximum ratings are stress ratings only, operation at or beyond these conditions is not implied and may shorten the life of the device or alter its performance.
2. The output pin can withstand EMC transients per ISO 7637-2-2-11 and Ford EMC-CS-2009.1 with a current limiting resistor of 220 Ω to a local bypass cap of 0.1 µF and additional 22 Ω between the capacitor and ground..
3. V_{DD} can withstand automotive EMC transients per ISO 7637-2-2-11 and Ford EMC-CS-2009.1 with a current limiting resistor of 220 Ω.

2. Functional Description

The Si7201/2/3/4/5/6 family of Hall Effect magnetic sensors digitize the component of the magnetic field in the z axis of the device (positive field is defined as pointing into the device from the bottom). The digitized field is compared to a pre-programmed threshold and the output pin goes high or low if the threshold is crossed. The parts are normally used to detect the presence or absence of a magnet in security systems, as position sensors or for counting revolutions.

Table 2.1. Part Ordering Guide

Part Number	Description
Si7201	Low voltage switches
Si7202	Low voltage latches
Si7203	Low voltage switch with tamper and/or disable pins
Si7204	Low voltage latches with tamper and/or disable pins
Si7205	High voltage switches
Si7206	High voltage latches

The output pin (push pull or open collector) can go high or low when the magnetic field crosses a threshold. The output pin configuration is determined by the type of part ordered.

The parts are preconfigured for the magnetic field measurement range, magnetic field operate and release points, sleep time, temperature compensation, tamper threshold and digital filtering and will wake into this mode when first powered. The specific configuration output type (open collector or push pull) are determined by the part number.

Following is a list of configuration options:

- Measurement Range: This is normally set so that after temperature compensation the full scale output is ±20.47 mT or ±204.7 mT For convenience these are referred to as the 20 mT and 200 mT scales
- Decision Points:
  - For 20 mT switch mode parts, the middle of the decision point can be configured from 0.08 mT to 19.2 mT. For 200 mT parts, the middle point of the decision threshold can be programmed from 0.8 mT to 192 mT
  - For latch mode parts the middle of the decision point is zero.
  - For 20 mT scale switch mode parts, the hysteresis can be programmed to ±0.04 mT to ±8.96 mT. On the 200 mT scale, these numbers are multiplied by 10.
  - For latch mode parts the decision points can be configured from ±0.08 mT to ±17.92 mT on the 20 mT scale. On the 200 mT scale these numbers are multiplied by 10.
  - For 20 mT scale parts, the tamper threshold can be configured from 2.65 mT to 19.84 mT. On the 200 mT scale these numbers are multiplied by 10. Tamper detection can also be disabled.
- Digital Filtering: To reduce noise in the output (normally 0.03 mT RMS on the 20 mT scale), digital filtering can be applied. The digital filtering can be done to a burst a measurements (FIR filter) or can be configured to average measurements in IIR style. The filtering can be done over a number of samples in powers of 2 (1,2,4,8,…) for up to 2^{12} (4096) samples
- Time between Measurements (or Measurement Bursts for the Case of FIR Filtering):
  - For lowest power, the part can be configured to sleep between measurements. Sleep times are configurable from 1 msec to 200 msec.
  - For faster measurement rates and for analog output mode the part is configured to idle between samples. Idle times are variable from 13.2 µsec to 206 msec nominally.
- The Digital Output Pin:
  - The direction in which the output pin goes in response to an increase in field
  - There is an option to take the magnitude of the field prior to the comparison so that the polarity is not field dependent
  - For 3 pin parts in the case of tamper detection the output pin will go to its zero field value (which in security systems is normally an indication of door or window open).
  - For 4 and 5 pin parts there is a separate tamper indication pin
- Temperature compensation of the magnetic field response to compensate for the nominal drop in magnetic field output of common magnets with increasing temperature.

  Note: In this case accuracy is defined at 25°C and the sensitivity increases at higher temperature

Examples:

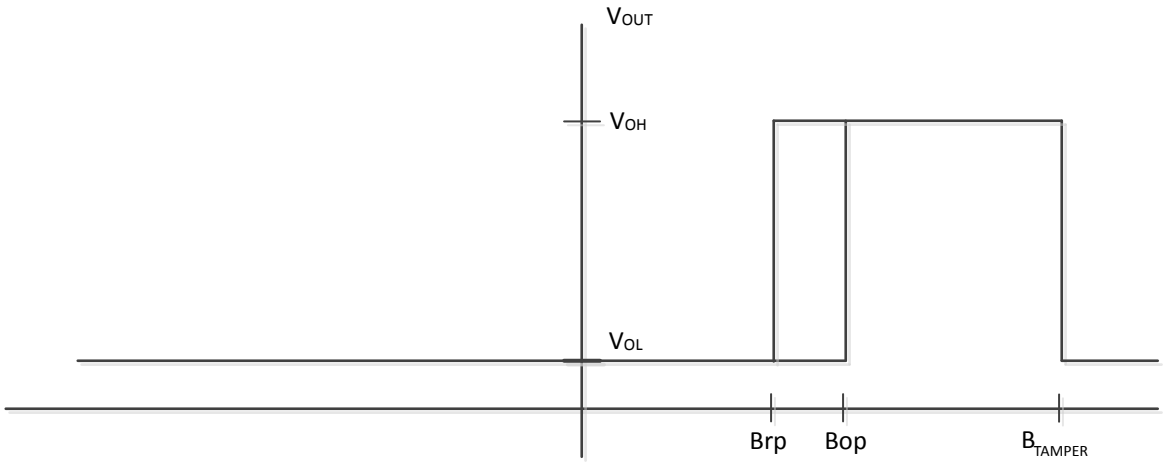


Figure 2.1. Unipolar Switch with Tamper

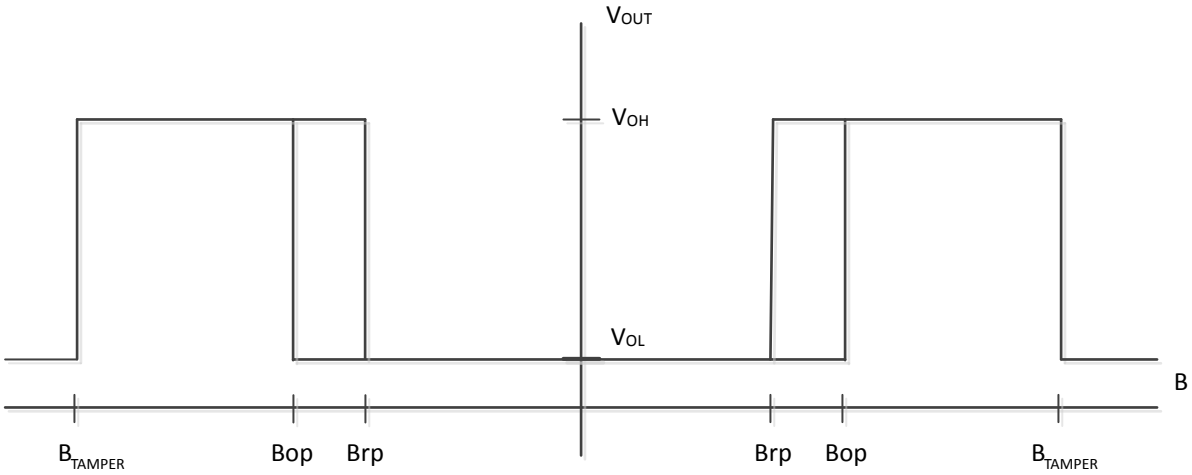


Figure 2.2. Omnipolar Swith with Tamper

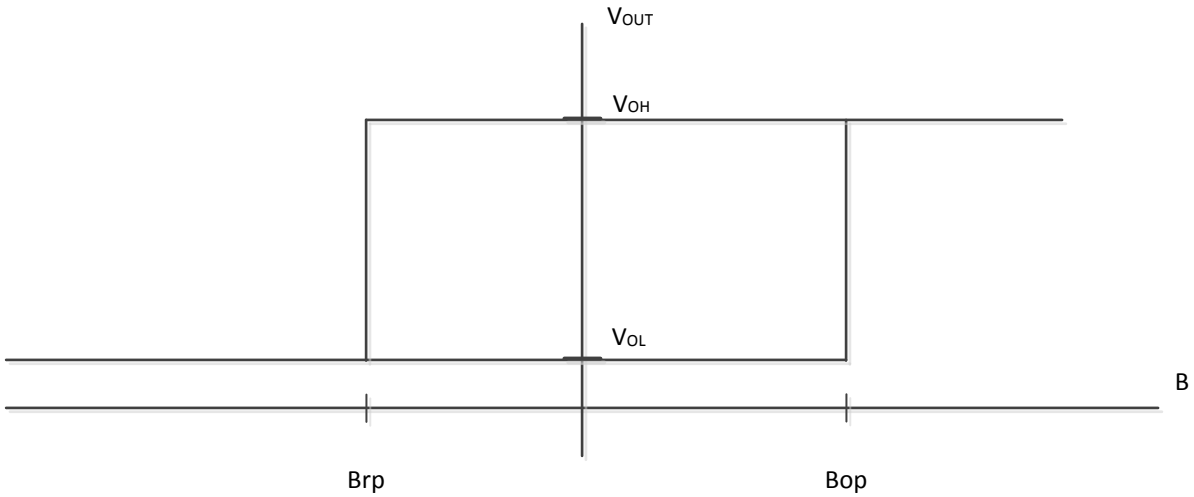


Figure 2.3. Latch

3. DISABLE Pin Timing

For a part that has a DISABLE pin, DISABLE high will put the part in complete sleep mode with I_{DD} typical of 100 nA. When DISABLE goes low, the part will wake and initiate a measurement. For a single measurement, this takes 11 µsec typically. Additional measurements in a burst take 8.8 µsec. Once the measurement (burst) is complete, the output pin status is updated and the part enters idle mode. The part will make a new measurement or measurement burst at the time-interval determined by the idle timer (typically 1 msec). The idle timer is reset when DISABLE transitions from high to low, so the time from the first measurement until the next measurement will always be the programmed idle time.

Disable low pulses can be as short as 1 µsec. For pulses shorter than a conversion burst, the part will make one burst and then go back to sleep.

When disable returns high, a measurement in progress (if any) will complete and the part will enter sleep mode.

As the idle time is typically long (i.e. 1 msec) compared to the measurement time (i.e. 11 µsec), it is possible to keep the DISABLE pin low duration short (i.e. 15 µsec) and have a long period in the sleep state. This is an effective way to control the sample rate and power.

For example, if the part is programmed to make a single measurement at a time and is programmed with an idle time of 1 msec and DISABLE is pulsed low for 15 µsec every 50 msec, then the average I_{DD} will be:

- 11 µsec to wake and make a measurement at I_{DD} typical of 5.0 mA (3.3V)/(50.015 msec cycle time) = 1.0 µA
- 4 µsec in idle mode at typical current of 360 µA/(50.015 msec cycle time) = 0.03 µA
- 50 msec in sleep mode at 50 nA/(50.015 msec cycle time) = 0.05uA
- Or 1.08 µA total

As the programmed idle time is shorter than the DISABLE low time in the example, the value of the programmed idle time does not make a difference.

4. Pin Description

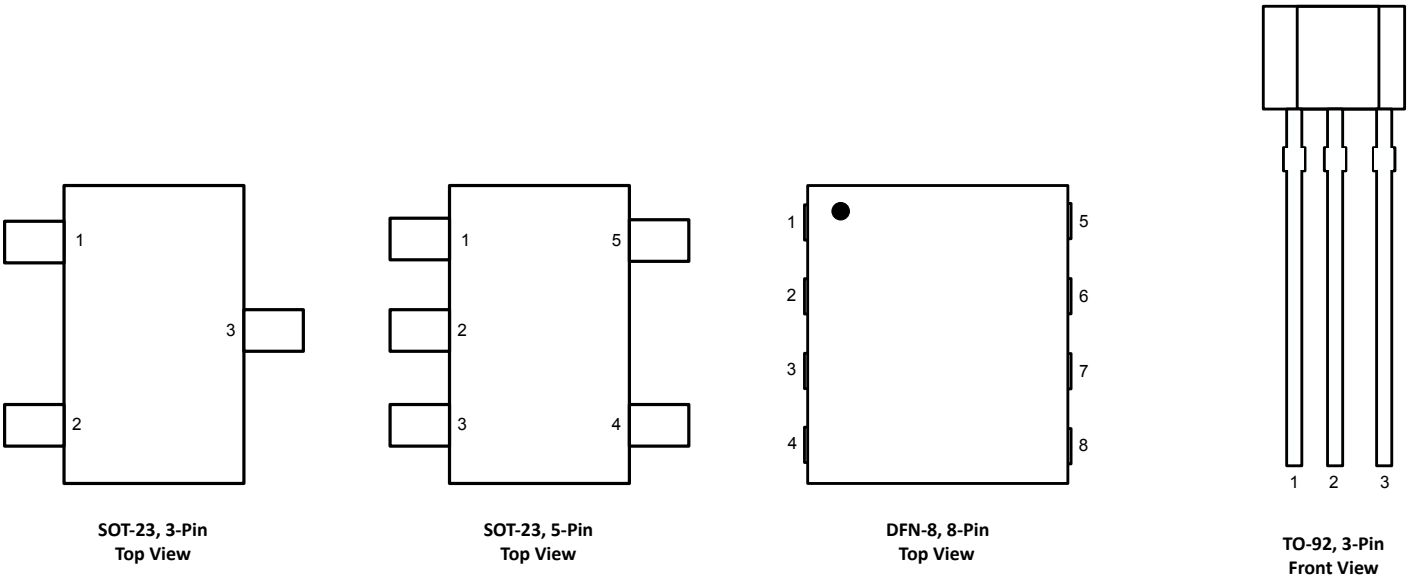


Figure 4.1. Si720xxx Pin Assignments

Note:

The 3-pin option includes part numbers: Si7201/2/5/6.

The SOT-23 5 pin and DFN 8 pin options include part numbers: Si7203/4.

Table 4.1. Si7201/2/5/6 (SOT23 3-pin Package)

Pin Name	Pin Number	Description
VDD	1	Power +1.7 to +5.5 V or 3.3 to 26.5 V
OUT1	2	Switch/latch output
GND	3	Ground

Table 4.2. Si7203/4/5 (SOT23 5-pin Package)

Pin Name	Pin Number	Description
OUT2/TAMPERb	1	OUT2/TAMPERb (tamper/high field indicator)
GND	2	Ground
DIS	3	Disables part (puts into sleep mode) when high. Measurement cycle will resume when pin goes low
VDD	4	Power +1.7 to +5.5 V
OUT1	5	Switch/latch output

Table 4.3. Si7203/4 (DFN 8-pin Package)

Pin Name	Pin Number	Description
VDD	8	Power +1.7 to +5.5 V
GND	1, 5	Ground
OUT1	6	Switch/latch output
OUT2/TAMPERb	4	OUT2/TAMPERb (tamper/high field indicator)
DIS	2	Disable (puts part into Sleep mode) when high. Measurement cycle will resume when pin goes low.

Table 4.4. Si7201/2/5/6 (TO-92 Package)

Pin Name	Pin Number	Description
VDD	1	Power
GND	2	Ground
OUT1	3	Output

5. Ordering Guide

Part No.[1]	Output Type	Output Polarity (high field)	IDD (typ. @ 3.3 V)	BOP, BRP[2]	Sleep/Idle Time	Temp Compensation	Tamper Threshold (typ.)	Digital Filtering	VDD
3-pin Switches. Temperature rating 0 °C to 70 °C.									
Si7201-B-00-FV(R)	Omnipolar Switch	Low (push-pull)	0.4 µA	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) |BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	None	None	1.7 - 3.6 V
Si7201-B-01-FV(R)	Omnipolar Switch	Low (push-pull)	0.4 µA	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) |BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	±19.8 mT	None	1.7 - 3.6 V
Si7201-B-02-FV(R)	Omnipolar Switch	High (push-pull)	1.1 µA	BOP = ±0.9 mT (max) BRP = ±0.2 mT (min) |BOP - BRP| = 0.2 mT (typ)	200 msec (sleep)	0.12%/°C	±19.8 mT	4 sample FIR	1.7 - 3.6 V
3-pin Switches. Temperature rating -40 °C to 125 °C.									
Si7201-B-03-IV(R)	Omnipolar Switch	High (push-pull)	57 µA	BOP = ±2.8 mT (max) BRP = ±1.1 mT (min) |BOP - BRP| = 0.6 mT (typ)	1 msec (sleep)	None	None	None	1.7 - 5.5 V
Si7201-B-04-IV(R)	Omnipolar Switch	Low (push-pull)	0.4 µA	BOP = ±1.4 mT (max) BRP = ±0.2 mT (min) |BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	None	None	1.7 - 5.5 V
Si7201-B-05-IV(R)	Omnipolar Switch	Low (push-pull)	0.4 µA	BOP = ±2.0 mT (max) BRP = ±0.6 mT (min) |BOP - BRP| = 0.6 mT (typ)	200 msec (sleep)	None	±19.8 mT	None	1.7 - 5.5 V

Part No.[1]	Output Type	Output Polarity (high field)	IDD (typ. @ 3.3 V)	BOP, BRP[2]	Sleep/Idle Time	Temp Compensation	Tamper Threshold (typ.)	Digital Filtering	VDD
Si7201-B-06-IV(R)	Omnipolar Switch	Low (open drain)	0.4 µA	BOP = ±2.0 mT (max) BRP = ±0.6 mT (min) |BOP - BRP| = 0.6 mT (typ)	200 msec (sleep)	None	None	None	1.7 - 5.5 V
Si7201-B-07-IV(R)	Omnipolar Switch	Low (open drain)	0.4 µA	BOP = ±2.0 mT (max) BRP = ±0.6 mT (min) |BOP - BRP| = 0.6 mT (typ)	200 msec (sleep)	None	±19.8 mT	None	1.7 - 5.5 V
3-pin Latches. Temperature rating 0 °C to 70 °C.									
Si7202-B-00-FV(R)	Latch	High (push-pull)	0.4 µA	BOP(max) = +0.65mT BOP(min) = +0.15 mT BRP(min) = -0.65 mT BRP(max) = -0.15 mT |BOP - BRP| = 0.8 mT (typ)	200 msec (sleep)	None	None	None	1.7 - 3.6 V
3-pin Latches. Temperature rating -40 °C to 125 °C.									
Si7202-B-01-IV(R)	Latch	Low (push-pull)	0.4 µA	BOP(max) = +1.4 mT BOP(min) = +0.6 mT BRP(min) = -1.4 mT BRP(max) = -0.6 mT |BOP - BRP| = 2.0 mT (typ)	200 msec (sleep)	None	None	None	1.7 - 5.5 V
5-pin Switches. Temperature rating 0 °C to 70 °C.									
Si7203-B-00-FV(R)	Omnipolar Switch	High (open drain)	0.4 mA (typ) 0.1 µA (DIS high)	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) |BOP - BRP| = 0.4 mT (typ)	1 msec (idle)	None	±19.8 mT	None	1.7 - 3.6 V

Part No.[1]	Output Type	Output Polarity (high field)	IDD (typ. @ 3.3 V)	BOP, BRP[2]	Sleep/Idle Time	Temp Compensation	Tamper Threshold (typ.)	Digital Filtering	VDD
5-pin Latches. Temperature rating 0 °C to 70 °C.									
Si7204-B-00-FV(R)	Latch	High (push-pull)	0.4 mA (typ) 0.1 µA (DIS high)	BOP(max) = +1.1 mT BOP(min) = +0.6 mT BRP(min) = -1.1 mT BRP(max) = -0.6 mT |BOP - BRP| = 1.8 mT (typ)	1 msec (idle)	None	None	None	1.7 - 3.6 V
High Voltage Switches. Temperature rating -40 °C to 125 °C.									
Si7205-B-00-IV(R)	Omnipolar Switch	Low (open drain)	950 µA	BOP = ±3.0 mT (max) BRP = ±0.8 mT (min) |BOP - BRP| = 0.6 mT (typ)	1 msec (idle)	None	None	None	3.3 - 26.5 V
High Voltage Latches. Temperature rating -40 °C to 125 °C.									
Si7206-B-00-IV(R)	Latch	Low (open drain)	950 µA	BOP(max) = +1.4 mT BOP(min) = +0.6 mT BRP(min) = -1.4 mT BRP(max) = -0.6 mT |BOP - BRP| = 2.0 mT (typ)	1 msec (idle)	None	None	None	3.3 - 26.5 V

Note:

1. B is the die revision. The next two digits are used with this look up table to give more specific information. I or F is the temperature range -40 to +125°C or 0 to 70°C. E is the temperature range (-40 to +150°C). B, M, or V is the package type (TO92, DFN8, or SOT23) the optional (R) is the designator for tape and reel (3000 pcs per reel). Parts not ordered by the full reel will be supplied in cut tape.
2. Specified at 25°C for parts with temperature compensation. Scale is 20 mT if Bop/Brp and Tamper threshold support this, otherwise it is 200 mT.
3. North pole of a magnet at the bottom of a SOT23 package is defined as positive field.

6. Package Outline

6.1 SOT23 3-Pin Package

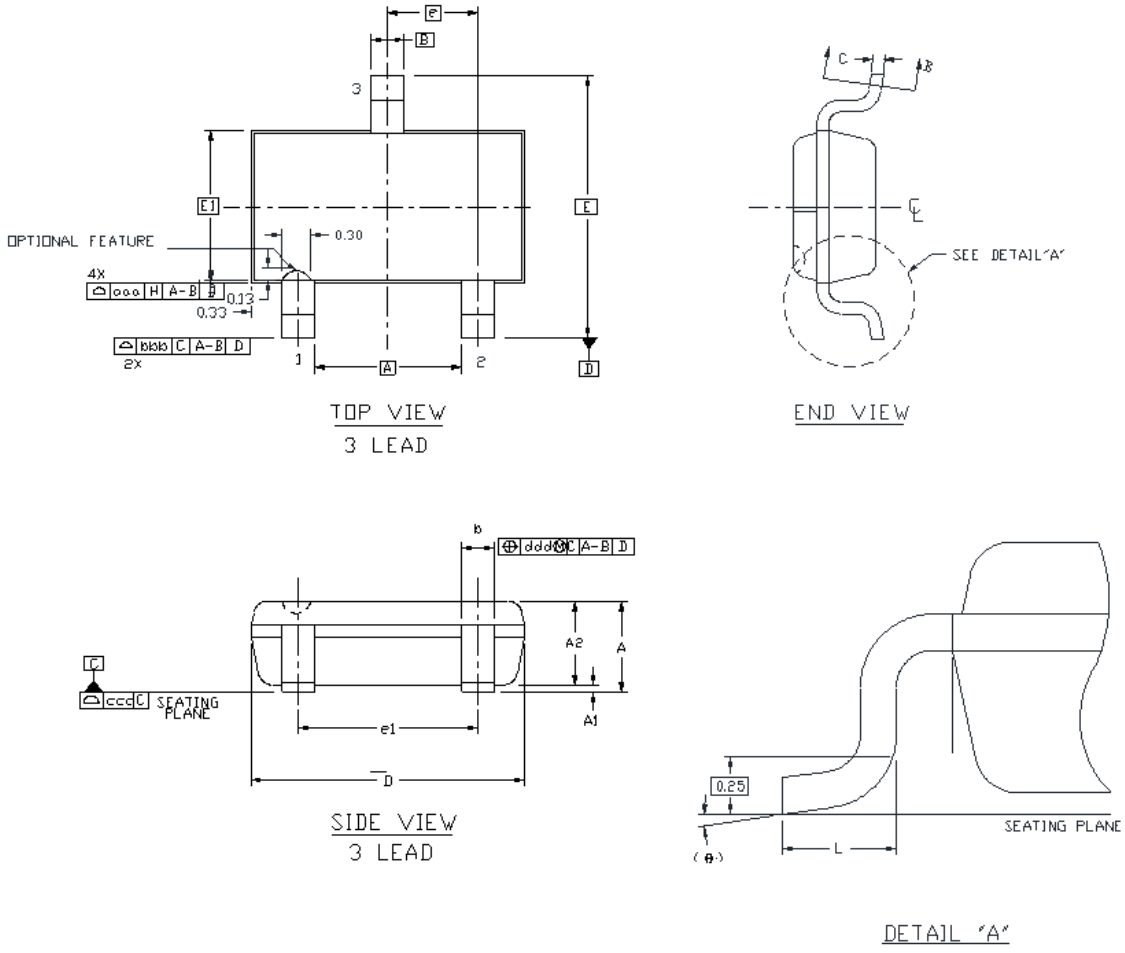


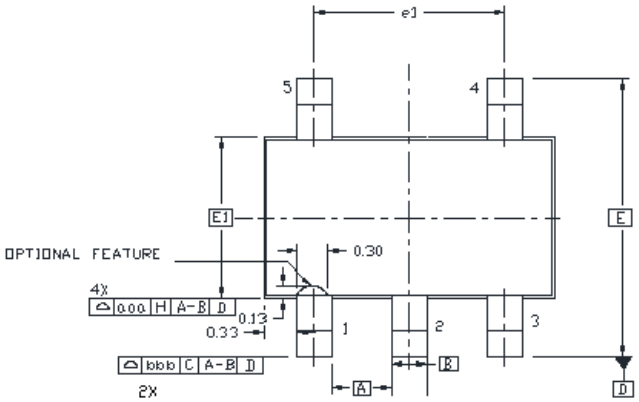
Table 6.1. SOT23 3-Pin Package Dimensions

Dimension	Min	Max
A	--	1.25
A1	0.00	0.10
A2	0.85	1.15
b	0.30	0.50
c	0.10	0.20
D	2.90 BSC	
E	2.75 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
θ	0°	8°
aaa	0.15	
bbb	0.20	
ccc	0.10	
ddd	0.20	

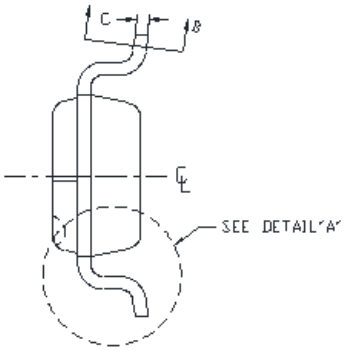
Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-193, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

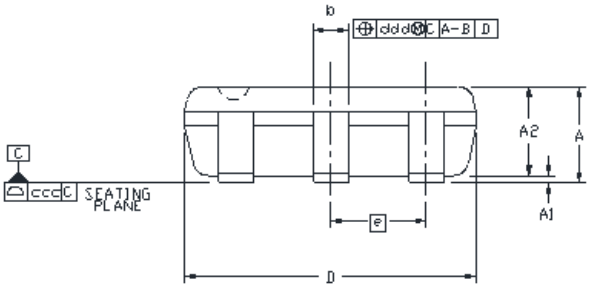
6.2 SOT23 5-Pin Package



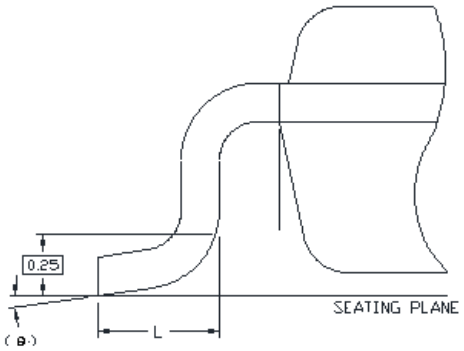
TOP VIEW
6 LEAD



END VIEW



SIDE VIEW
6 LEAD



DETAIL "A"

Table 6.2. SOT23 5-Pin Dimensions

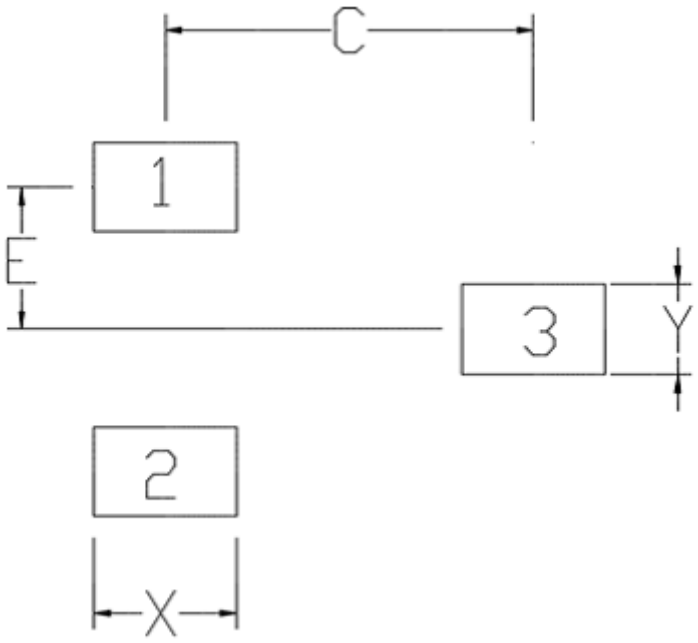
Dimension	Min	Max
A	--	1.25
A1	0.00	0.10
A2	0.85	1.15
b	0.30	0.50
c	0.10	0.20
D	2.90 BSC	
E	2.75 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L2	0.25 BSC	
θ	0°	8°
aaa	0.15	
bbb	0.20	
ccc	0.10	
ddd	0.20	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-193, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

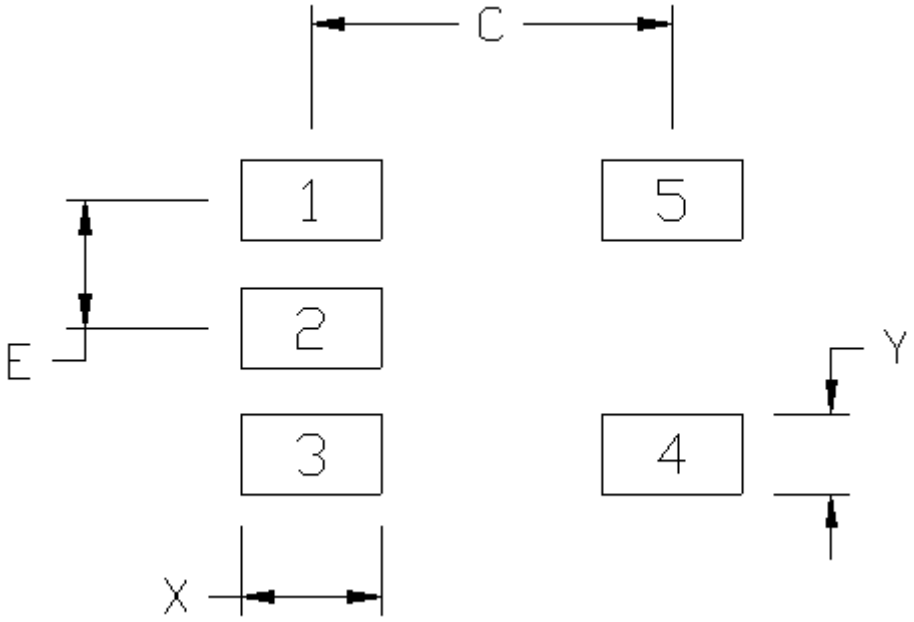
7. Land Patterns

7.1 SOT23 3-Pin PCB Land Pattern



Dimension	(mm)
C	2.70
E	0.95
X	1.05
Y	0.60

7.2 SOT23 5-Pin PCB Land Pattern



Dimension	(mm)
C	2.70
E	0.95
X	1.05
Y	0.60

Note:

General

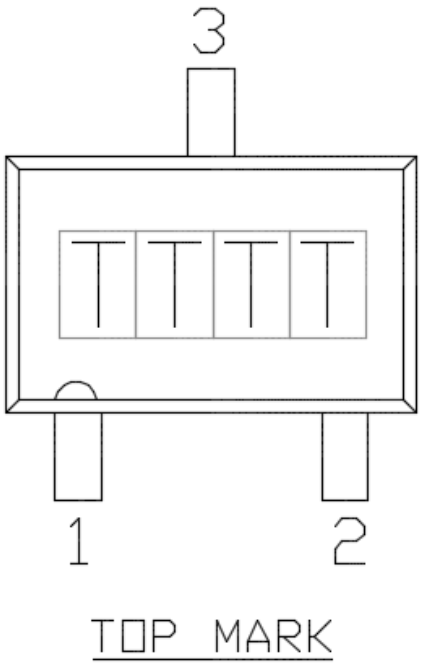
1. 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

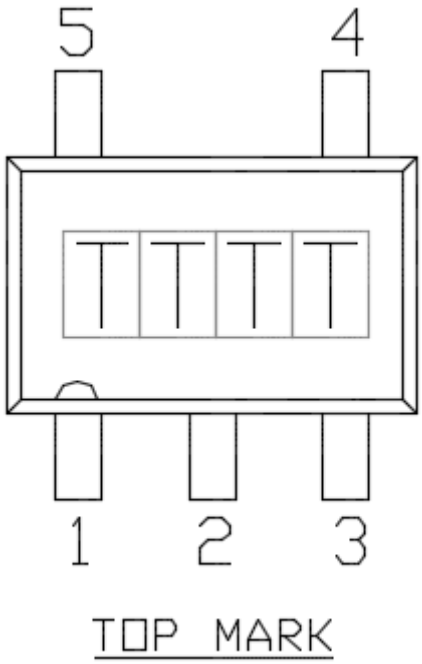
8. Top Marking

8.1 SOT23 3-Pin Top Marking



Note: TTTT is a manufacturing code.

8.2 SOT23 5-Pin Top Marking



Note: TTTT is a manufacturing code.

9. Revision History

9.1 Revision 0.1

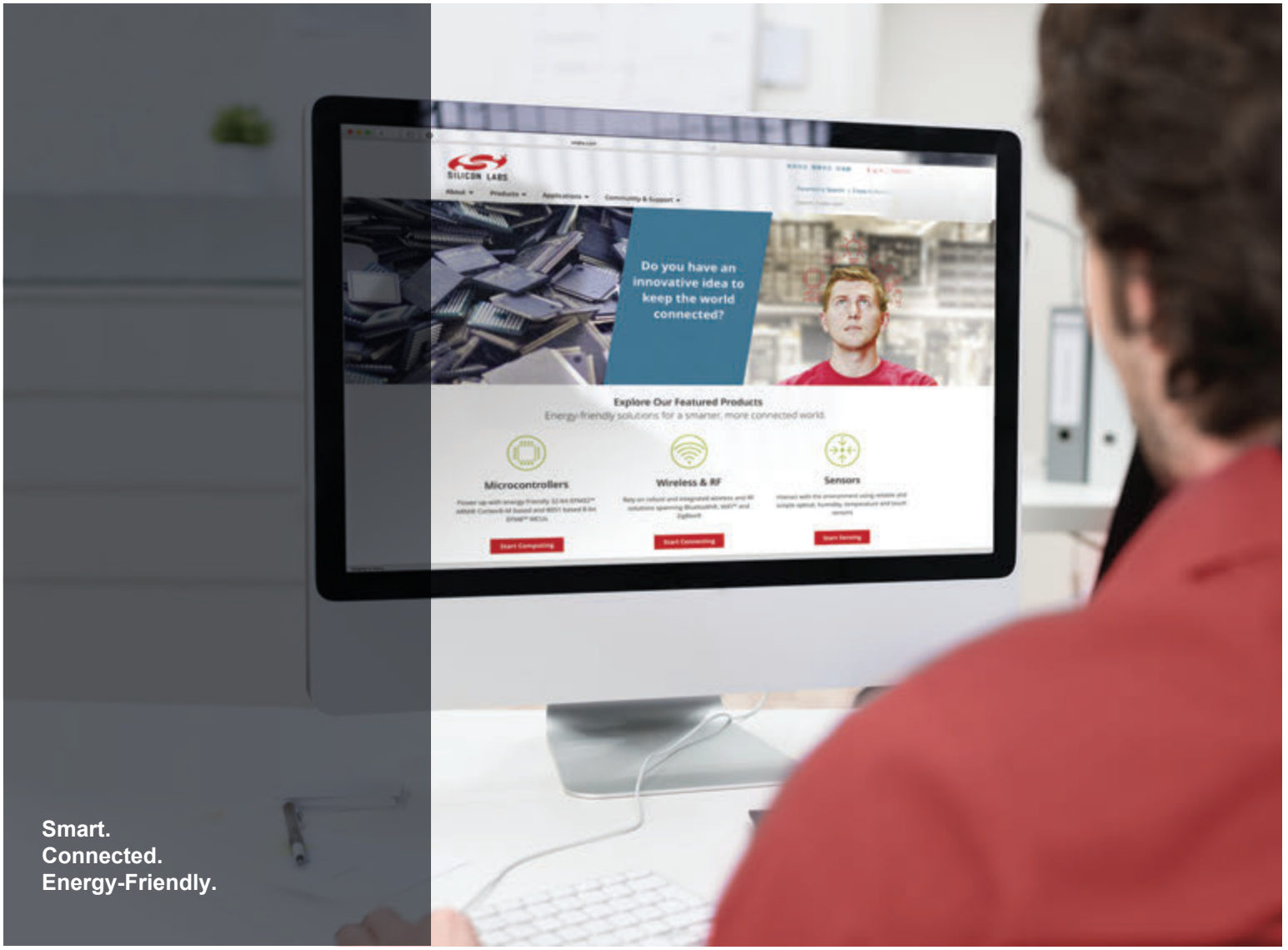
February 1, 2016

- Initial release.

9.2 Revision 0.9

June 30, 2017

- Updated 1. Electrical Specifications.
- Updated 5. Ordering Guide.
- Minor typo corrections.



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