User's Manual

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RL78/L1A Group

RPBRL78/L1A Promotion Board User's Manual

For e[2] studio

RENESAS MCU

RL78 Family / L1x Series

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- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The promotion board does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the demonstration application, how to use e[2] studio IDE to develop and debug software for the RPBRL78/L1A Promotion Board. It is intended for users designing code on the RPBRL78/L1A Promotion Board, using the many different incorporated peripheral devices.

The manual comprises of step-by-step instructions to load and debug a project in e[2] studio, but does not intend to be a complete guide to software development on the RPBRL78/L1A Promotion Board. Further details of the RL78/L1A microcontroller may be found in the RL78/L1A Group Hardware Manual and within the provided demonstration code.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RPBRL78/L1A Promotion Board. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the operation of the RPBRL78/L1A Hardware and software with information on direct drive of an LCD display.	RPBRL78/L1A Promotion Board User's Manual	R12UZ0011EG
Schematics	Circuit schematics of the board.	RPBRL78/L1A Promotion Board Schematics	R12UZ0008EG
Bill Of Materials	Parts list for the PCB Assembly	D014626_02_RPBRL78L1A_BOM	D014626_02
Hardware Layout	PCB layout	RPBRL78/L1A PCB Layout	R12UZ0009EG
Hardware Manual	Provides technical details of the RL78/L1A microcontroller.	RL78/L1A User's Manual: Hardware	R01UH0636EJ
RSK LCD Application Board V2 Schematics	Schematic for the RSK LCD Application board V2, compatible with RPBRL78/L1A	LCD Application Board V2 Schematics	REG99J0041
User's manual	Getting Started Guide for e[2] studio.	e[2] studio Integrated Development Environment User's Manual: Getting Started Guide	R20UT2771EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
ASCII	American Standard Code for Information Interchange
CSV	Comma Separated Variables
DAC	Digital-to-Analog Converter
DTC	Data Transfer Controller
E1 / E2 Lite	Renesas On-chip Debugging Emulator
ELC	Event Link Controller
ESD	Electro Static Discharge
HMI	Human-Machine Interface
IDE	Integrated Development Environment
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MCU	Micro-controller Unit
MUX	Multiplexed
PC	Personal Computer
Pmod™	This is a Digilent Pmod™ Compatible connector. Pmod™ is registered to Digilent Inc. Digilent-Pmod_Interface_Specification
RAM	Random Access Memory
ROM	Read Only Memory
RPB	Renesas Promotional Board
RTC	Real Time Clock
SPI	Serial Peripheral Interface
TAU	Timer Array Unit
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus

Table of Contents

1. Overview

1.1 Purpose

This promotion board is an evaluation tool for Renesas microcontrollers.

This manual describes the RPBRL78/L1A promotion board hardware and demonstration application.

2. Introduction

The RL78/L1A Family of microcontrollers are focused on analogue and low power applications together with integrated drive of segmented LCD displays. Particular features include:

- Analogue:
  - 12 bit ADC with up to 15 channels and a variety of operating modes.
  - 2 x 12 bit DACs.
  - 2 x Rail to rail, 1 x general purpose software controllable operational amplifiers.
  - 8 x software controllable analogue switches.
  - 3 x software controllable low resistance analogue switches.
  - Configurable voltage reference.
  - Analogue comparator.

- Low Power:
  - 3 low-power modes.
  - Selectable peripheral clocking.
  - Selectable main oscillator clock.

- CPU independent operations for Peripherals and Memory for Low Power and Improved Performance
  - Data Transfer Controller to perform memory transfer tasks independently of CPU.
  - Event Link Controller to operate peripherals independently of CPU.

The RPBRL78/L1A provides a hardware and embedded software platform to demonstrate the analogue capabilities of the RL78/L1A microcontroller. The integrated ADC, operational amplifier, comparator and analogue switches are used to create a simple oscilloscope function. This outputs a real-time sampled waveform to a colour display via a PMOD™ interface. The input signal to the oscilloscope section can be either from an external source or from a signal generator derived from an integrated DAC and operational amplifier, which provides a variety of user-configurable waveforms.

An on-board potentiometer and switch are used to control and configure the demonstration via an on-screen menu. Readings can also be fed back to the connected PC via a standard terminal application such as Putty or Tera-term by use of the on-board USB/Serial connection.

The RPBRL78/L1A also incorporates an integrated E2-Lite programmer/debugger to allow convenient access to the RL78/L1A MCU from a Renesas IDE such as e^2 studio.

There are various other options tracked into the RPBRL78/L1A PCB, which would require the user to solder the relevant components to the board to access:

- Footprint for a separate barrel-type 5V power supply connection, rather than the default USB-derived connection. This may be preferred for noise sensitive applications.
- A second PMOD™ connection. This is tracked to a different UART on the RL78/L1A device from the default one which is configured to connect to the display.
- Provision for a potentiometer to be connected to set the analogue trigger level of the oscilloscope application (R63), instead of the on-chip DAC.
- Header connection for a RSK LCD Application board to be connected in order to demonstrate the direct LCD segment drive capabilities of the RL78/L1A device.

2.1 Target Device

RL78/L1A 100pin LFQFP package, 128K/5.5K ROM/RAM, Part number R5F11MPGAFB

3. Operating the RPBRL78/L1A in Standalone Mode

3.1 Board Configuration and Operation

For standalone operation, the on-board E2-Lite programmer/debugger must be disabled. To achieve this, set switch SW1 as described in Figure 3-1.

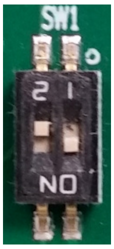
Standalone Operation	
SW1 position 1: ON SW1 position 2: OFF	

Figure 3-1 : Configuration of SW1 for Standalone Operation

The USB connection from the host PC should then be made to USB mini connector CN1. This supplies power to the board. The display will turn on and the main screen with the root-menu will be displayed, along with the current captured oscilloscope trace.

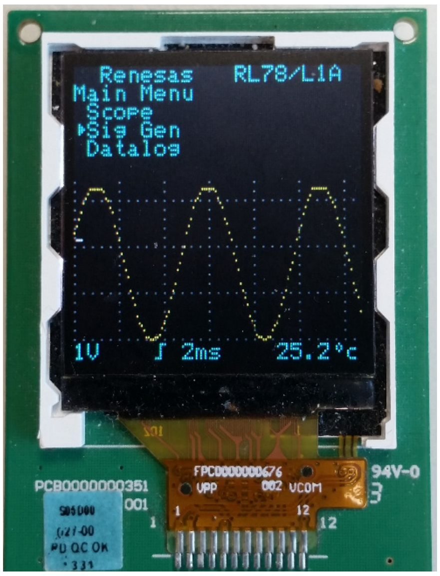


Figure 3-2: RPBRL78/L1A Main Menu

Use potentiometer R43 to move the menu selection pointer up and down and switch SW4 to activate the currently selected option. It is recommended to use the supplied shaft with the potentiometer for ease of adjustment.

3.2 Menu Structure

The following section describes the menu structure and the various options presented by them.

3.2.1 Main Menu

Scope	Opens sub-menu for oscilloscope configuration
Sig Gen	Opens sub-menu for Signal Generator configuration
Datalog	Opens sub-menu for Data Logging configuration

3.2.2 Scope Menu

Volts/Div	Opens sub-menu for adjusting the voltage per division of the oscilloscope
Timebase	Opens sub-menu for adjusting oscilloscope timebase
Trg Edge	Toggles the edge direction for oscilloscope trigger (default is positive going edge)
Trg Level	Adjusts the trigger level . Press switch SW4 again when required level selected
Back	Return to main menu

3.2.3 Scope\Volts/Div Menu

10mV	Set to 10mV per division
100mV	Set to 100mV per division
200mV	Set to 200mV per division
500mV	Set to 500mV per division
1V	Set to 1V per division
2V	Set to 2V per division
5V	Set to 5V per division
10V	Set to 10V per division
Back	Return to main menu

3.2.4 Scope\Timebase Menu

1ms	Set to 1ms per division
2ms	Set to 2ms per division
5ms	Set to 5ms per division
10ms	Set to 10ms per division
20ms	Set to 20ms per division
50ms	Set to 50ms per division
100ms	Set to 100ms per division
200ms	Set to 200ms per division
500ms	Set to 500ms per division
1sec	Set to 1 second per division
Back	Return to main menu

3.2.5 Sig Gen Menu

Waveform	Opens sub-menu for adjusting the signal generator waveform type
Amplitude	Adjusts the peak-to-peak amplitude of the waveform
Offset	Adjusts the offset of the waveform
Period	Opens sub-menu for adjusting the signal generator waveform period
Back	Return to main menu

3.2.6 Sig Gen\Waveform Menu

Sine	Sets the current signal generator waveform to be a sine wave
Triangle	Sets the current signal generator waveform to be a triangular wave
Square	Sets the current signal generator waveform to be a square wave
Back	Return to main menu

3.2.7 Sig Gen\Period Menu

2ms	Set to 2ms period
5ms	Set to 5ms period
10ms	Set to 10ms period
20ms	Set to 20ms period
50ms	Set to 50ms period
100ms	Set to 100ms period
200ms	Set to 200ms period
500ms	Set to 500ms period
1sec	Set to 1 second period
Back	Return to main menu

3.2.8 Datalog Menu

Start Log	Start data logging with current settings. Press reset button when in datalog mode to return to main menu.
Interval	Opens sub-menu for selecting the logging interval.
Sig Gen	Opens sub-menu for defining signal generator status in datalog mode.
Back	Return to main menu

3.2.9 Datalog\Interval Menu

1/2 Sec	Data logging at half second intervals
1 Sec	Data logging at second intervals
1 Min	Data logging at minute intervals
Back	Return to main menu

3.2.10 Datalog\Sig Gen Menu

Off	Signal Generator is disabled during data logging (to reduce current consumption)
On	Signal Generator is enabled.
Back	Return to main menu

4. Hardware Design

For detailed schematics, please refer to the schematic document as detailed in the overview section. Figure 4-1 below shows a block diagram of the hardware for the RPBRL78/L1A.

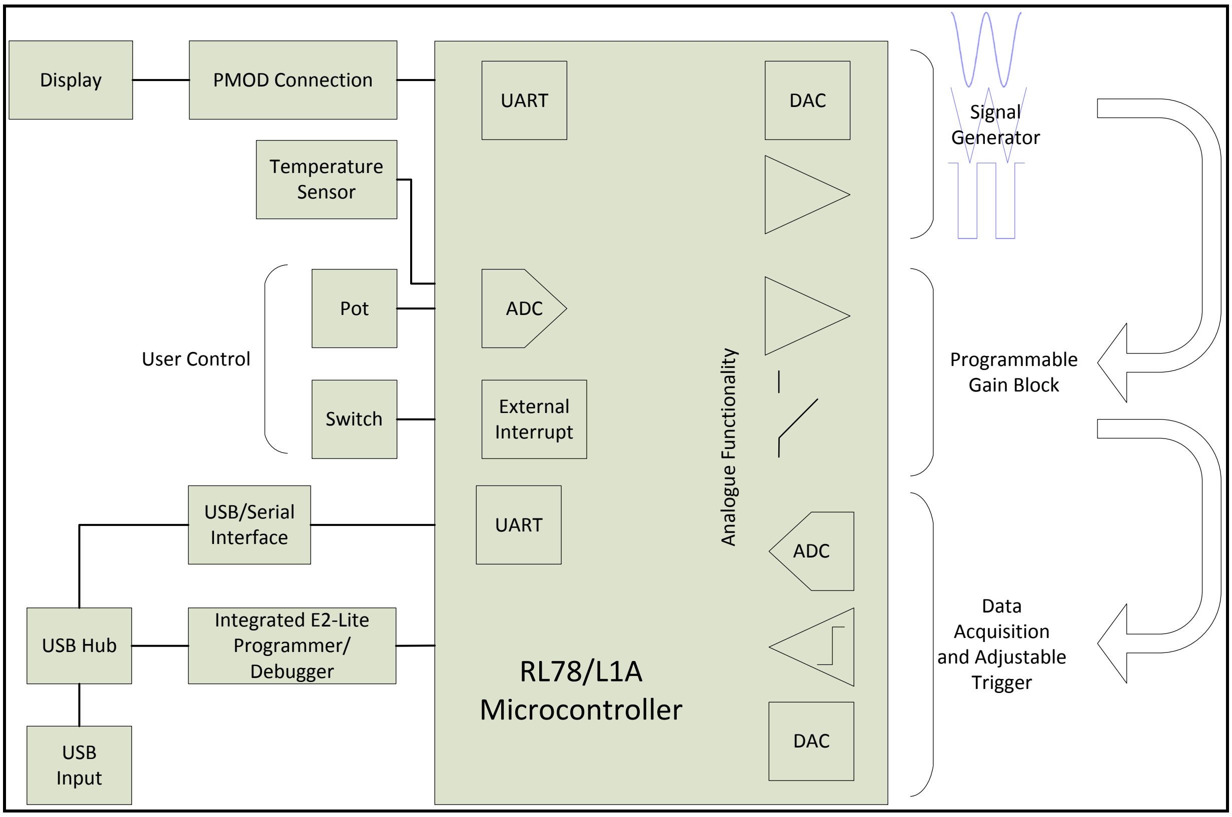


Figure 4-1 : Block Diagram of RPBRL78/L1A Hardware

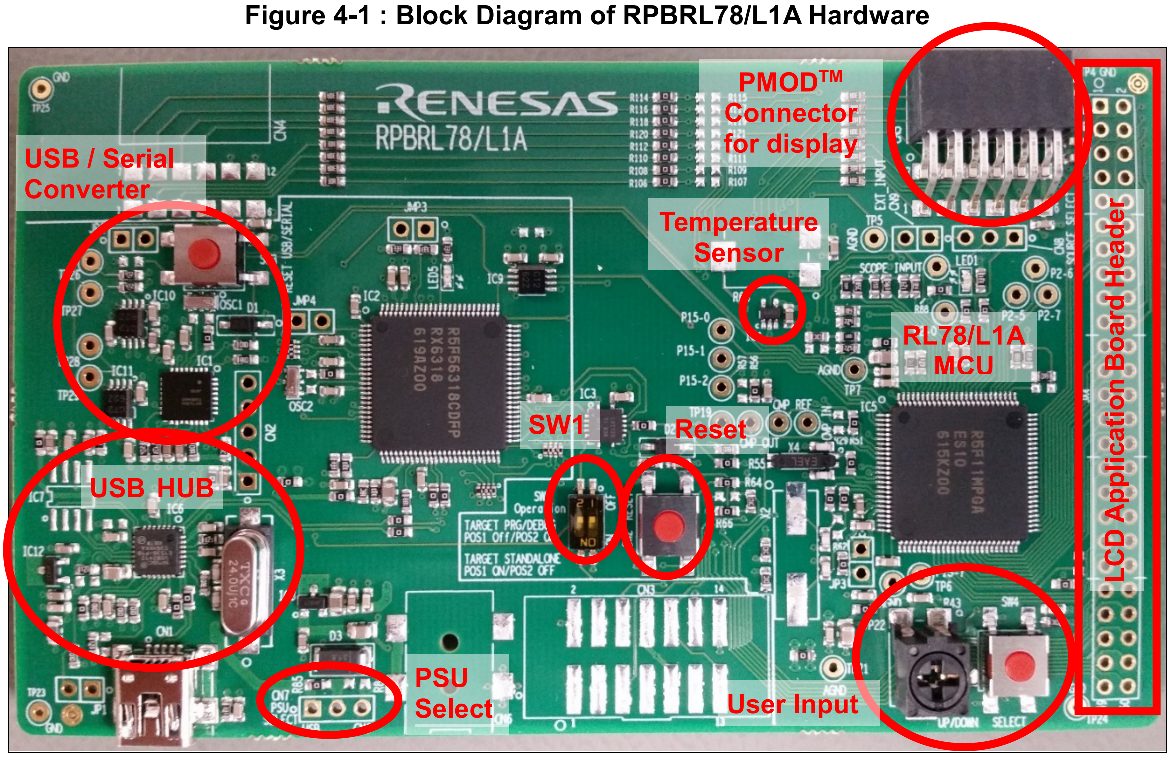


Figure 4-2 : RPBRL78/L1A Layout

4.1 USB Connection

The RPBRL78/L1A is connected to a PC and powered via a single USB connection. A Hub circuit is provided to allow a USB/Serial circuit and the integrated E2-Lite programmer/debugger to share the same USB connection. There is an option for a dedicated USB power management IC, MIC2026-2YM, at location IC7 to be fitted in order to provide supply protection and sequencing functions, but as default the 5V USB supply is provided to the downstream peripherals by 0603 size 0R links R76 and R75 for USB channels 1 and 2 respectively. If IC7 is fitted, then links R75 and R76 should be removed.

4.2 Power Supply

The USB Hub circuit is powered from the USB input via a 3.3V linear regulator, IC12, to provide the supply labelled in the schematic as 3V3_HUB. A separate 3.3V linear regulator, IC8, is provided to supply the microcontroller and associated circuitry. This is by default also fed from the USB input, by can be configured by jumper or link configuration (CN7, R84, R85) to be fed from a centre-positive barrel connector (CN6, part number kldx-smt2-0202-a, not fitted). This option has been made available for low noise applications.
The USB/Serial converter circuit is powered from the 5V supply USB_HUB_OUT2_5V, via link R75.

4.3 Integrated E2-Lite Programmer / Debugger

The RPBRL78/L1A board contains an integrated E2-Lite programmer debugger. The target RL78/L1A microcontroller can be debugged and programmed with this using the Renesas e[2] studio IDE or RFP programmer applications.
Switch SW1 on the PCB, as shown in Figure 4-2 on page 14, controls whether the E2-Lite is in programmer/debugger or standalone modes. Table 1 details the switch configuration for each mode. It is advised to power down the RPBRL78/L1A by removing the USB connection before making any changes to the operating mode.

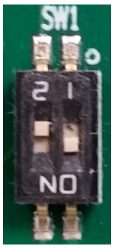
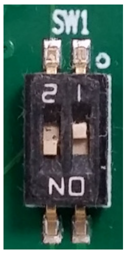
Standalone Operation	Programmer / Debugger Operation
SW1 position 1: ON SW1 position 2: OFF 	SW1 position 1: OFF SW1 position 2: ON 

Table 1: E2-Lite Configuration selection

4.4 USB/Serial Converter

An integrated USB/Serial converter is fitted to allow the target RL78/L1A microcontroller to communicate with the host PC via a terminal application such as PuTTY or Tera-Term. The circuit includes 3.3V / 5V logic level shifting and supports most common communication speeds. This connection is mapped to UART2 in the RL78/L1A microcontroller and RTS/CTS handshaking is brought out to ports 6-0 (pin 22) and 6-1 (pin 23) respectively, if required. There is also a reset button for the USB/Serial device, which will re-cycle the serial connection if pressed.
When the RPBRL78/L1A is connected to the host PC, with the correct driver installed, the RPBRL78/L1A is mapped to the next available COM port. See Figure 4-3 as an example of the COM port in Device Manager on the PC. The terminal application will need to be set to connect to this port for communication to be established.

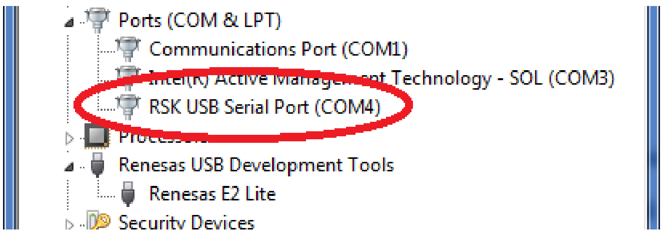


Figure 4-3 : USB/Serial Connection in Device Manager on PC

4.5 RL78/L1A Microcontroller

4.5.1 Programmer / Debugger Connections

The target RL78/L1A microcontroller, IC5, is connected by default to the integrated E2-Lite debugger. It is possible to reconfigure the board to connect to an external Renesas E1 or E2-Lite programmer/debugger connected to header CN3 (not fitted as standard). Table 2 below describes the hardware configurations for operation with the integrated debugger and the external debugger. If the board is reconfigured to external programmer/debugger operation, then switch SW1 should be set to put the integrated programmer/debugger into standalone mode. Refer to Table 1 above for details.

Integrated Debugger	External Debugger
CN3 : Header can be fitted or left open. R55 : Fit 0R Link (0603 resistor) R64 : Fit 0R Link (0603 resistor) R66 : Fit 0R Link (0603 resistor)	CN3 : fit header (Samtec SAM_HTST-107-01-X-DV) R55 : Open circuit R64 : Open circuit R66 : Open circuit

Table 2 : Configuration Details for Integrated or External Debugger

4.5.2 Clock Connections

The RPBRL78/L1A incorporates a crystal oscillator circuit for the main MCU oscillator. However it is expected that most applications will only require the use of the on-chip HOCO oscillator, so the crystal X2 is not fitted as standard. If a crystal is required then it is recommended to use a 20MHz 18pF crystal, part number 9C-20.000MAAJ-B from TXC.
A 32.768kHz crystal, X4, is provided for the low frequency oscillator, in order to facilitate low power modes and maintain accurate timing.

4.5.3 RL78/L1A MCU Supply Connections

The supply to the RL78/L1A MCU, IC5, is taken from the VCC3V3 supply, which is derived from the 5V input from the USB connection or the separate 5V supply, as configured. It is possible to measure the current consumption of IC5 by removing R62 and replacing it with an ammeter connection across JP3, to measure the current transferring from VCC3V3 to VCC_MCU supplies. The VCC_MCU supply connects the 3.3V supply to IC5's VDD pin (pin 21) as well as the analogue VDD pin (pin 99).
Please note that on no account should power be applied to the board when there is no connection on JP3 or R62 as it may then be possible to damage the MCU by back-feeding its supply.
Analogue circuitry has a separate supply and grounding arrangement. BOARD_AVCC is derived from VCC_3V3 from a single point through R94 and the analogue return is fed back through a single (star) point through R52, to minimize noise effects on analogue measurements and signals.

4.5.4 Temperature Sensor

The RPBRL78/L1A contains an integrated temperature sensor on board, MCP9700AT, IC4. This device produces a voltage linearly proportional to its ambient temperature. This voltage is fed to the MCU's ADC on channel 6 (P14-1, pin 89) where it is regularly sampled and a temperature reading derived accordingly.

4.5.5 User Controls

Inputs from the user are taken from the potentiometer R43, for up and down menu control and switch SW4, for user selection. The potentiometer is read on the MCU's ADC channel 5 (P14-0, pin 90). The reading, as a percentage of the full scale, is used to determine which menu item is currently highlighted by the user.
The momentary action switch, SW4 is connected to a hardware interrupt line INTP2, (P4-1, pin 12). This provides a interrupt to handle switch presses with a minimum of CPU intervention. The switch is used to determine the user's selection in the current menu.

4.5.6 PMOD™ Connectivity

The RPBRL78/L1A is distributed with a 128x128 colour display, which is driven from the PMOD™ connector on CN5. Communications between the MCU, IC5 and the PMOD™ display are made by the on-board UART2 peripheral, in SPI transmit only mode, plus various other signals to manage device select, reset and backlight control.

The connection of the display to the microcontroller is shown in Figure 4-4 and Table 3. Note that the pinout for the PMOD™ connector is not made in the standard fashion of left to right ascending, but ascending on the left then on the right, as per the PMOD™ standard.

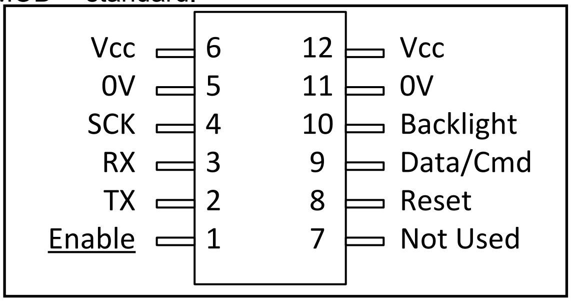


Figure 4-4 : Connection Diagram for PMOD™ display on CN5

CN5 PMOD™ Pin	Function	IC5 MCU Pin	IC5 MCU Pin function
1	Enable (Chip Select) (Active Low)	7	P13-0
2	TX	30	UART1 TXD1
3	RX (Not used on display)	31	UART1 RXD1
4	SCK	32	UART1 SCK1
7	Not used on display	36(Via link resistor R92)	P3-1
8	Reset	5	P15-4
9	Data/Cmd	4	P15-3
10	Backlight	88	P14-2

Table 3 : Connection Details for PMOD™ Display on CN5

There is space for a second PMOD™ connector to be fitted, to position CN4, part number Samtec part number SMH-106-02-T-D. This maps to UART3 on the RL78/L1A MCU, IC5. Connection details are shown in Table 4. **Bold** type indicates the default resistor link connection.

CN4 PMOD™ Pin	Function	IC5 MCU Pin	IC5 MCU Pin function	Resistor Link Configuration	
				Fit Link	Remove Link
1	uncommitted	66	P0-3	**R112**	R113
2	TX	67	UART3 TXD3	**R110**	R111
3	RX	68	UART3 RXD3	**R108**	R109
4	SCK	69	UART3 SCK3	**R106**	R107
5	0V				
6	3.3V (Vcc)				
7	uncommitted	48	P5-5	**R114**	R115
8	uncommitted	47	P5-6	**R116**	R117
9	uncommitted	46	P5-7	**R118**	R119
10	uncommitted	45	P7-0	**R120**	R121
11	0V				
12	3.3V (Vcc)				

Table 4 : Connection Details for PMOD™ Connector CN4

4.6 Signal Generator

The RL78/L1A microcontroller is configured to use 12-bit DAC channel 0 and rail-to-rail operational amplifier channel 0 to provide a signal generator function for the oscilloscope section to capture and display.
The output signal from the DAC is buffered by the rail-to-rail operational amplifier, channel 0 before being made available for measurement by the oscilloscope section. Figure 4-5 shows the electrical connectivity for the signal generator. The output from the signal generator is made available on test point P2-0 (before the op-amp buffer). The signal is available on header CN8 (Not fitted) pin 1.

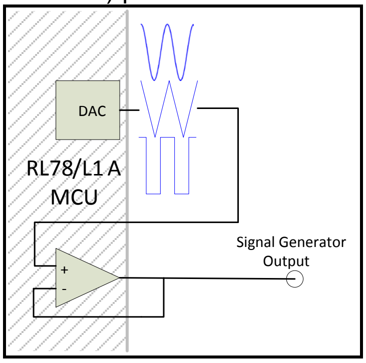


Figure 4-5 : RL78/L1A Based Signal Generator Scheme

4.7 Oscilloscope

4.7.1 Operation

The oscilloscope section applies a switchable analogue gain of x100, x10, x5, x2, x1, x0.5, x0.2, x0.1 to the input waveform. It is comprised of the rail-to-rail op-amp channel 1, the corresponding analogue and low-resistance switches to achieve the switchable gain input stage to the 12-bit ADC. Figure 4-6 shows a graphical representation of this.
The resistors and low-resistance switches on the positive input to the op-amp provide variable attenuation to the input signal. The resistors and multiplex analogue switches connected between inverting input and output of the op-amp provide variable gain to the input signal. It is with careful resistor value selection that the various combinations of switches can be applied to achieve the desired gain values. It should also be noted that the ADC measurement of the signal is taken from different channels connected on the switch side of the op-amp output, as required to minimize error resulting from the on-state resistance of the analogue multiplexer switches which can be up to 1kΩ in value.

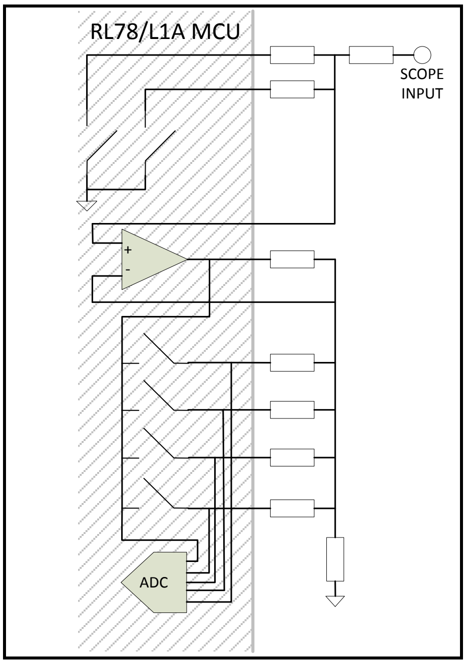


Figure 4-6 : Switchable Gain Input Stage

Triggering for the oscilloscope is achieved by the analogue comparator, with DAC channel 1 to provide a variable threshold to trigger the data acquisition sequence. The trigger direction, low-to-high, high-to-low or window, is configurable in software. Figure 4-7 details the connection scheme.

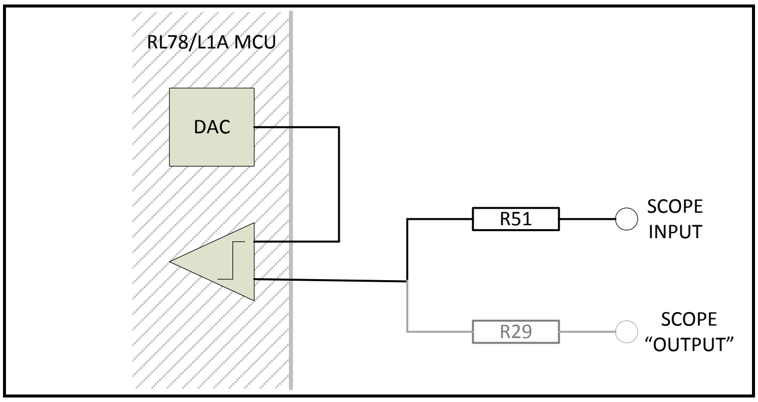


Figure 4-7 : Oscilloscope Triggering Scheme

The input to the trigger is connected to the input to the oscilloscope section by default, before the op-amp circuit. There is an option to use the output of the op-amp as the trigger input if required. The reason for this being connected to the input is to remove any errors to the trigger level caused when the op-amp output is being measured from one of the analogue switch pins rather than the op-amp output pin.
If the RPBRL78/L1A is reconfigured to monitor an external signal on the external input header CN9 then it is recommended to use the oscilloscope output as the trigger level rather than the input, in order to prevent any voltages greater than 3.3V being applied to the trigger input. In the source code, the #define SCOPE_TRIGGER_FROM_OUTPUT in file userdefine.h should be made active. Refer to Table 5 for details. **Bold** type indicates the default configuration.

Trigger from Op-Amp Input	Trigger from Op-Amp Output
R51 : Fit 0R Link (0603 resistor)	R51 : Open circuit
R29 : Open circuit	R29 : Fit 0R Link (0603 resistor)
Comment out the #define SCOPE_TRIGGER_FROM_OUTPUT in userdefine.h	Enable the #define SCOPE_TRIGGER_FROM_OUTPUT in userdefine.h

Table 5 : Connection Details for Optional Potentiometer to Control Trigger Level

There is also provision on the PCB for a potentiometer, R63, to provide the variable trigger level to the operational amplifier. This would enable the DAC to be turned off, to save power in the microcontroller. This option is not fitted by default. Refer to Table 6 for the connection details. **Bold** type indicates the default configuration.

DAC Controlled Oscilloscope Triggering	Pot Controlled Oscilloscope Triggering
R56 : Fit 0R Link (0603 resistor)	R56 : Open circuit
R57 : Open circuit	R57 : Fit 0R Link (0603 resistor)
R63 : Not required	R63 : Fit 10K Pot (Piher part number N6L50T7S-103R)

Table 6 : Connection Details for Optional Potentiometer to Control Trigger Level

4.7.2 Configuration of Oscilloscope Input

The oscilloscope can be set to read the signal generator output or an external signal. By default, the oscilloscope is configured to read the output from the signal generator, hardwired by 0R Link R88. The external signal can be connected to a 2-way header connected to CN9, and a 3-way header CN8 (not fitted as default) can be used to select between the 2 signal sources. It is also recommended to use the op-amp output as the trigger input to the comparator also. In the source code, the #define SCOPE_TRIGGER_FROM_OUTPUT in file userdefine.h should be made active.
Table 7 summarises the connections required. **Bold** type indicates the default configuration.

Signal Generator as Input Source	External Signal on CN9 as Input Source
R51 : Fit 0R Link (0603 resistor)	R51 : Open circuit
R29 : Open circuit	R29 : Fit 0R Link (0603 resistor)
R88 : Fit 0R Link (0603 resistor) OR	R88 : Open circuit
Fit Header CN8 and Link pins 1-2 by jumper	Fit Header CN8 and Link pins 2-3 by jumper Fit Header CN9 and connect external source to this.
Comment out the #define SCOPE_TRIGGER_FROM_OUTPUT in userdefine.h	Enable the #define SCOPE_TRIGGER_FROM_OUTPUT in userdefine.h

Table 7 : Connection Details for Optional Potentiometer to Control Trigger Level

5. Embedded Firmware Application

5.1 Overview

The application code for the RPBRL78/L1A is designed to showcase the analogue and low power capabilities of the RL78/L1A microcontroller and to provide an easy to use Human-Machine Interface (HMI).

Specifically the code is required to:

- Provide an easily navigable menu structure using the PMOD™ display and the potentiometer and switches.
- Control DAC channel 0 and op-amp channel 0 to provide a configurable signal generator function.
- Control low resistance analogue switches and analogue multiplexer switches for op-amp 1 in order to achieve the variable analogue gain oscilloscope input stage.
- Drive DAC channel 1 and analogue comparator to implement the oscilloscope triggering function.
- Display the acquired voltage waveform on the PMOD™ display, in real-time.
- Implement a low power data-logging mode which periodically samples the input signal and transmits the voltage reading to a terminal application on a PC, via UART.

The application code also demonstrates the use of the DTC and ELC peripherals to perform complex tasks independently of the CPU. This allows the CPU to be doing other things, or to be put into low power modes.

The Data Transfer Controller DTC allows the transfer of memory from one location to another, based upon hardware events. For example, the completion of an ADC sample could trigger a DTC to send the result to a UART for transmission, or append the result to a buffer. DTC operations can also be chained together so a single event can initiate a sequence of operations automatically. Given that all the peripherals on the microcontroller are configured and started by registers in memory, it is possible to use the DTC to operate peripherals in fairly complicated ways, all without CPU involvement.

The Event Link Controller allows the completion of an operation of a peripheral to trigger the start of another one. For example the interval interrupt of a timer to start the acquisition of an ADC. This also adds to the flexibility available for CPU independent event handling and processing.

5.2 General Application Configuration

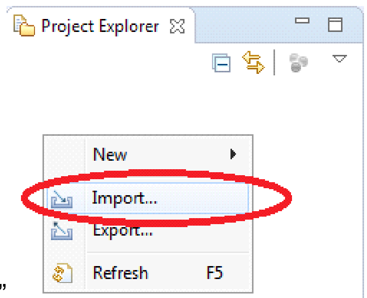
The target device is the RL78/L1A 100pin LFQFP package, with 128K/5.5K ROM/RAM, Part number R5F11MPGAFB.

The application project is designed to operate using the e^2 studio IDE, version 5.2. The toolchain is Renesas CCRL version 1.03. See the Renesas website in order to obtain these tools. A basic working knowledge of working with the e^2 studio IDE is assumed.
The project is configured to be programmed/debugged via the E2-Lite programmer/debugger as embedded in the board.

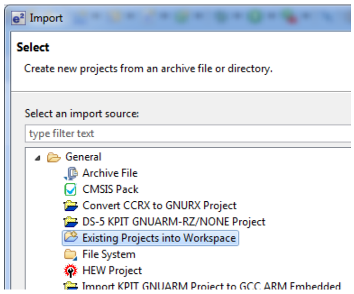
5.3 Importing the Application into e^2 studio

The application project is made available as an archive file, which needs to be imported into the e^2 studio workspace.
This is achieved as follows:

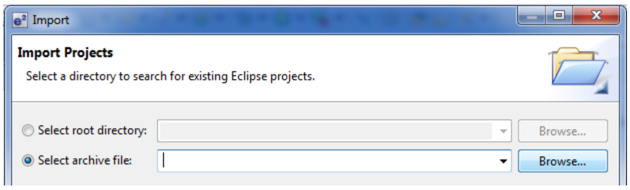
1. Right-click within the Project Explorer pane and select “Import…”



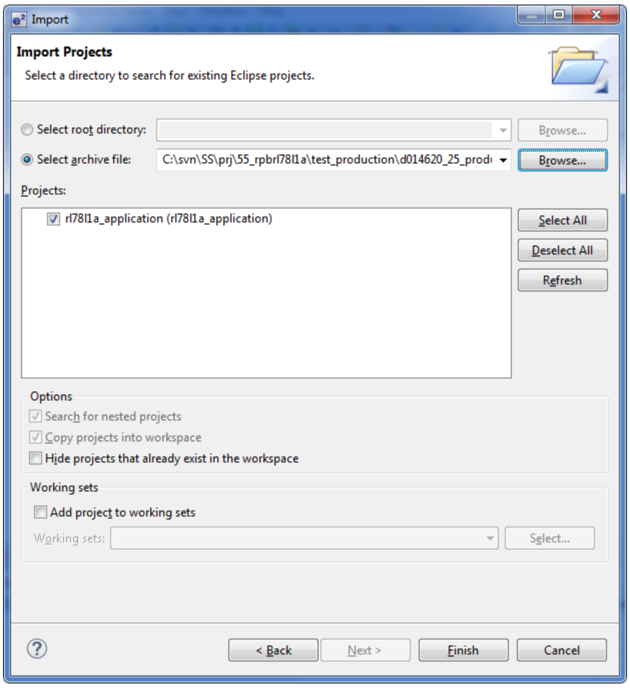
2. In the Import window, expand the “General” folder and select “Existing Projects into Workspace” then click “Next >”



3. Tick the “Select archive file” radio button and then “Browse…”



4. Select the archive file. The project will be shown on the import window:



5. Click the “Finish” button to complete the import.

6. A notification may appear stating that the toolchain path has been modified. In this case click "OK" to continue.

5.4 Running the Application Code

5.4.1 Running in Debugger Mode with Embedded E2-Lite

In order to run in debug mode the embedded E2-Lite debugger must be enabled using switch SW1. Figure 5-1 shows the correct switch settings.

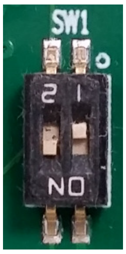
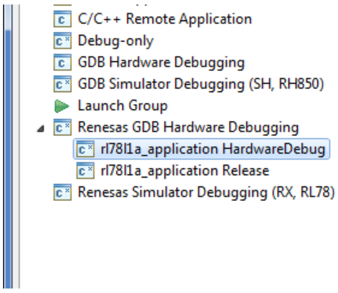
SW1 position 1: OFF	
SW1 position 2: ON	

Figure 5-1 : SW1 Setting for Debug Mode

The desired build configuration (HardwareDebug or Release) can then be programmed into the target device in e^2 studio by first connecting the RPBRL78/L1A to the host PC, then selecting “Run” then “Debug Configurations…” from the menu bar. Select the desired configuration then press the “Debug” button.



The project will then be loaded onto the target device and the user will be able to run or step through the application code by pressing the  button to run or the step buttons  or  on the toolbar.

5.4.2 Running in Standalone Mode

In order to run in standalone mode the embedded E2-Lite debugger must be disabled using switch SW1. Figure 5-2 shows the correct switch settings. The application can then be run by re-applying the input power or by pressing the reset button SW2.

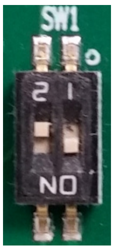
SW1 position 1: ON	
SW1 position 2: OFF	

Figure 5-2 : SW1 Setting for Standalone Mode

5.5 Project Configuration

The application code runs the RL78/L1A microcontroller from the internal HOCO (High speed On Chip Oscillator) set to 24MHz frequency. This is because of its quick stabilization time and that absolute accuracy of the CPU clock was not the main requirement, as there is a 32.768kHz RTC oscillator in circuit for that purpose.

5.6 Signal generator

5.6.1 Waveform Creation

The basic waveform pattern for each waveform type is stored in FLASH memory. The working waveform buffer is located in RAM and is defined by a combination of the selected waveform pattern (sine, triangular or square), scaling factor and offset values determined by the user in real-time.

When a change is made to the any of these parameters by the user, the waveform buffer is recalculated, using the algorithm shown in Figure 5-3. The DTC action has to be turned off when this recalculation is performed.

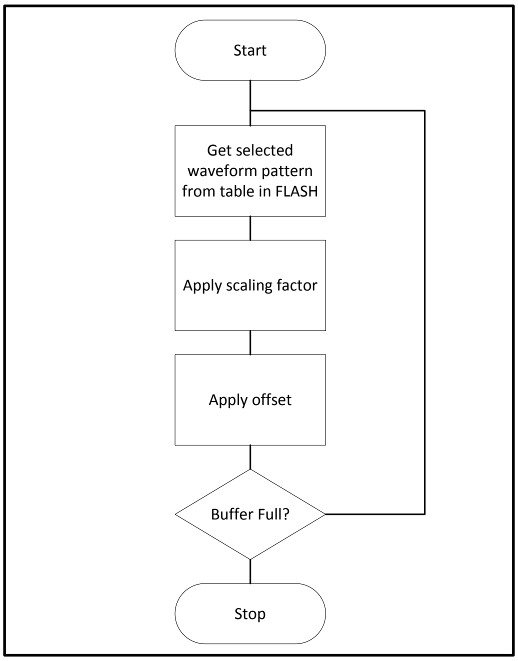


Figure 5-3 : Flowchart for waveform pattern buffer

5.6.2 Transfer of Waveform to DAC

The signal generator uses DAC channel 0 to provide the variable analogue voltage, op-amp channel 0 to buffer the output of the DAC and the timer array unit 0 channel 0 to schedule the changes to the output at regular intervals defined by the timebase of the signal generator. The Data Transfer Controller (DTC) peripheral is used to update the DAC when the timer interval interrupt occurs. This means that the signal generator operation is achieved without CPU involvement, reducing its workload. See Figure 5-4 for a graphical representation.

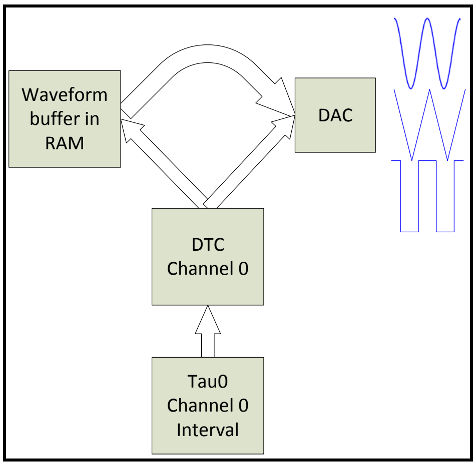


Figure 5-4 : DTC Scheme for Signal Generator

The signal generator source code is located in the file waveforms.c. The waveform sent to the DAC by the DTC is from a buffer in RAM, 64 x 16-bit words in size. The DTC operation requires that this buffer is located at an absolute address, specified by the #define “WAVEFORM_BUFFER_LOCATION”.

The source code to set up the DTC is located in the file dtc.c. DTC 0 is used for the transfer of the waveform information to the DAC. For detailed information concerning the operation of the DTC peripheral, refer to the RL78/L1A User’s manual - hardware.

DTC 0 is triggered by timer array unit 0 channel 0 interrupt, which occurs at regular intervals dictated by the timebase set for the signal waveform. The DTC vector (at offset 19 in the dtc vector table) for the TAU0 channel 0 interval interrupt is set to use the control data stored at 40Hex offset from the DTC base address. This control data defines how the DTC behaves when the DTC event occurs. See Figure 5-5 for a graphical representation.

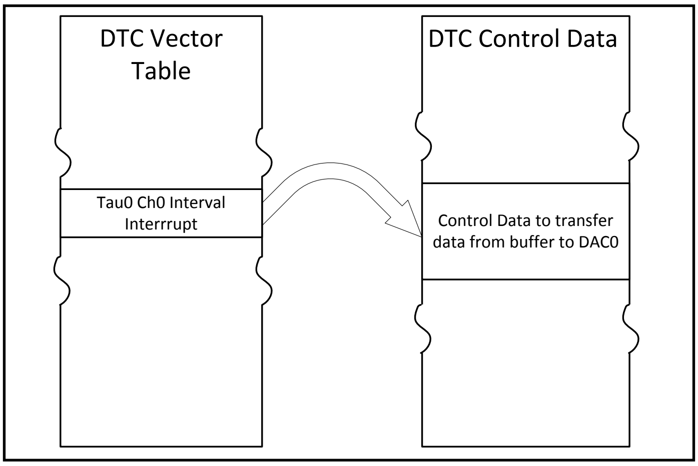


Figure 5-5 : DTC Event Handling

DTC 0 is configured to run with a data size of 16bits, incrementing the source address after each transfer (stepping through the buffer) and passing the current value from the buffer to the DADR0 register, which sets the output value of the DAC channel 0. The address of the DADR0 register is specified by the #define “DAC_VALUE_REGISTER_LOCATION”. It is also set to repeat mode so once it has stepped through the block size of 64 words, it automatically starts from the buffer start location again. This minimizes the necessary CPU interaction to just starting and stopping the transfer action.

5.6.3 Op-amp Buffer

The output of the DAC is passed through an on-chip rail-to-rail op-amp, channel 0, configured as a buffer, to present the signal generator as a low impedance voltage source. The op-amp is turned on and configured as software triggered (as opposed to being triggered by Event Link Controller or ADC) in the op-amp driver code in files r_opamp.c and opamp_wrapper.c.

5.7 Oscilloscope

The oscilloscope section consists of the input gain control, ADC, acquisition and display stages.

5.7.1 Input Gain Control Stage

The input gain stage hardware consists of the rail-to-rail op-amp channel 1, the associated MUX analogue switches MUX10-MUX13 and Low Resistance Analogue Switches AMP0OPD and AMP1OPD. Figure 5-6 shows the hardware scheme.

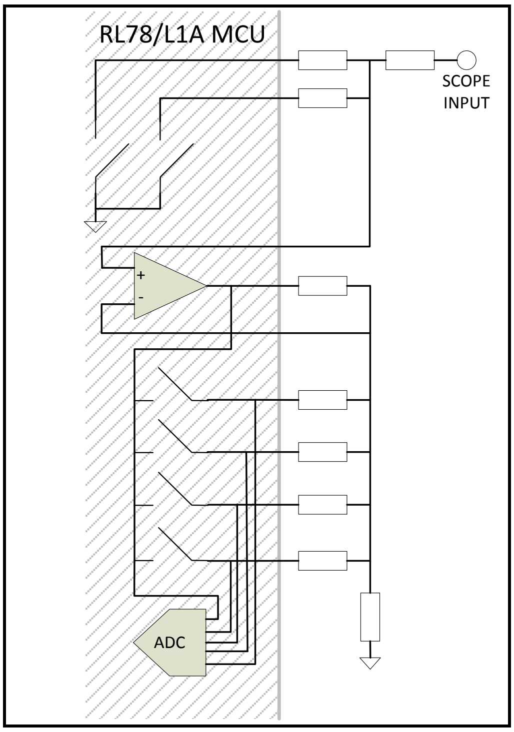


Figure 5-6 : Switchable Gain Input Stage

The op-amp channel 1 and the MUX switches are initialised in the main_user_init function in main.c, which calls the appropriate driver functions in r_opamp.c and opamp_wrapper.c for the op-amp and r_mux.c and mux_wrapper.c for the multiplex switches.

The control of the op-amp gain is carried out in the file oscilloscope.c. The function scope_set_switches selects the appropriate switch combinations for each gain setting.

5.7.2 ADC

The 12-bit, 15 channel successive approximation ADC on the RL78/I1A microcontroller is responsible for reading the oscilloscope input voltage with the correct gain applied, the external temperature sensor on channel ANI6 and also the potentiometer R43 (ANI5) to sample the user control input.

Please refer to the User's Manual - Hardware section 12 for detailed information on the ADC and its operating modes. In this application, the ADC is configured to perform in single scan mode, a group scan of selected channels each time an ADC read is performed.

When an oscilloscope trace is not being recorded, the system is waiting for a trigger. During this time the potentiometer R43 must still be measured, to allow the user input on the potentiometer to function correctly. In this case, the ADC acquisition is controlled in software by the function "scope_read_pot_and_temp" in oscilloscope.c, which is called at regular intervals from within the main background loop.

The driver for the ADC, in r_adc.c and adc_wrapper.c, starts the ADC measurement, acquires the readings and the ADC conversion complete interrupt function sets a flag to inform when the acquisition of the group samples is complete.

Depending upon the gain setting for the input gain op-amp circuit, different analogue channels are selected for the measurement result. This is because the on-state resistance of the MUX switches on the RL78/L1A can be up to 1kΩ in value and therefore may introduce a significant error in the reading. In order to compensate for this error, the measurement can be taken from the ADC channel connected on the MUX switch of the activated channels. Taking the reading on this side of the switch removes the switch impedance of the gain calculation. This is shown in Figure 5-7.

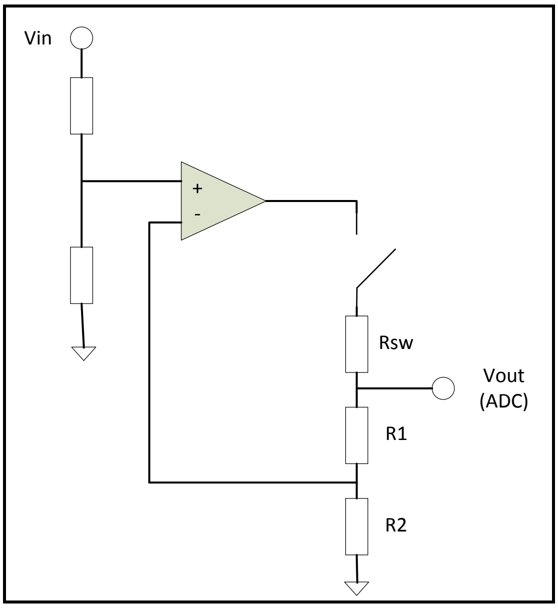


Figure 5-7 : Compensation for MUX On-State Switch Impedance

For gain settings where there are more than one MUX channel connecting resistors from the inverting input to the output of the op-amp, the ADC channel connected to the resistor with the lowest error is selected. This will be dependent upon the individual resistor values present.

5.7.3 Triggering and Data Acquisition

The ADC samples the current acquisition channel, user-control pot and temperature sensor at regular intervals triggered by software, in background, when it is waiting for a trigger for the acquisition of the oscilloscope trace.

The oscilloscope operation uses the analogue comparator peripheral to trigger the acquisition of an oscilloscope “trace”. A trace consists of a sequence of 128 samples of the input signal, taken at intervals of the selected timebase. This acquisition is sequenced by a combination of the Data Transfer Controller (DTC) and Event Link Controller (ELC) peripherals in the RL78/L1A microcontroller. This reduces the workload on the CPU and facilitates reduced power consumption.

Figure 5-8 shows the configuration of the DTC and ELC peripherals. When the comparator interrupt occurs, the DTC starts the first ADC acquisition and then follows a sequence of chained operation directly after this: The second step is to start the TAU0 channel 1 timer (by transferring the appropriate start value to the start register for the timer). This timer is then used to trigger successive regular ADC samples. The third step is to disable the comparator to prevent re-triggering during trace acquisition. The fourth step is to set a variable to a specific value to let other software processes know that the acquisition is in progress and the ADC cannot be used or reconfigured in any way during this time.

The ELC is configured to start an ADC conversion automatically each time the TAU0 channel 1 timer interval interrupt occurs. This implements the regular acquisition of data from the oscilloscope.

Finally a separate DTC operation is triggered by the availability of new sample data on the ADC. This DTC automatically appends the new sample to the trace buffer. Once the required number of samples (128) have been collected, this DTC operation completes, the normal software ADC interrupt occurs and the software then handles the newly acquired buffer of 128 ADC samples.

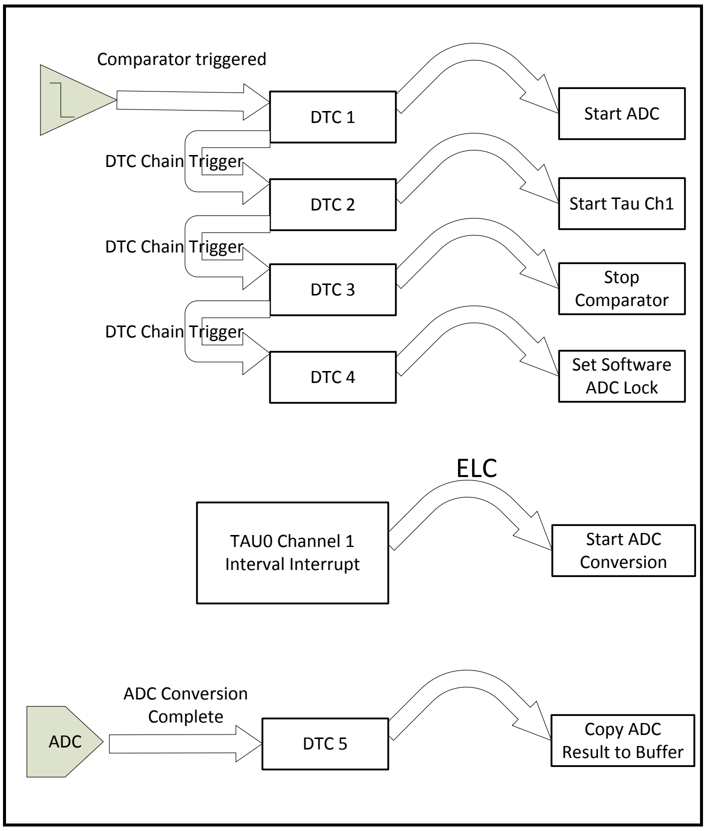


Figure 5-8 : DTC and ELC Configuration for Trace Capture Sequence

Figure 5-9 shows the timeline of the sample acquisition sequence in a graphical form.

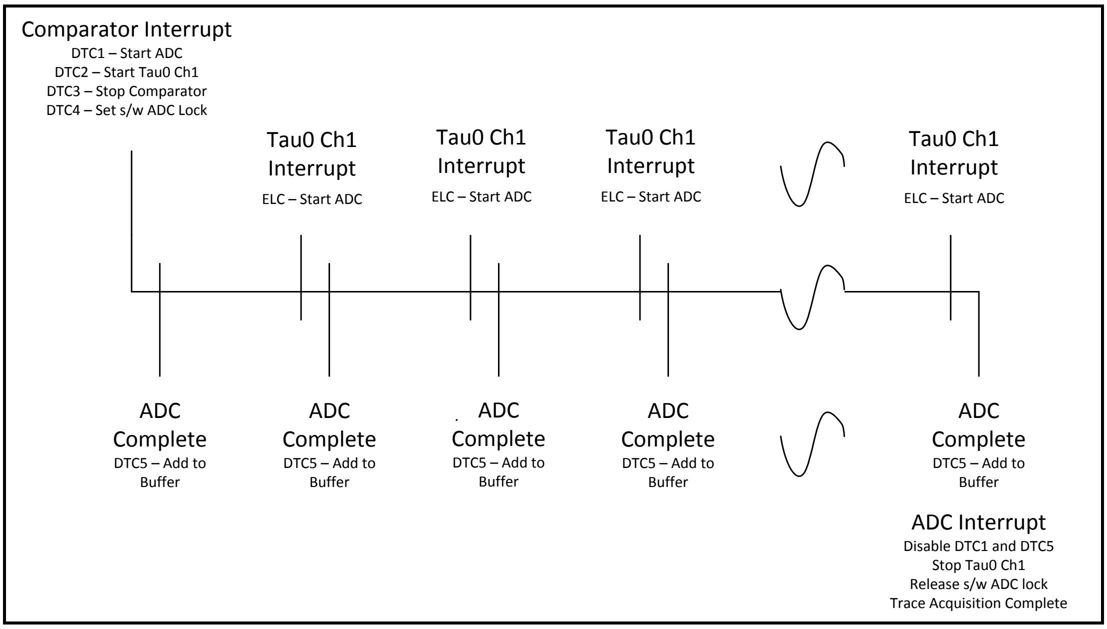


Figure 5-9 : Data Acquisition Timeline

5.7.4 Trace Display

Once the trace has been acquired, it is then displayed in the grid on the PMODTM display connected to PMODTM connector CN5. This operation follows in background, called by the function scope_handle_trace_acquisition in oscilloscope.c. This rescales the trace buffer from ADC values to voltages in mV. It then calls the function display_trace which loops through each x-co-ordinate on the display, removing the pixel from the previous trace (with the grid colour if the pixel is overlapping the oscilloscope grid on the display) before placing the new one.

5.8 Data Logging Mode

The application incorporates a data-logging mode, where at periodic intervals the unit will wake from STOP mode, enable the op-amp circuit, take a reading, convert the result to mV and then output it to a terminal program on the host PC via the UART2 and the USB/Serial link. Communication is made at 115200 baud, 8 data bits, 1 stop bit, no parity, no handshaking. The interval, controlled by the RTC, can be set to ½ second, 1 second or 1 minute.

The data acquisition process is shown in Figure 5-10.

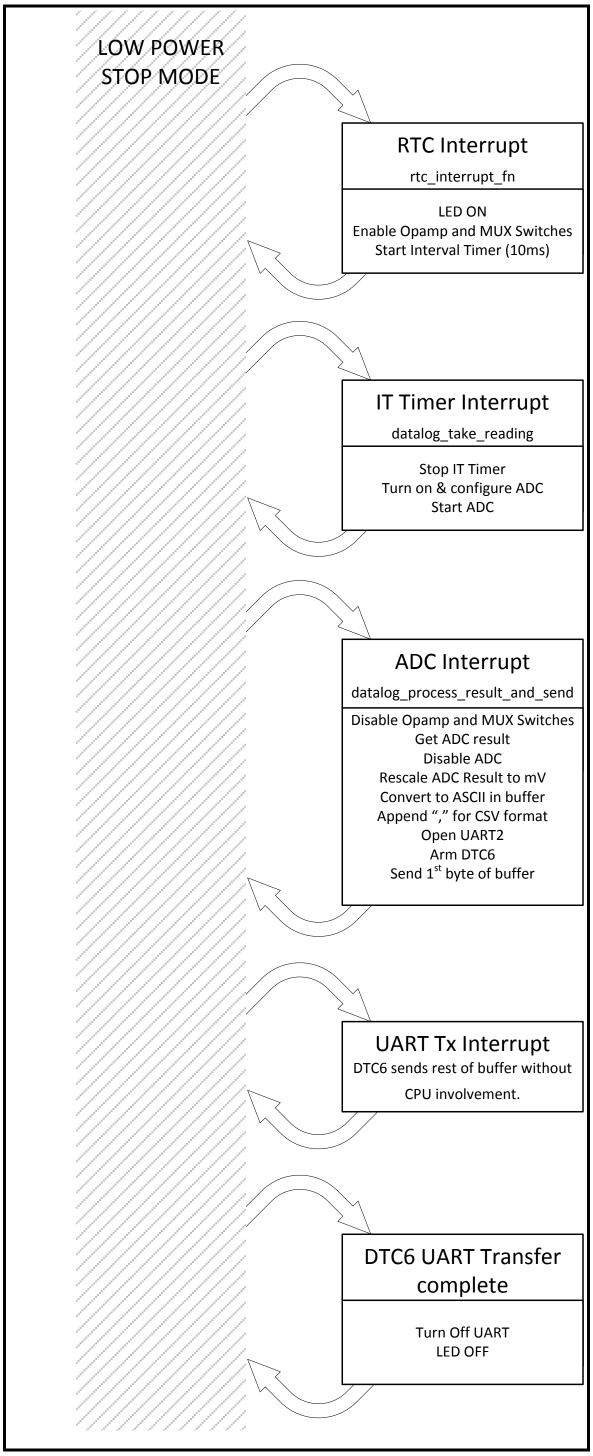


Figure 5-10 : Data Logging Process Workflow

The source code to run the datalog mode is located in the file datalog.c. The RTC interrupt starts the data acquisition process, by activating the op-amp circuit and starting the interval timer, which is set to 10ms to allow for the stabilisation time of the op-amp and analogue switch circuits. When the interval time has expired, the interval timer interrupt then enables, configures and starts the ADC conversion. When the ADC conversion complete interrupt occurs, the ADC, op-amp and analogue switches are turned off. The result is then re-scaled to a voltage value in mV and converted to ASCII format in a buffer, with a comma being appended for the CSV format of the data to be sent by UART. The UART and DTC channel 6 are enabled. DTC 6 is configured to transfer data from the buffer to the UART transmit register, triggered by the UART transmit complete interrupt. Once the data in the buffer has been transmitted, the UART Tx complete interrupt is called which then disables the UART to minimize current consumption until the next RTC interrupt occurs.

5.9 Human Machine Interface

The application provides a simple to use menu system for the user to configure and operate the oscilloscope demonstration. The code for this is located in menu.c. As a general principle, the value of the pot determines which item in the current menu is highlighted (to be selected) and an arrow is put on the display to point to this. The potentiometer thresholds for the menu items vary, proportionally to the number of items in the menu. For example, if there are 2 items, the threshold will be at (ADC Full Scale) / 2. If there are 4 items, the thresholds will be at ¼, ½ and ¾ of the full scale ADC result. If the menu is not the root menu, the last menu item will be “Back”. The switch SW4, selects the currently highlighted option.

The contents of the menus are located in menu_items.c. The menus created from arrays of menu elements, which are structs that define the menu item’s on-screen text, whether the destination is a sub-menu or a function and a pointer to the sub-menu or function. Selecting an option either runs the function pointed to or updates the current menu to the selected sub-menu and refreshes the menu display.

6. Direct Segment Drive LCD

The RPBRL78/L1A is designed to allow a Renesas RSK LCD Application Board V2 to be connected to it on a 50-way, dual-row standard 0.1 inch pitch socket (not fitted as standard) at location JA4. This allows the RPBRL78/L1A to demonstrate direct-drive of an LCD display. Please refer to the RL78/L1A User's Manual : Hardware, Chapter 19 LCD Controller/Driver for further details on driving the LCD display.

Figure 6-1 shows the segment numbering of the display. Table 8 shows the mapping of the MCU pins on the RPBRL78/L1A to the LCD pins and segments of the LCD fitted to the LCD Application Board. MCU pins that cannot map to the LCD Application board are shown in pink colour. MCU pins that have dual connectivity with the second PMOD™ connection CN4 are shown in yellow colour. These are by default configured to connect to the PMOD™. See Table 8 for the resistor links to fit and remove for these connections.

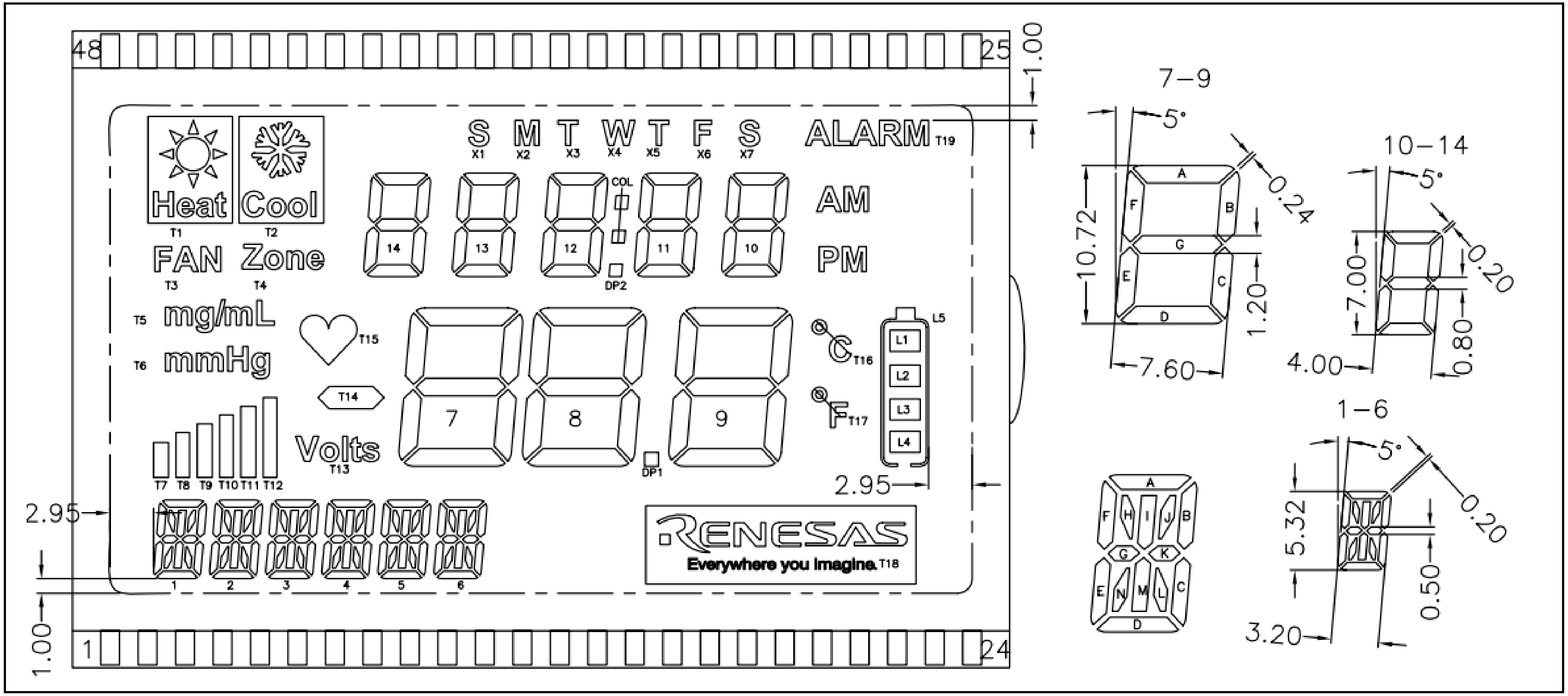


Figure 6-1 : Segmented LCD Display on LCD Application Board

Display Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
COM1	COM1				1H	1A	2H	2A	3H	3A	4H	4A	5H	5A	6H	6A	7F	7A	8F	8A	9F	9A	L5	L1
COM2		COM2			1I	1J	2I	2J	3I	3J	4I	4J	5I	5J	6I	6J	7G	7B	8G	8B	9G	9B	PM	L2
COM3			COM3		1N	1M	2N	2M	3N	3M	4N	4M	5N	5M	6N	6M	7E	7C	8E	8C	9E	9C	T16	L3
COM4				COM4	1D	1L	2D	2L	3D	3L	4D	4L	5d	5L	6D	6L	T14	7D	T18	8D	DP1	9D	T17	L4
JA4 Pin	1	2	3	4			11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PCB Link - Fit													R115	R117	R119	R121								
PCB - Remove													R114	R116	R118	R120								
MCU Pin	26	27	29	28			54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37
MCU Seg							SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19	SEG20
MCU Port			P12-5					P5-0	P5-1	P5-2	P5-3	P5-4	P5-5	P5-6	P5-7	P7-0	P7-1	P7-2	P7-3	P7-4	P7-5	P7-6	P7-7	P3-0

Display Pin	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
COM1	AM	10D	X5	11D	X4	DP2	12D	X1	13D	T1	14D	T2	T15	T13	T4	T3	T5	T6	T12	T11	T10	T9	T8	T7
COM2	T19	10C	10E	11C	11E	COL	12C	12E	13C	13E	14C	14E	6B	6F	5B	5F	4B	4F	3B	3F	2B	2F	1B	1F
COM3	X7	10B	10G	11B	11G	X3	12B	12G	13B	13G	14B	14G	6K	6G	5K	5G	4K	4G	3K	3G	2K	2G	1K	1G
COM4	X6	10A	10F	11A	11F	X2	12A	12F	13A	13F	14A	14F	6C	6E	5C	5E	4C	4E	3C	3E	2C	2E	1C	1E
JA4 Pin	29	30	31	32	33	34	35	36	37	38			41	42	43	44	45	46	47	48	49	50		
PCB Link - Fit													R107	R109	R111	R113								
PCB - Remove													R106	R108	R110	R112								
MCU Pin	36	35	34	33	57	56	55	74	73	72			69	68	67	66	65	64	63	62	71	70		
MCU Seg	SEG21	SEG22	SEG23	SEG24	SEG0	SEG1	SEG2	SEG28	SEG29	SEG30			SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39	SEG40	SEG31	SEG32		
MCU Port	P3-1	P3-2	P3-3	P3-4				P1-3	P1-4	P1-5			P0-0	P0-1	P0-2	P0-3	P0-4	P0-5	P0-6	P0-7	P1-6	P1-7		

Display Segment Not connected

Display Segment Connection shared with PMOD™ CN4

Table 8 : Mapping of MCU SEG pins to LCD App Board

The LCD drive power connections are shown in Figure 6-2. The capacitors used are 470nF ceramic capacitors with X7R dielectric. These can be reconfigured if required in order to implement the desired drive method. For further details, please refer to the RL78/L1A User's Manual : Hardware, Chapter 19 LCD Controller/Driver.

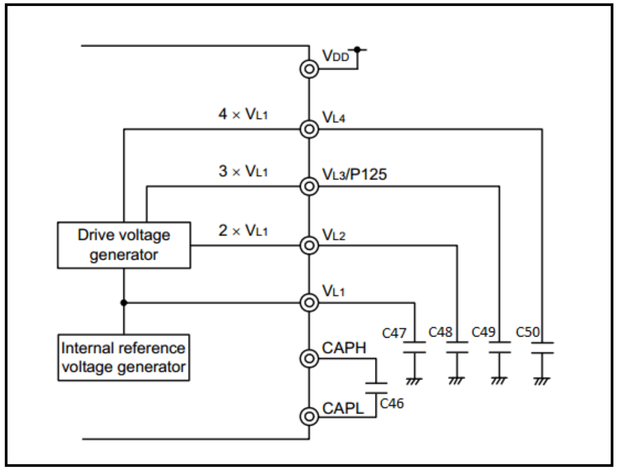
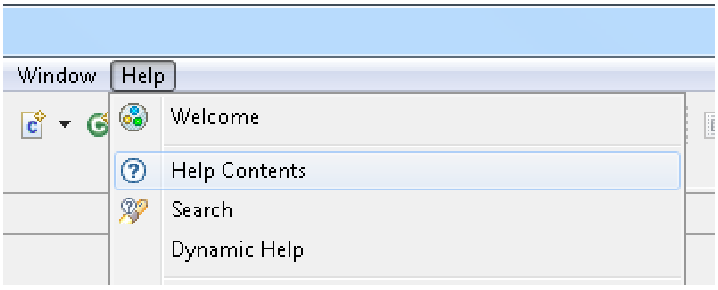


Figure 6-2 : LCD Drive Capacitor Connections

7. Additional Information

Technical Support

For details on how to use e^2 studio, refer to the help file by opening e^2 studio, then selecting Help > Help Contents from the menu bar.



For information about the RL78/L1A Group microcontrollers refer to the RL78/L1A Group Hardware Manual.

For information about the RL78 assembly language, refer to the RL78 Family Software Manual.

Online technical support and information is available at: www.renesas.com/RPB-RL78-L1A

Technical Contact Details

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Global & Japan: https://www.renesas.com/support/contact.html

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