3-Channel, Very Low Power Video Amplifiers with EDTV Filters and 6-dB Gain

FEATURES

- **Very Low Total Quiescent Current: 3.4 mA at 3.3 V**
- **0.15-μA Total Disabled Supply Current**
- **Third-Order Butterworth Low-Pass Filters:**
  –1 dB at 17 MHz
  –3 dB at 20 MHz
  21-dB Attenuation at 43 MHz
  Supports 480p/576p $Y'P'_BP'_R$ or R'G'B' Video
  Supports CVBS, S-Video, 480i/576i $Y'P'_BP'_R$, or Y'U'V' in Oversampled Systems
- **DC-Coupled Input with 150-mV Output Shift**
- **Built-in 6-dB Gain (2 V/V)**
- **+2.6-V to +5-V Single-Supply Operation**
- **Rail-to-Rail Output Allows AC or DC Output Coupling**
- **Low Differential Gain/Phase of 0.05%/0.03°**
- **Ultra-Small, MicrostarCSP™ 9-Ball Package**
  - **Tiny PCB Area: 1,5 mm × 1,5 mm**
  - **Very Low Profile Height: 0,45 mm (max)**

APPLICATIONS

- **Personal Media Players**
- **Digital Cameras**
- **Cellular Phone Video Output Buffering**
- **USB/Portable Low-Power Video Buffering**

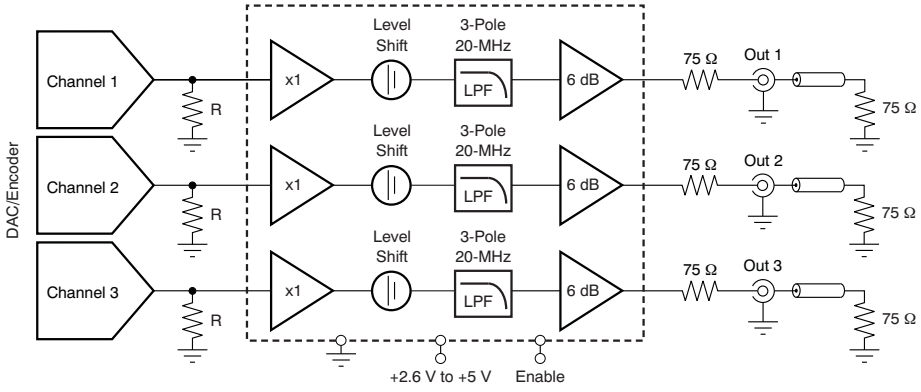
DESCRIPTION

Fabricated using the revolutionary, complementary Silicon-Germanium (SiGe) BiCom3X process, the THS7319 is a very low-power, 2.6-V to 5-V single-supply, three-channel, integrated filter video buffer. This device is ideal for battery-powered applications where size and power are critical parameters. Total quiescent current is only 3.4 mA at 3.3 V and can be reduced to 0.15 μA while disabled.

The THS7319 incorporates three enhanced definition (ED) filter channels with third-order Butterworth characteristics. These filters are useful as digital-to-analog converter (DAC) reconstruction filters or as analog-to-digital converter (ADC) anti-aliasing filters supporting 480p/576p $Y'P'_BP'_R$ and R'G'B' video. The THS7319 is also ideal for oversampled systems that produce standard-definition (SD) signals including CVBS, S-Video, 480i/576i $Y'P'_BP'_R$, Y'U'V', and R'G'B'.

The THS7319 is designed for dc-coupled inputs. To mitigate any DAC/encoder termination interaction, the input impedance is a very high 2.4 MΩ. The 150-mV output level shift allows for a full sync dynamic range at the output with a 0-V input that prevents sync crushing. The rail-to-rail output stage supports both ac and dc line driving.

The THS7319 is offered in a RoHS-compliant ultra-small MicrostarCSP 9-ball package.



Single-Supply DC-Input/DC-Output Coupled Video Line Driver

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	TRANSPORT MEDIA, QUANTITY	ECO STATUS(2)
THS7319IZSVT	MicrostarCSP 9-Ball	ZSV	Small Tape and Reel, 250	Pb-Free, Green
THS7319IZSVR			Tape and Reel, 3000	

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) These packages conform to Lead (Pb)-free and green manufacturing specifications. Additional details including specific material content can be accessed at www.ti.com/leadfree.
GREEN: TI defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight. N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree. Pb-FREE: TI defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		THS7319	UNIT
Supply voltage, V_{S+} to GND		5.5	V
Input voltage, V_I		–0.4 to V_{S+}	V
Output current, I_O		±75	mA
Continuous power dissipation		See Dissipation Ratings Table	
Maximum junction temperature, any condition(2), T_J		+150	°C
Maximum junction temperature, continuous operation, long-term reliability(3), T_J		+125	°C
Storage temperature range, T_{STG}		–65 to +150	°C
ESD rating:	Human body model (HBM)	2000	V
	Charge device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING(1) (T_J = +125°C)	
			AT T_A = +25°C	AT T_A = +85°C
MicrostarCSP 9-Ball (ZSV)	100	250(2)	400 mW	160 mW

(1) Power rating is determined with a junction temperature of +125°C. This temperature is the point where performance starts to degrade and long-term reliability starts to be reduced. Thermal management of the final printed circuit board (PCB) should strive to keep the junction temperature at or below +125°C for best performance and reliability.
(2) These data were measured with the JEDEC High-K test PCB. For the JEDEC low-K test PCB, θ_{JA} is +550°C/W.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{S+}	2.6		5	V
Ambient temperature, T_A	–40		+85	°C

ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7319			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
AC PERFORMANCE						
Passband bandwidth	–0.1 dB; relative to 1 MHz		11		MHz	C
	±1 dB; relative to 1 MHz	14	17		MHz	A
–3-dB bandwidth	Relative to 1 MHz	17	20		MHz	B
Normalized stop band gain	f = 43 MHz, relative to 1 MHz		–21	–12	dB	A
	f = 54 MHz, relative to 1 MHz		–27		dB	C
Group delay	f = 100 kHz		19		ns	C
Group delay variation	f = 11 MHz, relative to 1 MHz		4		ns	C
Channel-to-channel delay			0.3		ns	C
Differential gain	NTSC/PAL		0.05		%	C
Differential phase	NTSC/PAL		0.03		°	C
Total harmonic distortion	f = 1 MHz, V_O = 2 V_{PP}		–81		dB	C
Signal-to-noise ratio	100 kHz to 13.5 MHz, non-weighted		69		dB	C
	100 kHz to 13.5 MHz, unified weighting		79		dB	C
Rise/fall time	V_{OUT} = 2-V step		20		ns	C
Slew rate	V_{OUT} = 2-V step		80		V/µs	C
Output impedance	f = 12 MHz		1.3		Ω	C
	f = 12 MHz, return loss		41		dB	C
	Disabled		20 || 3		kΩ || pF	C
Crosstalk	f = 5 MHz		–54		dB	C
DC PERFORMANCE						
Biased output voltage	V_{IN} = 0 V	110	150	250	mV	A
Input voltage range	Linear dc input, limited by output		–0.06/1.5		V	C
Input bias current		–1000	–130	–40	nA	A
Input resistance			2.4 || 2		MΩ || pF	C
Voltage gain		1.99	2.01	2.03	V/V	A
Gain matching	Channel-to-channel	–1	±0.14	+1	%	A

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation only. **(C)** Typical value only for information.

ELECTRICAL CHARACTERISTICS: V_{S+} = +3.3 V (continued)

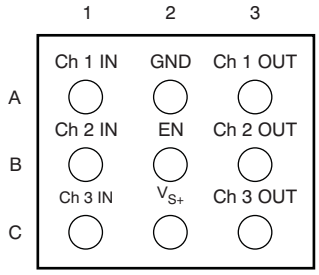
At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS7319			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX		
OUTPUT CHARACTERISTICS						
High output voltage swing	R_L = 150 Ω to GND	2.85	3.1		V	A
Low output voltage swing	R_L = 150 Ω to GND		0.01		V	C
Output current	Short-circuit		70		mA	C
POWER SUPPLY						
Operating voltage		2.5	3.3	5.5	V	B
Total quiescent current, no load	Enable pin = 3.3 V, no load, V_{IN} = 0 V	2.7	3.4	4.5	mA	A
	Enable pin = 0 V, no load, V_{IN} = 0 V		0.15	1	µA	A
Power-supply rejection ratio (PSRR)	At dc	46	51		dB	A
LOGIC CHARACTERISTICS(2)						
V_{IH}	Enabled	2	1.8		V	A
V_{IL}	Disabled		0.7	0.65	V	A
I_{IH}	Enable pin = 3.3 V		0.1	1	µA	A
I_{IL}	Enable pin = 0 V		0.1	1	µA	A
Disable time			80		ns	C
Enable time			100		ns	C

(2) The logic input pin (Enable pin) should not be left floating. It must be connected to logic low (or GND) or logic high (or V_{S+}).

PIN CONFIGURATION

ZSV PACKAGE
MicrostarCSP 9-BALL
(TOP VIEW)



ZSV PACKAGE
MicrostarCSP 9-BALL
(TOP VIEW)

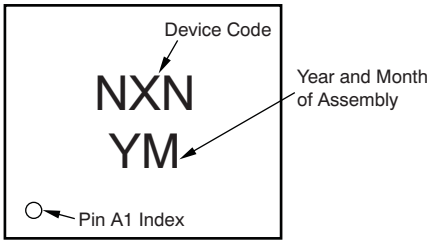
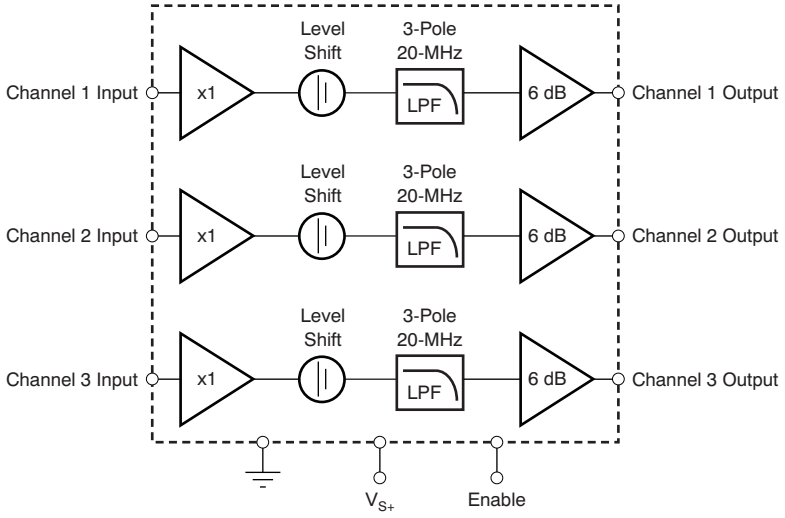


Table 1. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
Channel 1 Input	A1	I	Video input, channel 1
GND	A2	I	Ground pin for all internal circuitry
Channel 1 Output	A3	O	Video output, channel 1
Channel 2 Input	B1	I	Video input, channel 2
Enable	B2	I	Enable pin. Logic high enables the THS7319; logic low disables the THS7319. This pin must not be left floating.
Channel 2 Output	B3	O	Video output, channel 2
Channel 3 Input	C1	I	Video Input, channel 3
V_{S+}	C2	I	Positive power-supply pin; connect to +2.6 V or +5 V.
Channel 3 Output	C3	O	Video output, channel 3

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

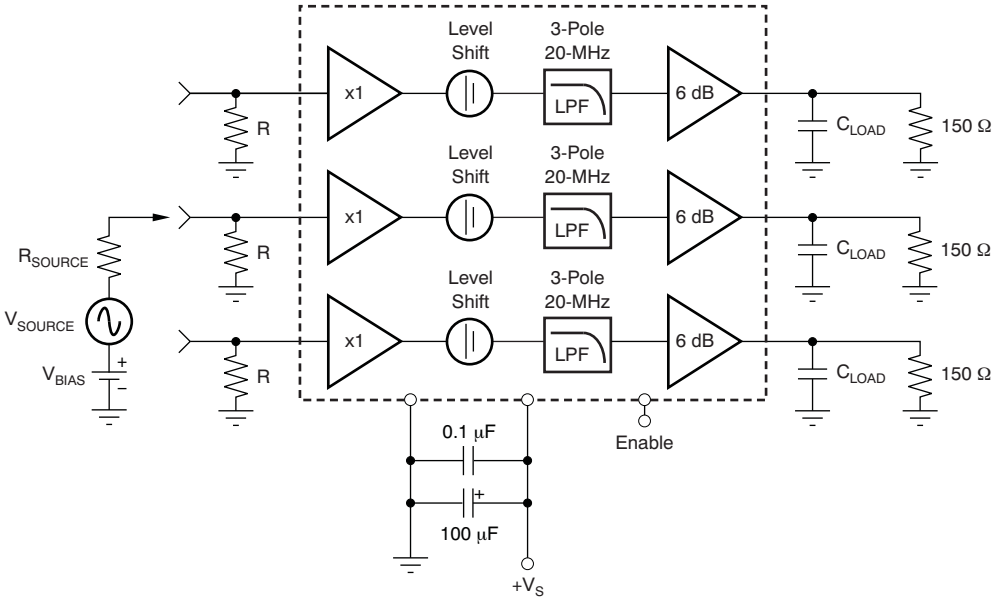


Figure 1. Standard Test Circuit

Table of Graphs: V_{S+} = 2.6 V

TITLE	FIGURE
Signal Gain vs Frequency	Figure 2, Figure 3
Phase vs Frequency	Figure 4
Group Delay vs Frequency	Figure 5
Small-Signal Frequency Response vs Capacitive Loading	Figure 6
Crosstalk vs Frequency	Figure 7
Second-Order Harmonic Distortion vs Frequency	Figure 8
Third-Order Harmonic Distortion vs Frequency	Figure 9
Small-Signal Pulse Responses vs Time	Figure 10
Large-Signal Pulse Responses vs Time	Figure 11
Slew Rate vs Output Voltage	Figure 12
Enable/Disable Response vs Time	Figure 13

Table of Graphs: V_{S+} = 3.3 V

TITLE	FIGURE
Signal Gain vs Frequency	Figure 14, Figure 15
Phase vs Frequency	Figure 16
Group Delay vs Frequency	Figure 17
Small-Signal Frequency Response vs Capacitive Loading	Figure 18
Crosstalk vs Frequency	Figure 19
Second-Order Harmonic Distortion vs Frequency	Figure 20
Third-Order Harmonic Distortion vs Frequency	Figure 21
Small-Signal Pulse Responses vs Time	Figure 22
Large-Signal Pulse Responses vs Time	Figure 23
Slew Rate vs Output Voltage	Figure 24
Enable/Disable Response vs Time	Figure 25
Input Bias Current vs Temperature	Figure 26
Output Offset Voltage vs Temperature	Figure 27
Maximum Output Voltage vs Temperature	Figure 28
Attenuation at 14 MHz vs Temperature	Figure 29
Attenuation at 43 MHz vs Temperature	Figure 30

Table of Graphs: V_{S+} = 5 V

TITLE	FIGURE
Signal Gain vs Frequency	Figure 31, Figure 32
Phase vs Frequency	Figure 33
Group Delay vs Frequency	Figure 34
Small-Signal Frequency Response vs Capacitive Loading	Figure 35
Crosstalk vs Frequency	Figure 36
Second-Order Harmonic Distortion vs Frequency	Figure 37
Third-Order Harmonic Distortion vs Frequency	Figure 38
Small-Signal Pulse Responses vs Time	Figure 39
Large-Signal Pulse Responses vs Time	Figure 40
Slew Rate vs Output Voltage	Figure 41
Enable/Disable Response vs Time	Figure 42

Table of Graphs: General

TITLE	FIGURE
Differential Gain vs Supply Voltage	Figure 43, Figure 44
Total Quiescent Current vs Temperature	Figure 45
Output Impedance vs Frequency	Figure 46
S22 Output Reflection Ratio vs Frequency	Figure 47
Disabled Output Impedance vs Frequency	Figure 48

TYPICAL CHARACTERISTICS: V_{S+} = 2.6 V

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

SIGNAL GAIN vs FREQUENCY

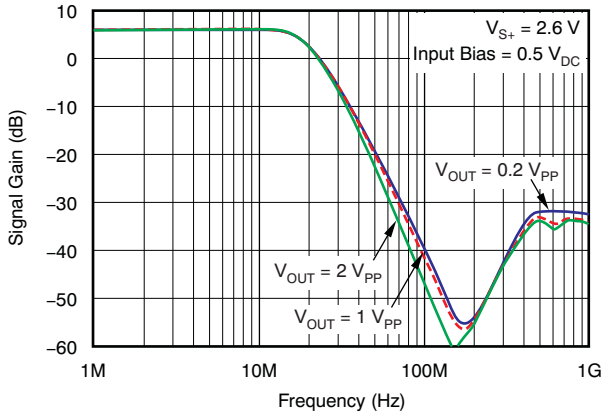


Figure 2.

SIGNAL GAIN vs FREQUENCY

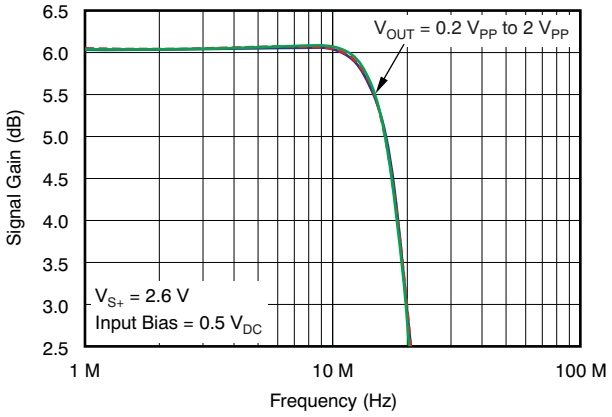


Figure 3.

PHASE vs FREQUENCY

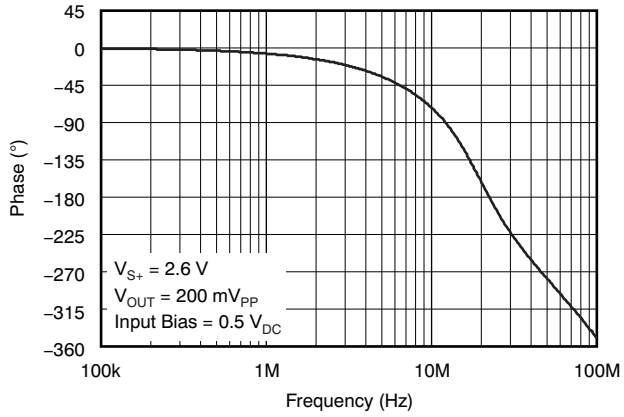


Figure 4.

GROUP DELAY vs FREQUENCY

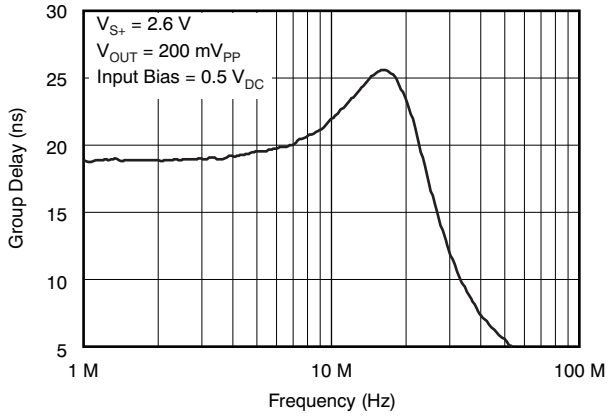


Figure 5.

SMALL-SIGNAL FREQUENCY RESPONSE vs CAPACITIVE LOADING

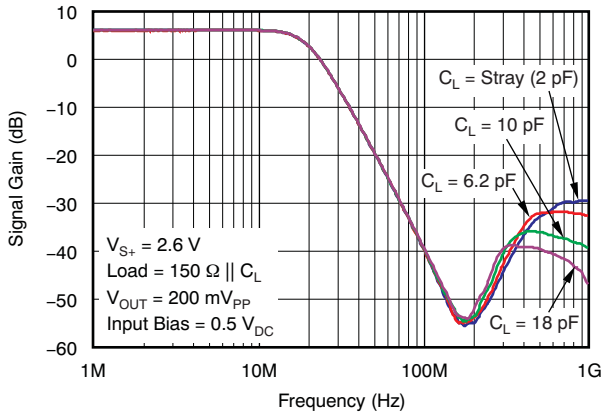


Figure 6.

CROSSTALK vs FREQUENCY

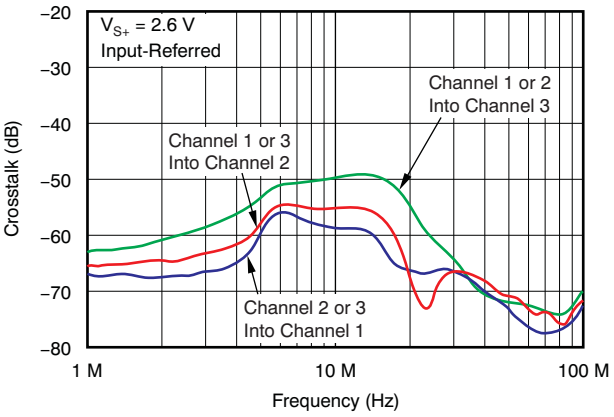


Figure 7.

TYPICAL CHARACTERISTICS: V_{S+} = 2.6 V (continued)

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

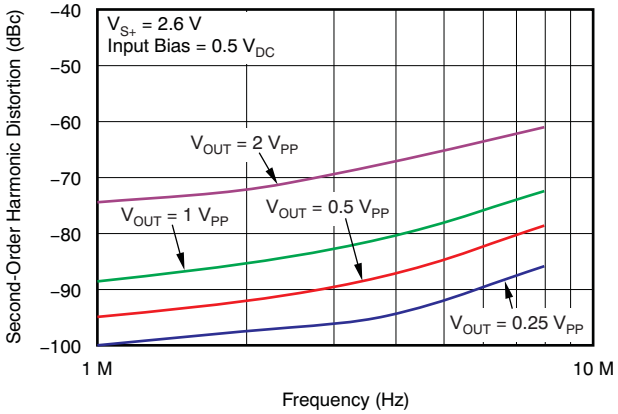


Figure 8.

THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

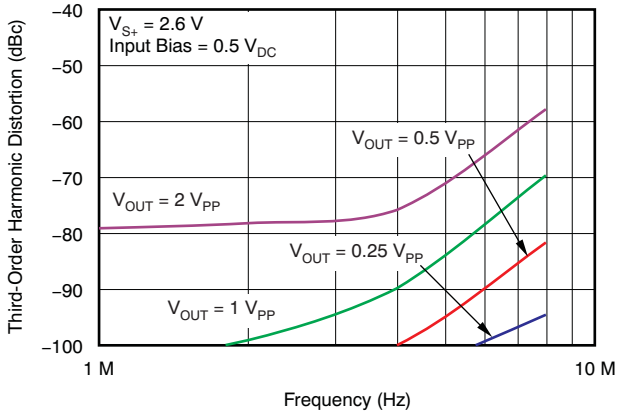


Figure 9.

SMALL-SIGNAL PULSE RESPONSES vs TIME

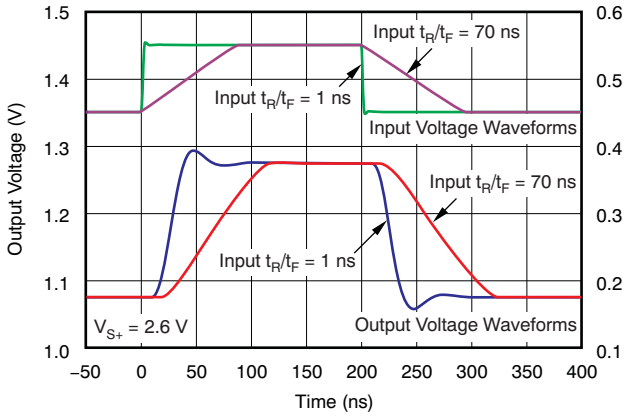


Figure 10.

LARGE-SIGNAL PULSE RESPONSES vs TIME

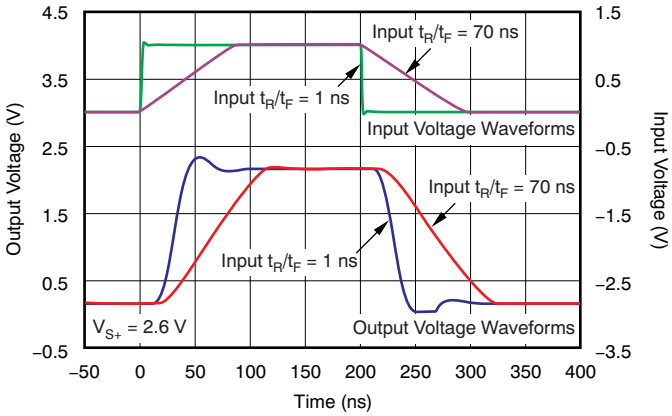


Figure 11.

SLEW RATE vs OUTPUT VOLTAGE

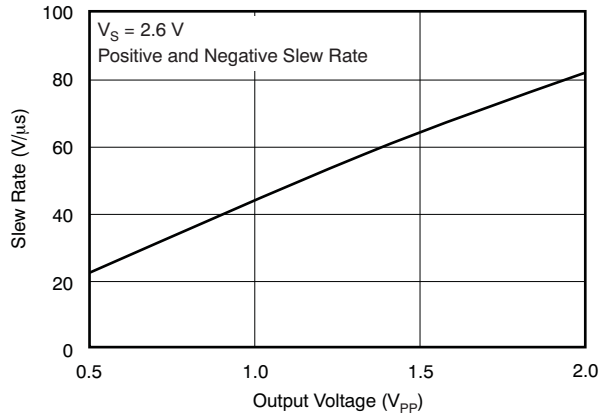


Figure 12.

ENABLE/DISABLE RESPONSE vs TIME

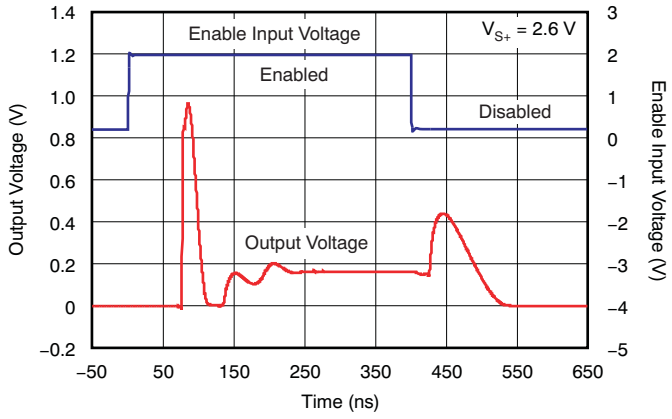


Figure 13.

TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

SIGNAL GAIN vs FREQUENCY

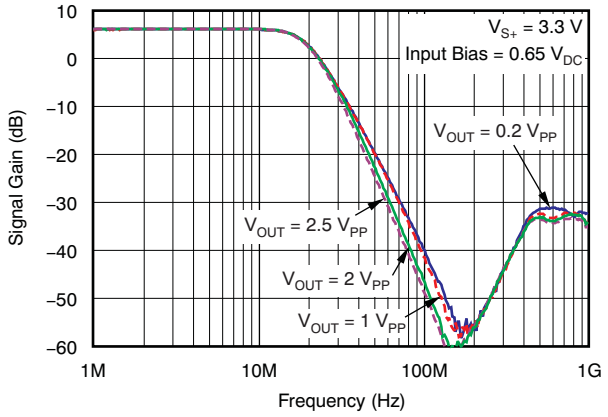


Figure 14.

SIGNAL GAIN vs FREQUENCY

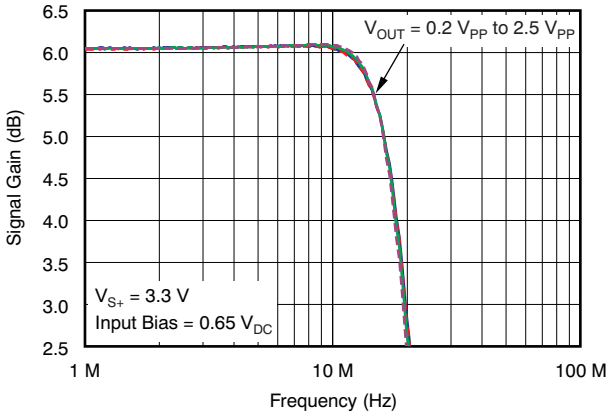


Figure 15.

PHASE vs FREQUENCY

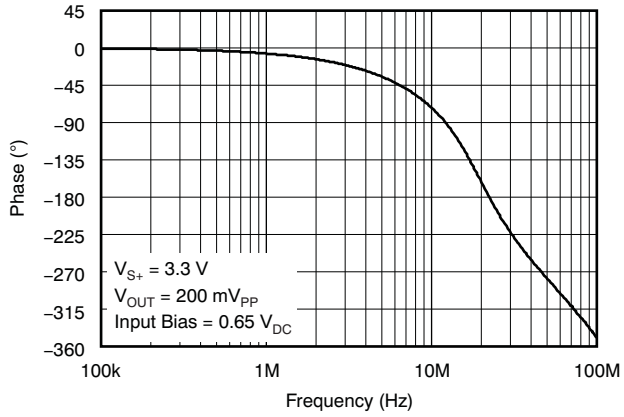


Figure 16.

GROUP DELAY vs FREQUENCY

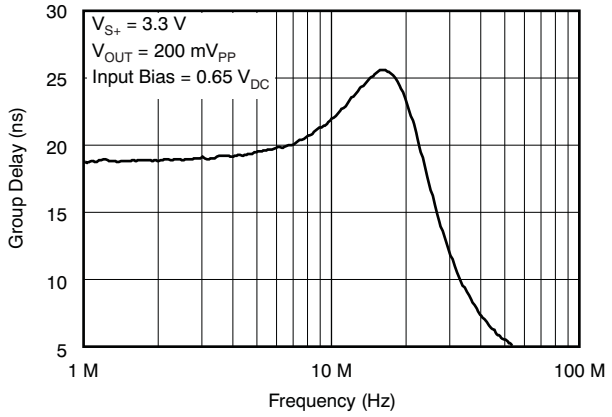


Figure 17.

SMALL-SIGNAL FREQUENCY RESPONSE vs CAPACITIVE LOADING

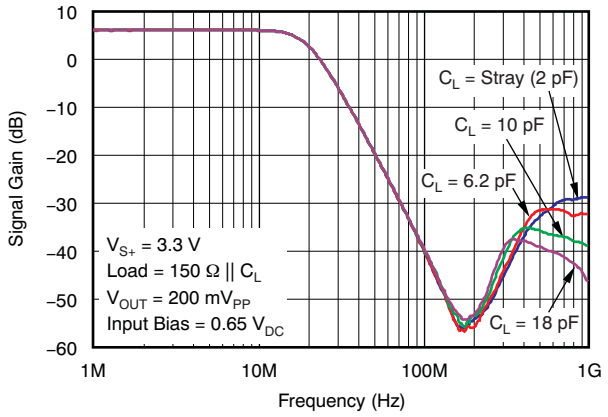


Figure 18.

CROSSTALK vs FREQUENCY

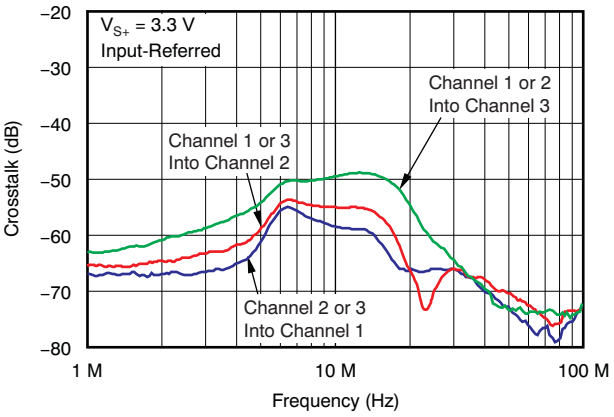


Figure 19.

TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V (continued)

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

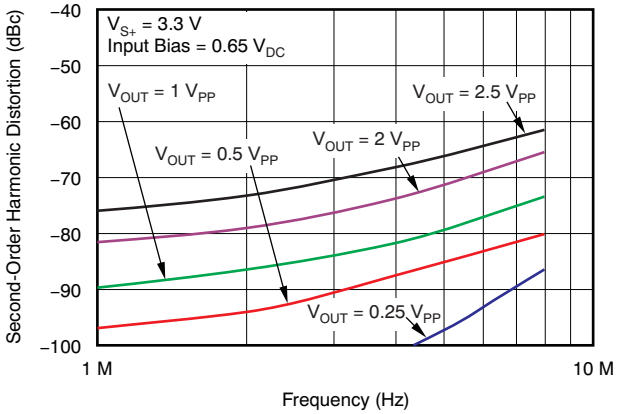


Figure 20.

THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

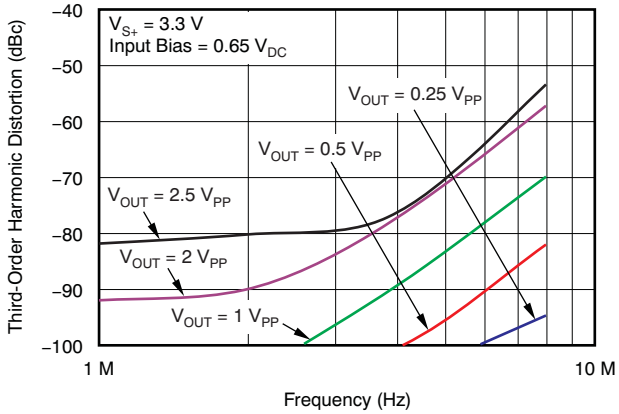


Figure 21.

SMALL-SIGNAL PULSE RESPONSES vs TIME

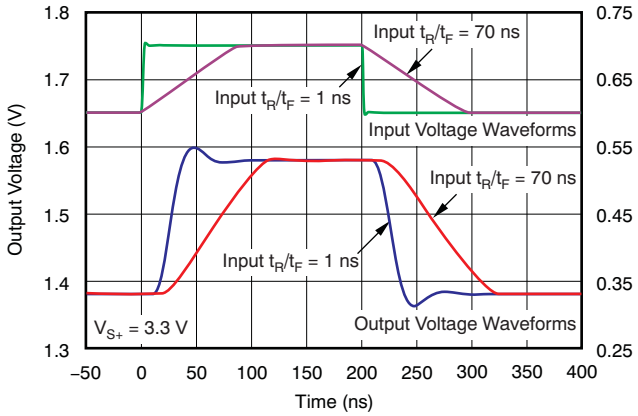


Figure 22.

LARGE-SIGNAL PULSE RESPONSES vs TIME

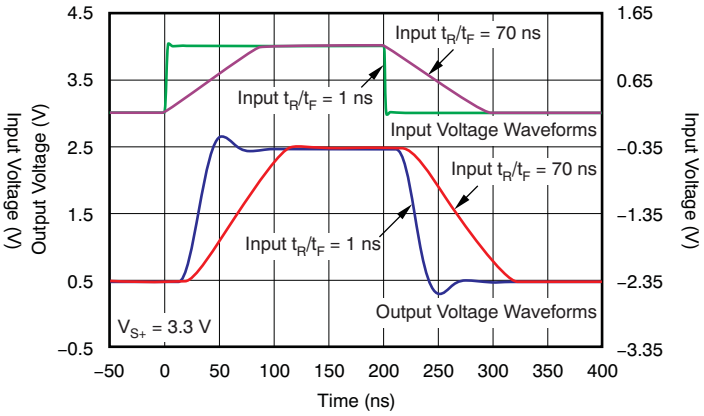


Figure 23.

SLEW RATE vs OUTPUT VOLTAGE

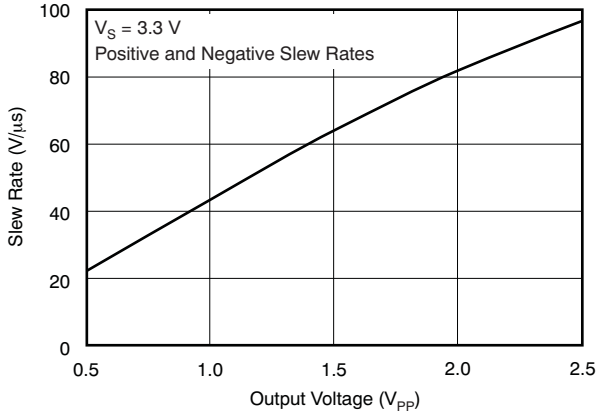


Figure 24.

ENABLE/DISABLE RESPONSE vs TIME

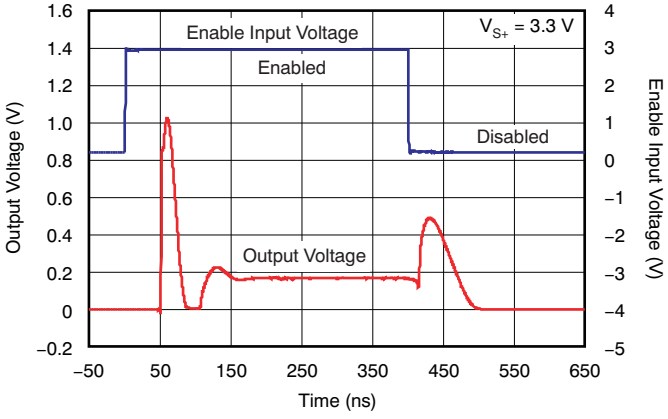


Figure 25.

TYPICAL CHARACTERISTICS: V_{S+} = 3.3 V (continued)

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

INPUT BIAS CURRENT vs TEMPERATURE

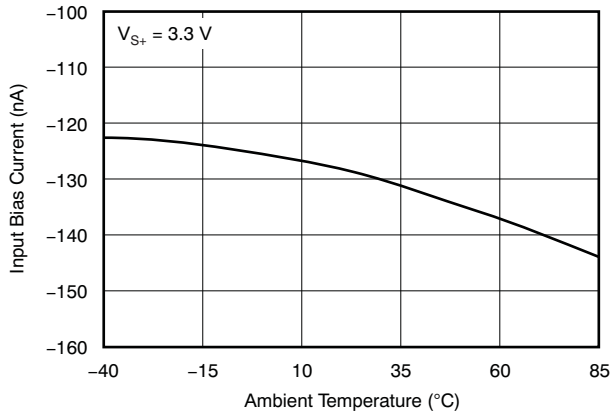


Figure 26.

OUTPUT OFFSET VOLTAGE vs TEMPERATURE

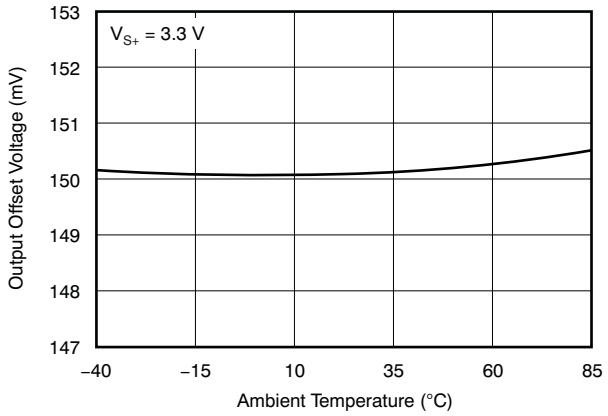


Figure 27.

MAXIMUM OUTPUT VOLTAGE vs TEMPERATURE

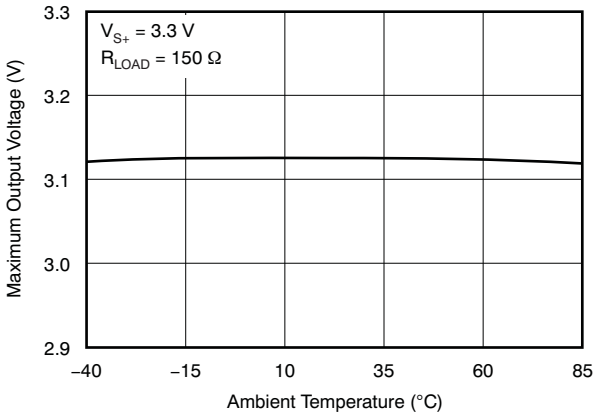


Figure 28.

ATTENUATION AT 14 MHz vs TEMPERATURE

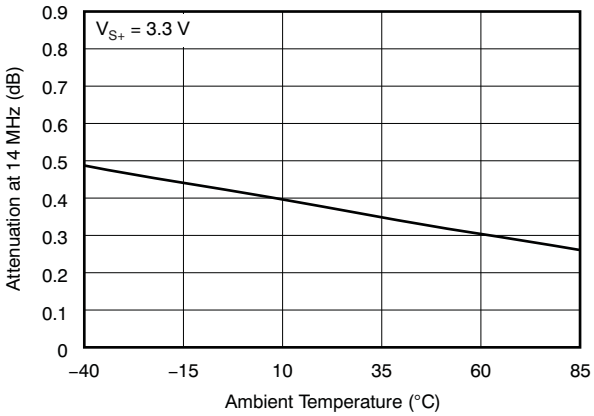


Figure 29.

ATTENUATION AT 43 MHz vs TEMPERATURE

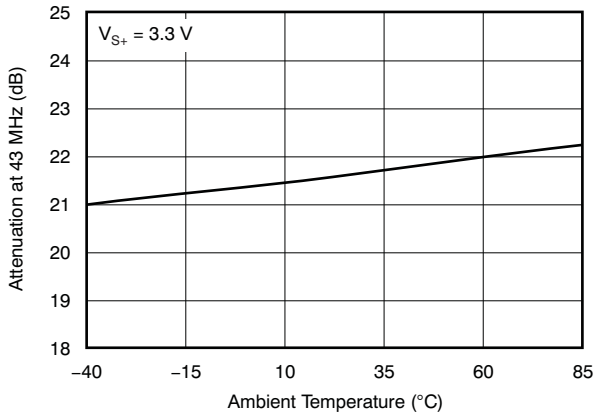


Figure 30.

TYPICAL CHARACTERISTICS: V_{S+} = 5 V

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

SIGNAL GAIN vs FREQUENCY

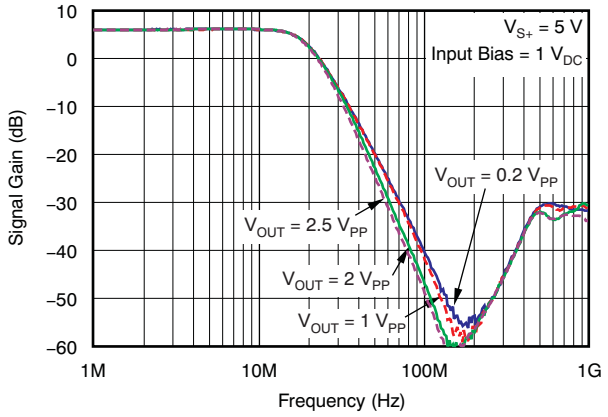


Figure 31.

SIGNAL GAIN vs FREQUENCY

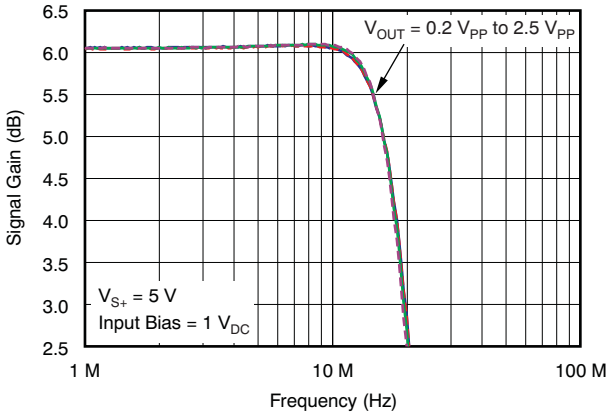


Figure 32.

PHASE vs FREQUENCY

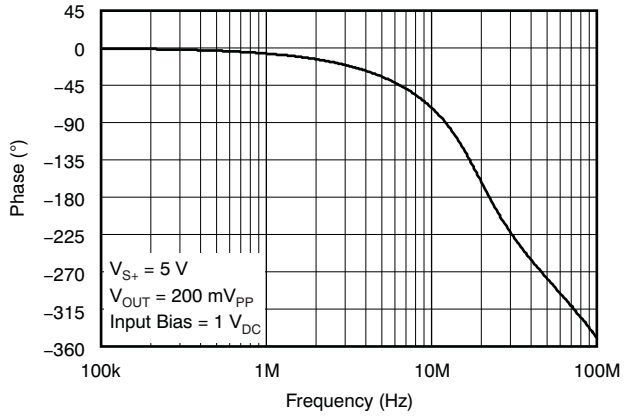


Figure 33.

GROUP DELAY vs FREQUENCY

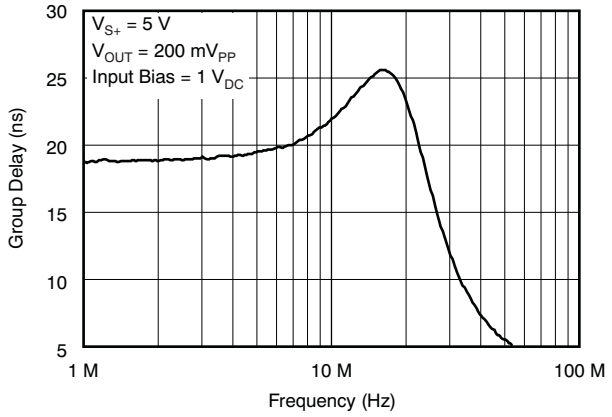


Figure 34.

SMALL-SIGNAL FREQUENCY RESPONSE vs CAPACITIVE LOADING

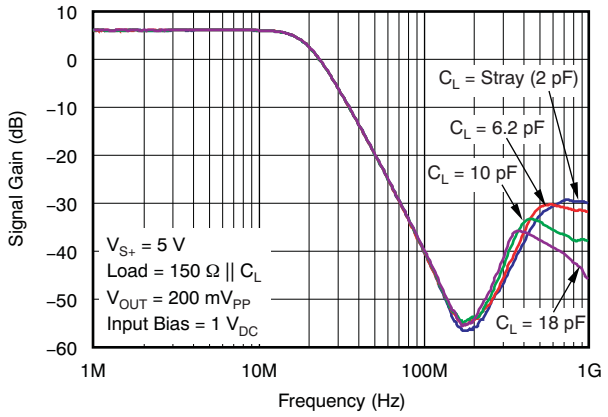


Figure 35.

CROSSTALK vs FREQUENCY

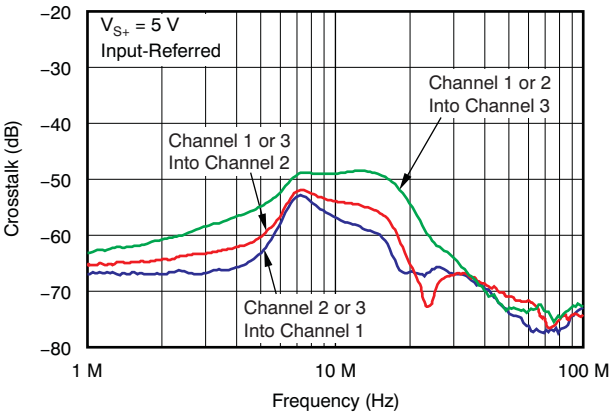


Figure 36.

TYPICAL CHARACTERISTICS: V_{S+} = 5 V (continued)

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

SECOND-ORDER HARMONIC DISTORTION vs FREQUENCY

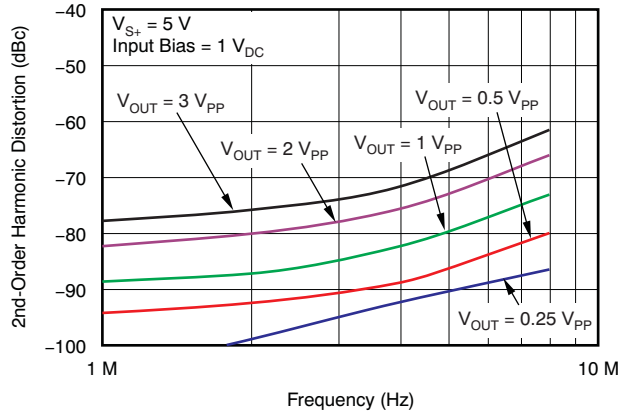


Figure 37.

THIRD-ORDER HARMONIC DISTORTION vs FREQUENCY

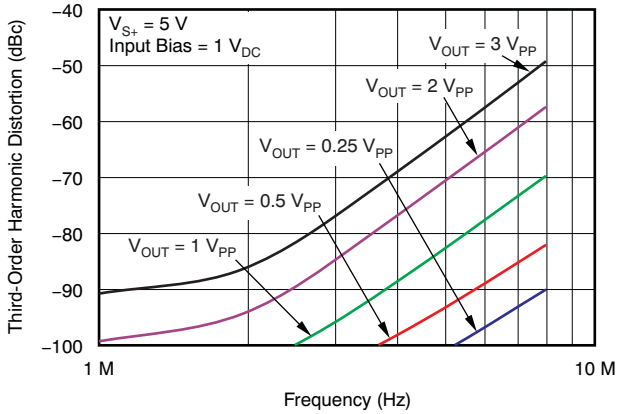


Figure 38.

SMALL-SIGNAL PULSE RESPONSES vs TIME

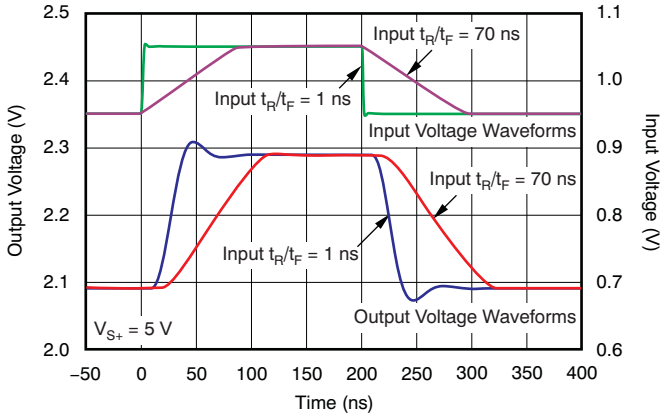


Figure 39.

LARGE-SIGNAL PULSE RESPONSES vs TIME

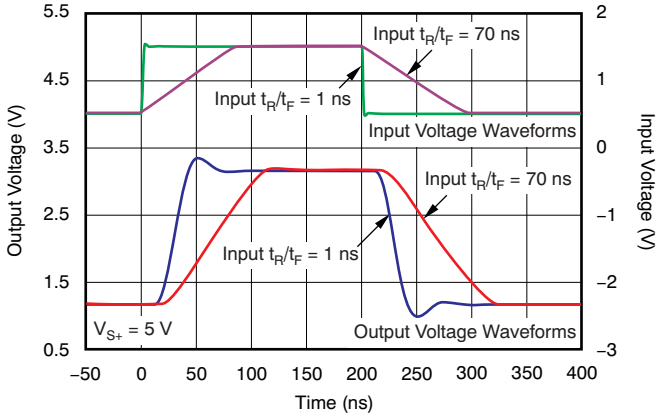


Figure 40.

SLEW RATE vs OUTPUT VOLTAGE

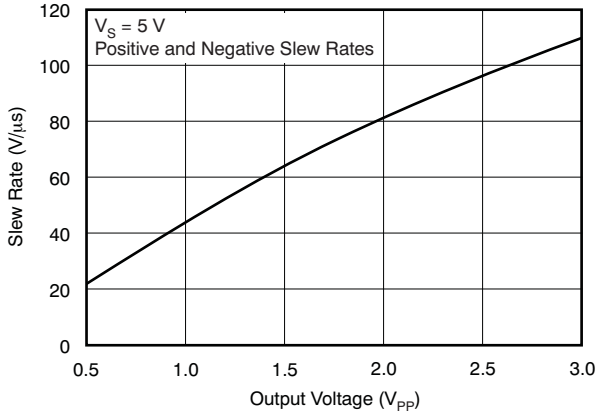


Figure 41.

ENABLE/DISABLE RESPONSE vs TIME

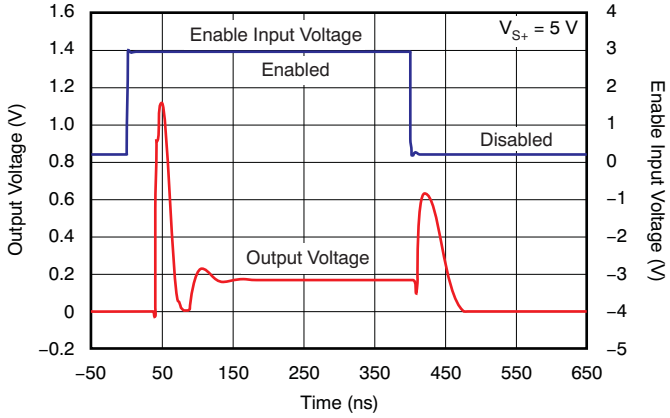


Figure 42.

TYPICAL CHARACTERISTICS: GENERAL

At T_A = +25°C, load = 150 Ω || 6.2 pF to GND, and dc-coupled input/output, unless otherwise noted.

DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

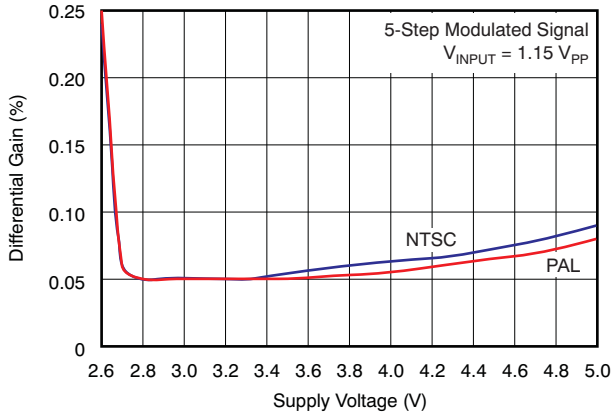


Figure 43.

DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

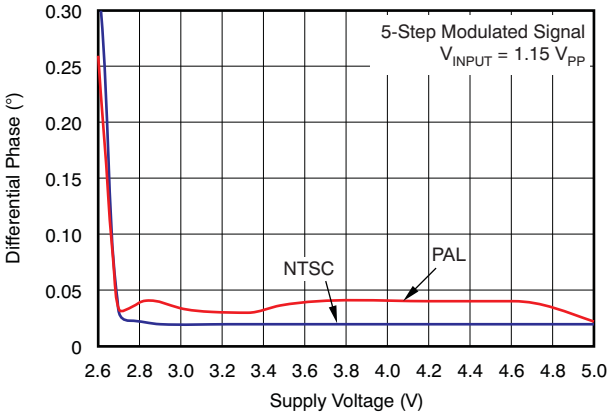


Figure 44.

TOTAL QUIESCENT CURRENT vs TEMPERATURE

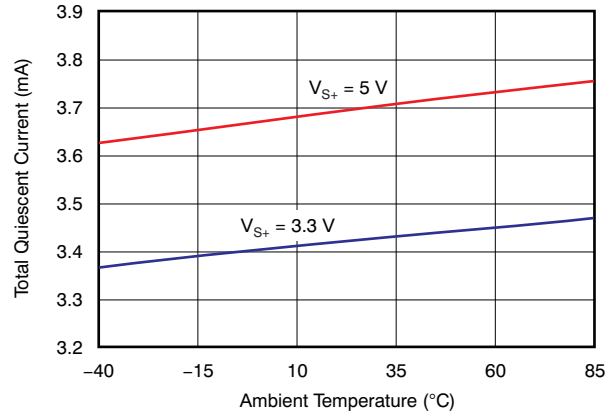


Figure 45.

OUTPUT IMPEDANCE vs FREQUENCY

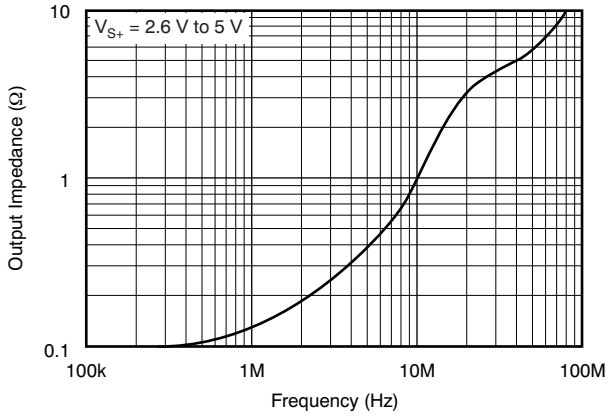


Figure 46.

S22 OUTPUT REFLECTION RATIO vs FREQUENCY

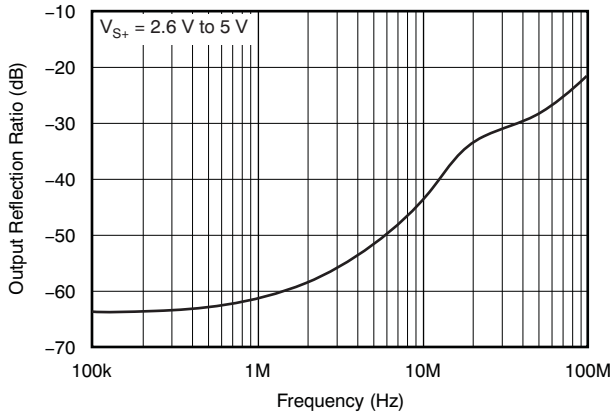


Figure 47.

DISABLED OUTPUT IMPEDANCE vs FREQUENCY

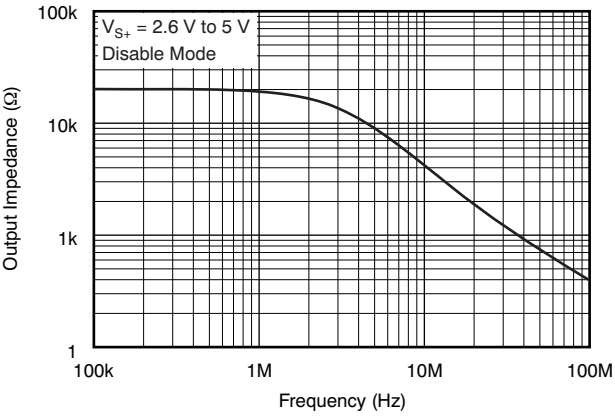


Figure 48.

APPLICATION INFORMATION

The THS7319 is targeted for triple-channel video output applications that require three enhanced-definition (ED) video and/or RGB video output buffers. The THS7319 also supports standard definition (SD) video for oversampled systems with DAC sampling frequency of 54-MHz or greater. Although the THS7319 can be used for numerous other applications, the needs and requirements of the video signal are the most important design parameters. Built on the revolutionary, complementary Silicon Germanium (SiGe) BiCom3X process, the THS7319 incorporates many features not typically found in integrated video parts while consuming very low power. The THS7319 includes the following features:

- Single-supply 2.6-V to 5-V operation with low total quiescent current of 3.4 mA at 3.3 V and 3.7 mA at 5 V
- Enable mode for shutting down the THS7319 amplifiers to save system power in power-sensitive applications
- DC input configuration with internal 150-mV dc level shifting to prevent sync crushing and saturation effects
- Third-order 20-MHz (–3-dB) low-pass filter for DAC reconstruction or ADC image rejection ideal for:
  - NTSC/PAL 480p/576p $Y'P'_BP'_R$ or G'B'R' (R'G'B') signals
  - NTSC/PAL/SECAM composite video (CVBS), S-Video Y'/C', 480i/576i $Y'P'_BP'_R$, and G'B'R' (R'G'B') signals for oversampled systems
- Internally-fixed gain of 2-V/V (+6 dB) amplifiers that allows for dc-coupling or traditional ac-coupling
- Flow-through configuration using an ultra-small MicrostarCSP package

OPERATING VOLTAGE

The THS7319 is designed to operate from 2.6 V to 5 V over a –40°C to +85°C temperature range. The impact on performance over the entire temperature range is negligible as a result of the implementation of thin film resistors and high-quality, low-temperature coefficient capacitors. The design of the THS7319 allows operation down to 2.5 V, but it is recommended to use at least a 2.7 V supply to ensure that no issues arise with headroom or clipping with 100% color-saturated CVBS signals. If only 75% color saturated CVBS is supported, then the output voltage requirements are reduced to 2 V_{PP} on the output, allowing a 2.6-V supply to be used without issues.

A 0.1-µF capacitor should be placed as close as possible to the power-supply pins to avoid potential ringing or oscillation. Additionally, a large capacitor (such as 22 µF to 100 µF) should be placed on the power-supply line to minimize interference with 50-/60-Hz line frequencies.

INPUT VOLTAGE

The THS7319 input range allows for an input signal range from –0.06 V to approximately (V_{S+} – 1.5 V). However, because of the internal fixed gain of 2 V/V (+6 dB) and the internal output level shift of 150 mV (typical), the output is generally the limiting factor for the allowable linear input range. For example, with a 5-V supply, the linear input range is from –0.06 V to 3.5 V. However, because of the gain and level shift, the linear output range limits the allowable linear input range to approximately –0.06 V to 2.3 V.

INPUT OVERVOLTAGE PROTECTION

The THS7319 is built using a very high-speed, complementary, bipolar, and CMOS process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All input and output device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 49.

These diodes provide moderate protection to input overdrive voltages above and below the supplies as well. The protection diodes can typically support 30 mA of continuous current when overdriven.

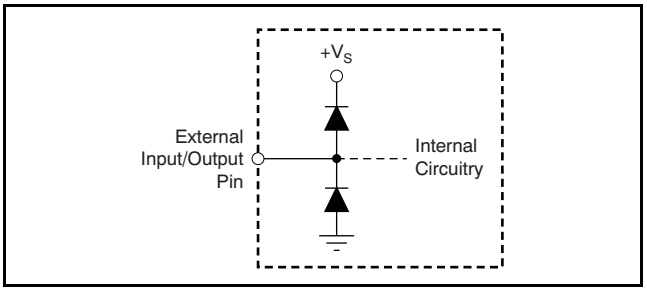


Figure 49. Internal ESD Protection

TYPICAL CONFIGURATION AND VIDEO TERMINOLOGY

A typical application circuit using the THS7319 as a video buffer is shown in Figure 50. It shows a DAC or encoder dc-coupled to the input channels of the THS7319 and the output of the THS7319 dc-coupled to the video line. These signals can be NTSC, PAL, or SECAM signals including composite video baseband signal (CVBS), S-Video Y'C', component $Y'P'_BP'_R$ video, broadcast G'B'R' video, or computer R'G'B' video signals.

Note that the *Y'* term is used for the luma channels throughout this document rather than the more common luminance (*Y*) term. This usage accounts for the definition of luminance as stipulated by the International Commission on Illumination (CIE). Video departs from true luminance because a nonlinear term, *gamma*, is added to the true RGB signals to form R'G'B' signals. These R'G'B' signals are then used to mathematically create luma (Y'). Thus, luminance (Y) is not maintained, providing a difference in terminology.

This rationale is also used for the chroma (*C'*) term. Chroma is derived from the nonlinear R'G'B' terms and, thus, it is nonlinear. Chominance (*C*) is derived from linear RGB, giving the difference between chroma (C') and chrominance (C). The color difference signals (P'_B/P'_R/U'/V') are also referenced in this manner to denote the nonlinear (gamma corrected) signals.

R'G'B' (commonly mislabeled *RGB*) is also called G'B'R' (again commonly mislabeled as *GBR*) in professional video systems. The Society of Motion Picture and Television Engineers (SMPTE) component standard stipulates that the luma information is placed on the first channel, the blue color difference is placed on the second channel, and the red color difference signal is placed on the third channel. This practice is consistent with the $Y'P'_BP'_R$ nomenclature. Because the luma channel (Y') carries the sync information and the green channel (G') also carries the sync information, it makes logical sense that G' be placed first in the system. Because the blue color difference channel (P'_B) is next and the red color difference channel (P'_R) is last, then it also makes logical sense to place the B' signal on the second channel and the R' signal on the third channel, respectfully. Thus, hardware compatibility is better achieved when using G'B'R' rather than R'G'B'. Note that for many G'B'R' systems, sync is embedded on all three channels, but this configuration may not always be the case in all systems.

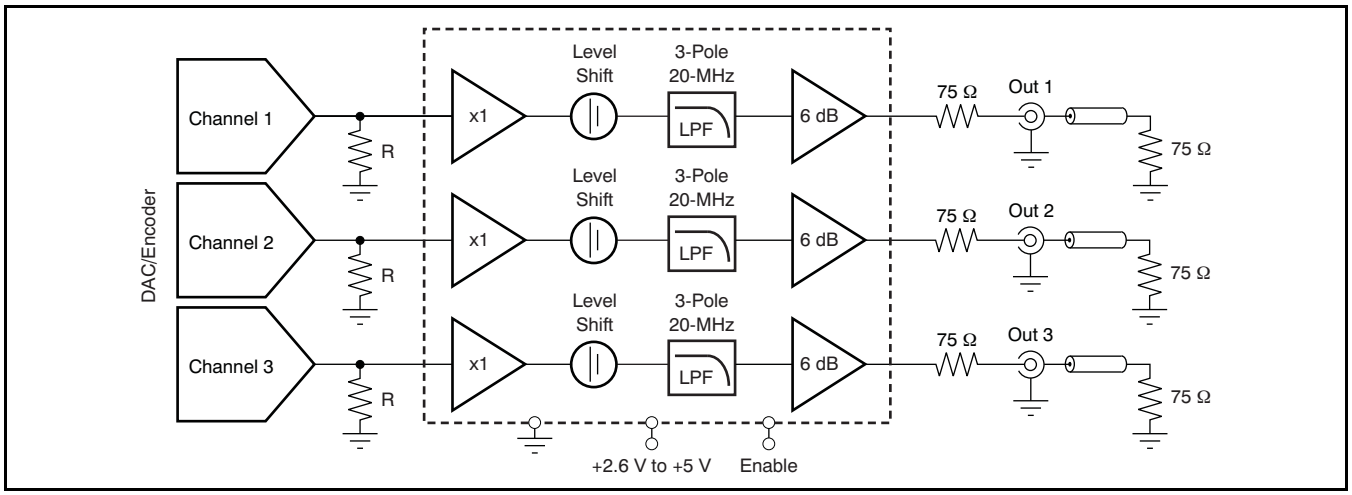


Figure 50. Typical THS7319 System with DC-Coupled Encoder/DAC and DC-Coupled Line Driving

INPUT OPERATION

The inputs to the THS7319 allow for dc-coupled inputs. Most DACs or video encoders can be dc-connected to the THS7319 with essentially any DAC termination resistance desired for the system. One of the potential drawbacks to dc-coupling is when 0 V is applied to the input from the DAC. Although the input of the THS7319 allows for a 0-V input signal without issue, the output swing of a traditional amplifier cannot yield a 0-V signal that results in possible clipping of the signal. This limitation is true for any single-supply amplifier because of the characteristics of the output transistors. Neither CMOS nor bipolar transistors can achieve 0 V while sinking current. This transistor characteristic is also the same reason why the highest output voltage is always less than the power-supply voltage when sourcing current.

This output clipping can reduce the sync amplitudes (both horizontal and vertical sync) on the video signal. A problem occurs if the video signal receiver uses an automatic gain control (AGC) loop to account for losses in the transmission line. Some video AGC circuits derive gain from the horizontal sync amplitude. If clipping occurs on the sync amplitude, then the AGC circuit can increase the gain too much—resulting in too much luma and/or chroma amplitude gain correction. This correction may result in a picture with an overly bright display with too much color saturation.

Other AGC circuits may use the chroma burst amplitude for amplitude control. For this situation, reduction in the sync signals does not alter the proper gain setting. However, it is good engineering design practice to ensure that saturation/clipping does not take place. Transistors always take a finite amount of time to come out of saturation. This saturation could possibly result in timing delays or other aberrations on the signals that may not be desirable.

To eliminate saturation or clipping problems, the THS7319 has a 150-mV output level shift feature. This feature takes the input voltage and adds an internal +75-mV shift to the input signal. Because of the 6-dB (2 V/V) gain, the resulting output with a 0-V applied input signal is approximately 150 mV. The THS7319 rail-to-rail output stage can create this output level while connected to a typical video load. This configuration ensures the sync signal clipping or saturation does not occur. This shift is constant, regardless of the input signal. The equation for this is $V_{OUT} = (V_{IN} \times 2\ V/V) + 0.15\ V$. For example, if a 1-V input is applied, the output is (1 V × 2 V/V) + 0.15 V = 2.15 V.

Because the internal gain is fixed at +6 dB (2 V/V), it dictates the allowable linear input voltage range. For example, if the power supply is set to 3 V, the maximum output is approximately 2.9 V while driving a significant amount of current. Thus, to avoid clipping, the allowable input is ([2.9 V – 0.15 V]/2) = 1.375 V. This range is valid for up to the maximum recommended 5-V power supply that allows approximately a ([4.9 V – 0.15 V]/2) = 2.375 V input range while avoiding clipping on the output.

The input impedance of the THS7319 is dictated by the internal high-impedance unity-gain buffer as shown in Figure 51. This buffer has a very high 2.4 MΩ || 2 pF input impedance that is effectively transparent to the source with no interactions. Unlike other products where the filter elements are tied directly to the input pin without buffering, there are no filter performance changes or interaction with the DAC termination resistance. Note that the internal voltage shift does not appear at the input pin; it only shows at the output pin.

While ac-coupling with dc-biasing using external resistor dividers can be done, it is generally not recommended because of the large resistor values required. These large resistor values coupled with the input bias current of the THS7319 input can cause a significant voltage shift to appear on the input. If ac coupling is necessary for a system, several elements must be taken into account for a proper design: the high-pass corner frequency (typically desired to be about 2.5-Hz); the size of the input capacitor value; the parallel input resistance of the voltage divider; and the input bias current. Contact Texas Instruments for design support if ac coupling is necessary in the design.

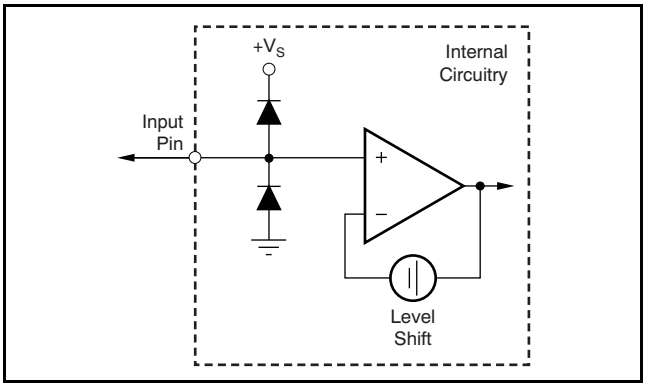


Figure 51. Equivalent DC Input Mode Circuit

DC-COUPLED OUTPUT

The THS7319 incorporates a rail-to-rail output stage that can drive the line directly without the need for large ac-coupling capacitors. This design offers the best line tilt and field tilt (droop) performance because no ac-coupling occurs. Keep in mind that if the input is ac-coupled, then the resulting tilt as a result of the input ac-coupling continues to be seen on the output, regardless of the output coupling. The 70-mA output current drive capability of the THS7319 is designed to drive the video line while keeping the output dynamic range as wide as possible.

One concern of dc-coupling, however, arises if the line is terminated to ground. If an ac-bias input configuration is used or if a dc reference from the DAC is applied, such as S-Video C'/component P'_B/or component P'_R signals, the output of the THS7319 will have a dc bias on the output, such as 1 V. This configuration allows a dc current path to flow, such as 1 V/150 Ω = 6.67 mA. The result of this configuration is a slightly decreased high output voltage swing and an increase in power dissipation of the THS7319. While the THS7319 was designed to operate with a junction temperature of up to +125°C, care must be taken to ensure that the junction temperature does not exceed this level or else long-term reliability could suffer. Using a 5-V supply, this configuration can result in an additional power dissipation of (5 V – 1 V) × 6.67 mA = 26.7 mW per channel. With a 3.3-V supply, this dissipation reduces to 15.3 mW per channel. The overall low quiescent current of the THS7319 design minimizes potential thermal issues even when used at high ambient temperatures, but power and thermal analysis should always be examined in any system to ensure that no issues arise. Be sure to use RMS power and not instantaneous power when evaluating the thermal performance.

Note that the THS7319 can drive the line with dc-coupling regardless of the input mode of operation. The only requirement is to make sure the video line has proper termination in series with the output (typically 75 Ω). This requirement helps isolate capacitive loading effects from the THS7319 output. Failure to properly isolate capacitive loads may result in ringing or oscillation. The stray capacitance appearing directly at the THS7319 output pins should be kept below 18-pF. One method to ensure this condition is to make sure the 75-Ω source resistor is placed next to each THS7319 output pin.

There are many reasons dc-coupling is desirable, including reduced costs, printed circuit board (PCB) area, and no line tilt or field tilt. A common question is whether or not there are any drawbacks to using dc-coupling. There are a few potential issues that must be examined, such as the dc current bias as discussed above. Another potential risk is whether this configuration meets industry standards. EIA-770 stipulates that the back-porch shall be 0 V ± 1 V as measured at the receiver. With a double-terminated load system, this requirement implies a 0-V ± 2-V level at the video amplifier output. The THS7319 can easily meet this requirement without issue. However, in Japan, the EIAJ CP-1203 specification stipulates a 0-V ± 0.1-V level with no signal. This requirement can be met with the THS7319 in disable mode, but while active it cannot meet this specification without output ac-coupling.

AC-COUPLED OUTPUT

A very common method of coupling the video signal to the line is with a large capacitor. This capacitor is typically between 220 µF and 1000 µF, although 470 µF is very typical. The value of this capacitor must be large enough to minimize the line tilt (droop) and/or field tilt associated with ac-coupling as described previously in this document. AC-coupling is performed for several reasons, but the most common is to ensure full interoperability with the receiving video system. This approach ensures that regardless of the reference dc voltage used on the transmitting side, the receiving side re-establishes the dc reference voltage to its own requirements.

In the same way as the dc output mode of operation discussed previously, each line should have a 75-Ω source termination resistor in series with the ac-coupling capacitor. This 75-Ω series resistor should be placed next to the THS7319 output to minimize capacitive loading effects.

Because of the edge rates and frequencies of operation, it is recommended (but not required) to place a 0.1-µF to 0.01-µF capacitor in parallel with the large 220-µF to 1000-µF capacitor. These large value capacitors are most commonly aluminum electrolytic. It is well-known that these capacitors have significantly large equivalent series resistance (ESR), and the impedance at high frequencies is rather large as a result of the associated inductances involved with the leads and construction. The small 0.1-µF to 0.01-µF capacitors help pass these high-frequency signals (greater than 1 MHz) with much lower impedance than the large capacitors.

Although it is common to use the same capacitor values for all the video lines, the frequency bandwidth of the chroma signal in a S-Video system is not required to go as low (or as high of a frequency) as the luma channels. Thus, the capacitor values of the chroma line(s) can be smaller, such as 0.1 µF.

Figure 52 shows a typical configuration where the input is dc-coupled and the output is also ac-coupled. AC-coupled inputs are generally required when current-sink DACs are used or the input is connected to an unknown source, such as when the THS7319 is used as an input device.

LOW-PASS FILTER

Each channel of the THS7319 incorporates a third-order low-pass filter. These video reconstruction filters minimize DAC images from being passed onto the video receiver. Depending on the receiver design, failure to eliminate these DAC images can cause picture quality problems as a result of aliasing of the ADC in the receiver. Another benefit of the filter is to smooth out aberrations in the signal that DACs typically have associated with the digital stepping of the signal. This benefit helps with picture quality and ensures that the signal meets video bandwidth requirements.

Each filter has an associated Butterworth characteristic. The benefit of the Butterworth response is that the frequency response is flat with a relatively steep initial attenuation at the corner frequency. The concern with the Butterworth characteristic is that the group delay rises near the corner frequency. Group delay is defined as the change in phase (radians/second) divided by a change in frequency. An increase in group delay corresponds to a time domain pulse response that has overshoot and some possible ringing associated with the overshoot.

The use of other type of filters, such as elliptic or chebyshev, are not recommended for video applications because of the very large group delay variations near the corner frequency resulting in significant overshoot and ringing. While these filters may help meet the video standard specifications with respect to amplitude attenuation, the group delay is well beyond the standard specifications. Considering this group delay with the fact that video can go from a white pixel to a black pixel over and over again, it is easy to see that ringing can occur. Ringing typically causes a display to have ghosting or fuzziness appear on the edges of a sharp transition. On the other hand, a Bessel filter has ideal group delay response, but the rate of attenuation is typically too low for acceptable image rejection. Thus, the Butterworth filter is a respectable compromise for both attenuation and group delay.

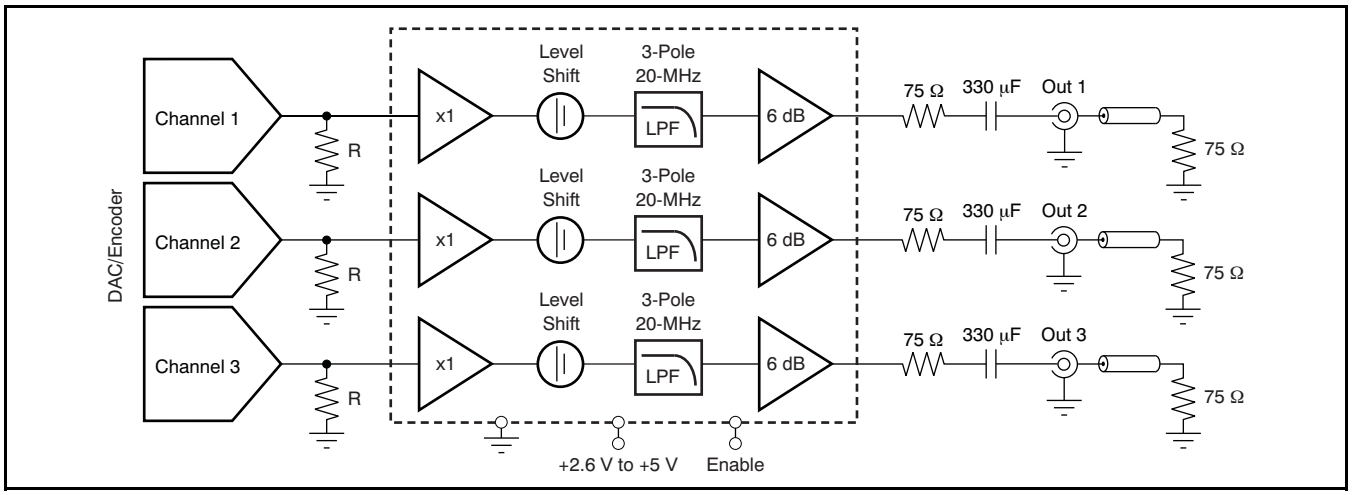


Figure 52. Typical DC Input System Driving AC-Coupled Video Lines

The THS7319 filters have a nominal corner (–3 dB) frequency at 20-MHz and a –1 dB passband typically at 17-MHz. This 20-MHz filter is ideal for enhanced definition (ED) NTSC or PAL 480p/576p Y'P'$_B$P'$_R$ or G'B'R'/R'G'B' signals. For oversampled systems, the THS7319 works well for passing standard definition (SD) NTSC, PAL, or SECAM composite video (CVBS), S-Video signals (Y'C'), 480i/576i Y'P'$_B$P'$_R$, Y'U'V', broadcast G'B'R' signals, and R'G'B' video signals. The 20-MHz, –3-dB corner frequency was designed to achieve 27-dB of attenuation at 54 MHz—a common sampling frequency between the DAC/ADC second and third Nyquist zones found in many video systems. This consideration is important because any signal that appears around this frequency can also appear in the baseband as a result of aliasing effects of an ADC found in a receiver. Another specification ensured for the THS7319 is attenuation at 43 MHz. This frequency is derived from the fact that the ED Y' signal has an 11-MHz bandwidth. Following standard sampling theory, this means that the second Nyquist zone image starts at 54 MHz – 11 MHz = 43 MHz.

Keep in mind that images do not stop at the DAC sampling frequency, f_S (for example, 54 MHz for traditional ED DACs); they continue around the sampling frequency harmonics of 2× f_S, 3× f_S, 4× f_S, and so on (that is, 108-MHz, 162-MHz, 216-MHz, etc.). Because of these multiple images, an ADC can fold down into the baseband signal, meaning that the low-pass filter must also eliminate these higher-order images. The THS7319 filters are designed to attenuate all of these higher frequencies without *bounce effect* that some filters can allow.

The filter frequencies were chosen to account for process variations in the THS7319. To ensure the required video frequencies are effectively passed, the filter corner frequency must be high enough to allow component variations. The other consideration is that the attenuation must be large enough to ensure the anti-aliasing/reconstruction filtering is sufficient to meet the system demands. Thus, the selection of the filter frequencies was not arbitrarily selected and is a good compromise that should meet the demands of most systems.

BENEFITS OVER PASSIVE FILTERING

Two key benefits of using an integrated filter system, such as the THS7319, over a passive system are PCB area and filter variations. The ultra-small MicrostarCSP 9-ball package is much smaller over a passive RLC network, especially a three-pole passive network for three channels. Additionally, consider that inductors have at best ±10% tolerances (normally, ±15% to ±20% is common) and capacitors typically have ±10% tolerances. A Monte Carlo analysis shows that the filter corner frequency (–3 dB), flatness (–1 dB), Q factor (or peaking), and channel-to-channel delay have wide variations. These variances can lead to potential performance and quality issues in mass-production environments. The THS7319 solves most of these problems with the corner frequency being essentially the only variable.

Another concern about passive filters is the use of inductors. Inductors are magnetic components, and are therefore susceptible to electromagnetic coupling/interference (EMC/EMI). Some common coupling can occur because of other video channels nearby using inductors for filtering, or it can come from nearby switched-mode power supplies. Some other forms of coupling could be from outside sources with strong EMI radiation and can cause failure in EMC testing such as required for CE compliance.

One concern about an active filter in an integrated circuit is the variation of the filter characteristics when the ambient temperature and the subsequent die temperature change. To minimize temperature effects, the THS7319 uses low-temperature coefficient resistors and high-quality, low-temperature coefficient capacitors found in the BiCom3X process. These filters have been specified by design to account for process variations and temperature variations to maintain proper filter characteristics. This approach maintains a low channel-to-channel time delay that is required for proper video signal performance.

Another benefit of the THS7319 over a passive RLC filter is the input and output impedance. With a passive filter, the input impedance presented to the DAC varies significantly, from 35 Ω to over 1.5 kΩ, and may cause voltage variations over frequency. The THS7319 input impedance is 2.4 MΩ, and only the 2-pF input capacitance plus the PCB trace capacitance impact the input impedance. As such, the voltage variation appearing at the DAC output is better controlled with a fixed termination resistor and the high input impedance buffer of the THS7319.

On the output side of the filter, a passive filter again has a large impedance variation over frequency. The EIA770 specifications require the return loss to be at least 25 dB over the video frequency range of use. For a video system, this requirement implies that the source impedance (which includes the source, series resistor, and the filter) must be better than 75 Ω, +9/–8 Ω. The THS7319 is an operational amplifier that approximates an ideal voltage source, which is desirable because the output impedance is very low and can source and sink current. To properly match the transmission line characteristic impedance of a video line, a 75-Ω series resistor is placed on the output. To minimize reflections and to maintain a good return loss meeting EIA specifications, this output impedance must maintain a 75-Ω impedance. A wide impedance variation of a passive filter cannot ensure this level of performance. On the other hand, the THS7319 has approximately 1 Ω of output impedance, or a return loss of 40 dB, at 11 MHz. Thus, the system is matched significantly better with a THS7319 compared to a passive filter.

One final benefit of the THS7319 over a passive filter is power dissipation. A DAC driving a video line must be able to drive a 37.5-Ω load: the receiver 75-Ω resistor and the 75-Ω impedance matching resistor next to the DAC to maintain the source impedance requirement. This requirement forces the DAC to drive at least 1.25 V_P (100% saturation CVBS)/37.5 Ω = 33.3 mA. A DAC is a current-steering element, and this amount of current flows internally to the DAC even if the output is 0 V. Thus, power dissipation in the DAC may be very high, especially when three channels are being driven.

Using the THS7319 with a high input impedance can reduce DAC power dissipation significantly. This outcome is possible because the resistance that the DAC drives can be substantially increased. It is common to set this resistance in a DAC by a current-setting resistor on the DAC itself. Thus, the resistance can be 300 Ω or more, substantially reducing the current drive demands from the DAC and saving significant amounts of power. For example, a 3.3-V, three-channel DAC dissipates 330 mW alone for the steering current capability (three channels × 33.3 mA × 3.3 V) if it must drive a 37.5-Ω load. With a 300-Ω load, the DAC power dissipation as a result of current steering current would only be 41 mW (three channels × 4.16 mA × 3.3 V), or over eight times lower power. For overall system power, this scenario must also account for the THS7319 power. The THS7319 only consumes 3.4 mA total quiescent current. The quiescent power added is then 3.3 V × 3.4 mA = 11.2 mW. The total system power is then 41 mW + 11 mW = 52 mW, or a factor of six times lower power compared to the DAC driving the line directly. Saving power by adding the THS7319 in a system is easy to see and accomplish, not to mention the added benefit of a three-pole filter on each channel.

PRINTED WIRING BOARD (PWB) DESIGN GUIDE

When designing the pad size for the MicrostarCSP, it is recommended that the layout use a non-solder mask defined (NSMD) landing pad. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 53 and Table 2 define the land pattern recommendations. Figure 54 and Table 3 show a trace width example.

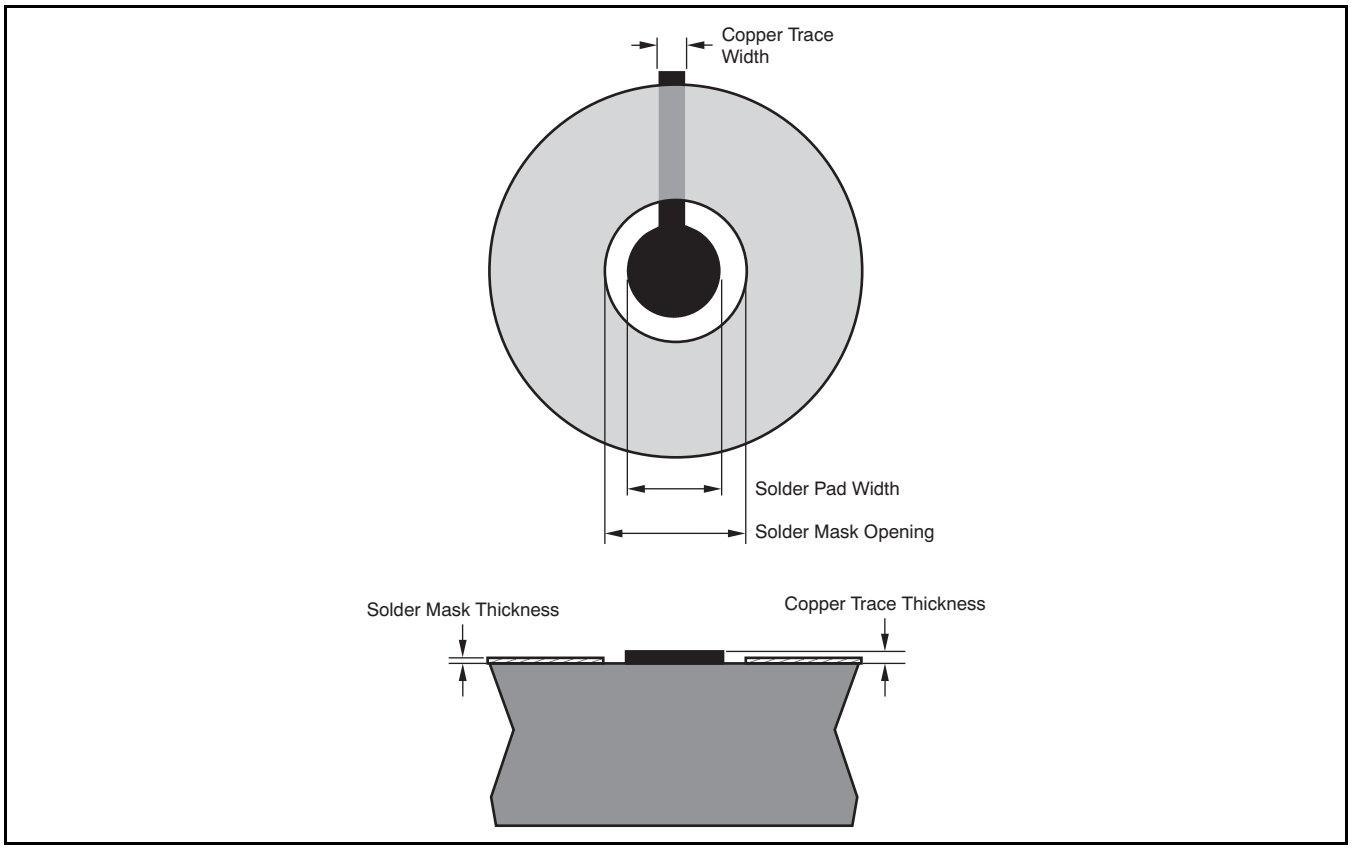
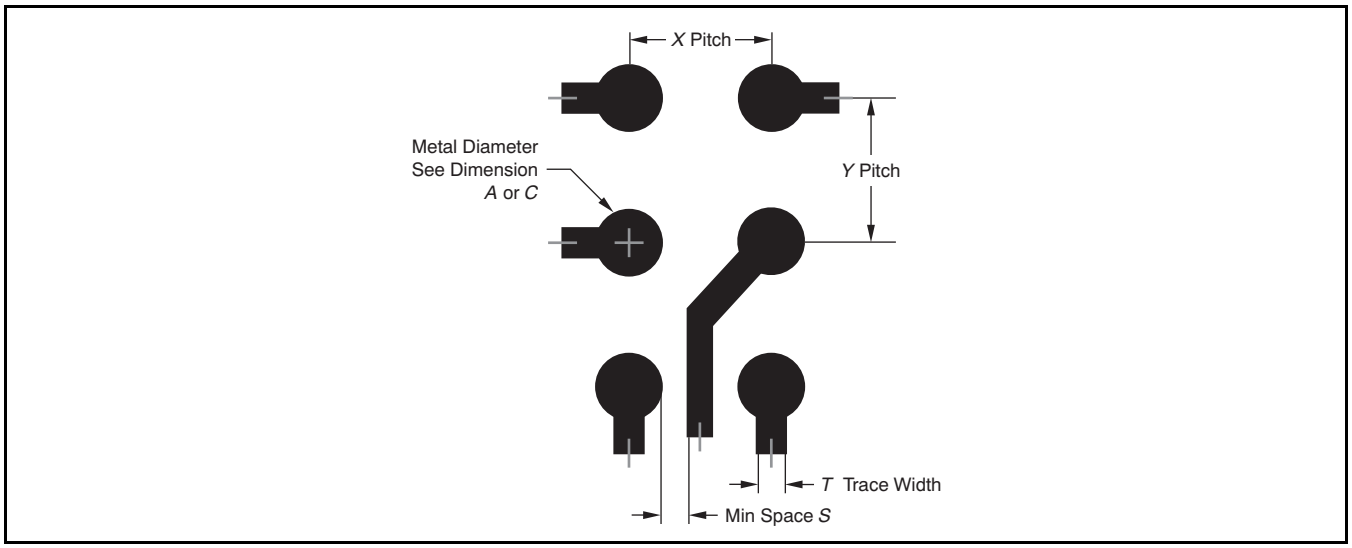


Figure 53. Land Pattern Recommendations

Table 2. Definitions for Figure 53

SOLDER PAD	COPPER PAD	SOLDER MASK OPENING	STENCIL OPENING	STENCIL THICKNESS
Non-solder mask defined (NSMD)	200 µm to 275 µm	Copper pad + 50µm	250 µm × 250 µm square (rounded corners)	100 µm



(1) Circuit traces from the NSMD-defined PWB lands should be 75-µm to 100-µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand-off and impact reliability.

(2) Best reliability results are achieved when the PWB laminate glass transition temperature is greater than the operating temperature range of the intended application.

(3) For a PWB using a Ni/Au surface-finish, the Au thickness should be less than 0.5 µm to avoid a reduction in thermal fatigue performance.

(4) Solder mask thickness should be less than 20 µm above the copper circuit pattern.

(5) Best solder stencil performance is achieved using laser-cut stencils with electro-polishing. Use of chemically-etched stencils results in inferior solder-paste volume control.

(6) Trace routing away from the MicrostarCSP device should be balanced in *X* and *Y* directions to avoid unintentional component movement because of solder wetting forces.

Figure 54. Trace Width/Spacing Example

Table 3. Definitions for Figure 54

PAD	PACKAGE PITCH	(*A* or *C*) METAL DIAMETER	(*S* or *T*) TRACE WIDTH/SPACING
NSMD	0.50 mm	0.25 mm	0.08 mm

Solder Paste

TI recommends using a Type 3 or finer solder paste when mounting the MicrostarCSP. This paste offers the following advantages:

- It acts as a flux to aid wetting of the solder ball to the PCB land.
- The adhesive properties of the paste hold the component in place during the reflow process.
- Solder paste selection is normally driven by the overall system-assembly requirements. In general, the *no clean* compositions are preferred because of the difficulty in cleaning below the mounted components. Customers should check with the solder-paste vendors regarding electrical issues from residues left on the board.

TI recommends a pressure safety zone in mounting the MicrostarCSP package. The recommended force should be controlled to 5N maximum for static and 2.5N for impact.

EXAMPLE REFLOW PROFILE

The MicrostarCSP package solder ball is compatible with lead and lead-free pastes. Example reflow profiles for SnPb and Pb-free are shown in Figure 55 and Figure 56. Table 4 lists the profiles for SnPb and Pb-free reflow.

TI recommends that the solder-paste manufacturer temperature profile be used to optimize flux activity within the MSL guidelines for the most thermally-sensitive component. Refer to J-STD-033 for more details on the MSL classification.

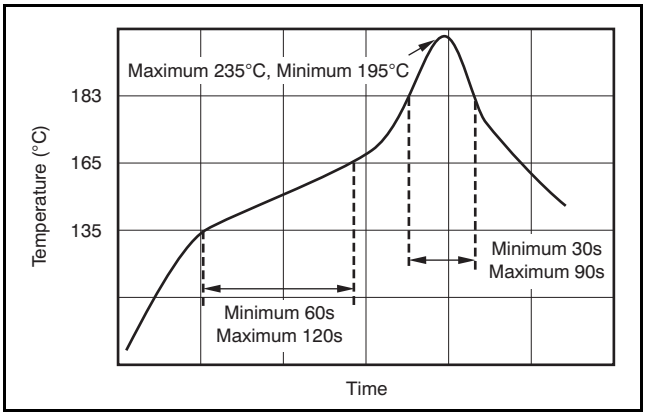


Figure 55. SnPb Temperature Profile Example

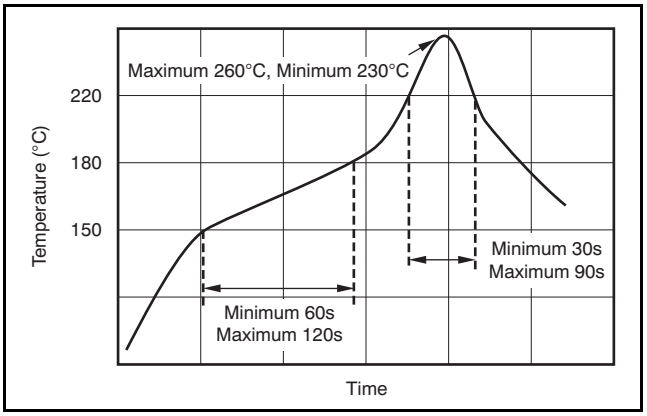


Figure 56. Pb-Free Temperature Profile Example

Table 4. SnPb and Pb-Free Example Reflow Profiles

PARAMETER	SnPb	Pb-FREE
Ramp rate	3°C/second, maximum	3°C/second, maximum
Preheat	135°C to 165°C	150°C to 180°C
	60 to 120 seconds	60 to 120 seconds
Time above liquids	183°C	220°C
	30 to 90 seconds	30 to 90 seconds
Peak temperature	235°C	260°C +0/–5°C
Time within 5°C peak temperature	10 to 20 seconds	10 to 20 seconds
Ramp down rate	6°C/second, maximum	6°C/second, maximum

EVALUATION MODULE

To evaluate the THS7319, an evaluation module (EVM) is available. The EVM allows dc-coupled input and output configurations. Inputs and outputs include BNC connectors commonly found in video systems along with 75-Ω input termination resistors, 75-Ω series source termination resistors, and 75-Ω characteristic impedance traces. This EVM is designed to be used with a single supply from 2.6 V up to 5 V.

The EVM input configuration sets all channels for dc input coupling. The input signal must be within 0 V to approximately 1.5 V for proper operation. Failure to be within this range saturates and/or clips the output signal. Refer to the *Application Information* section for further information.

The THS7319 incorporates an easy method to configure the enable mode. JP1 controls the enable feature. Connecting JP1 to GND applies 0 V to the enable pin and the THS7319 is placed into shutdown mode consuming nominally 0.15 μA of quiescent current. Moving JP1 to $+V_S$ causes the THS7319 to be in normal operation mode where the quiescent current should be nominally 3.4 mA for the entire EVM. This quiescent current is with no load or no signal applied on the input. Adding a load and/or input signal causes the quiescent current to vary accordingly.

Figure 57 shows the EVM schematic. Figure 58 and Figure 59 illustrate the two layers of the EVM PCB, incorporating standard high-speed layout practices. Table 5 lists the bill of materials as the board comes supplied from Texas Instruments.

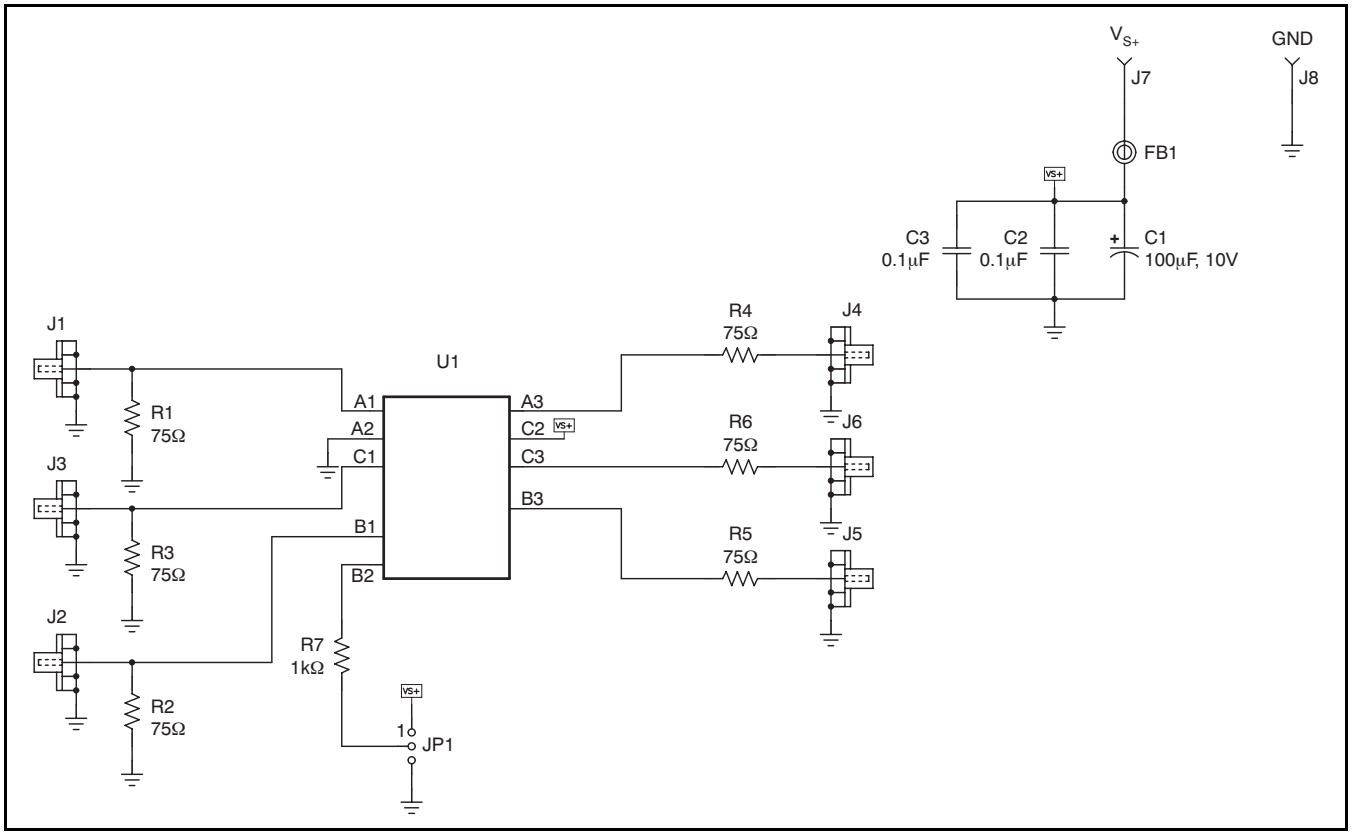


Figure 57. THS7319 EVM Schematic

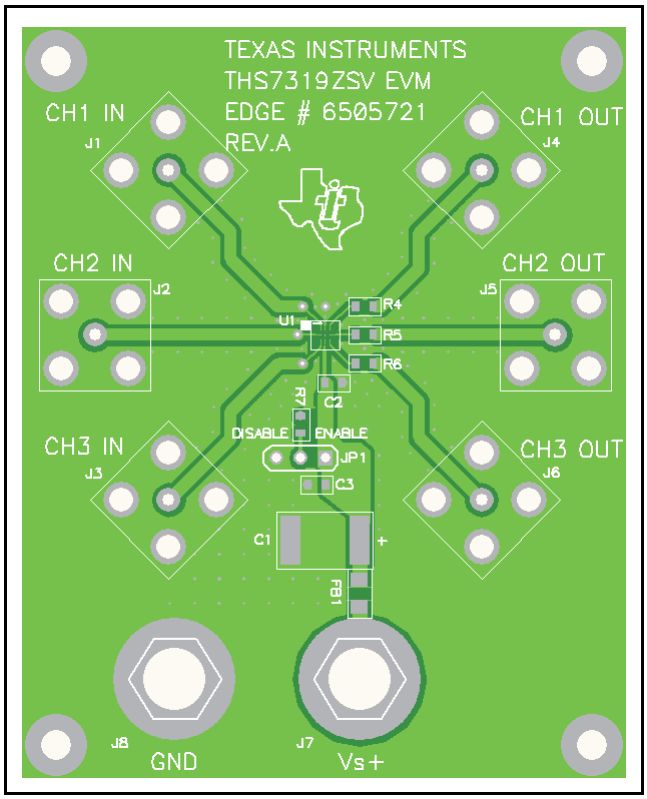


Figure 58. THS7319 EVM PCB Top Layer

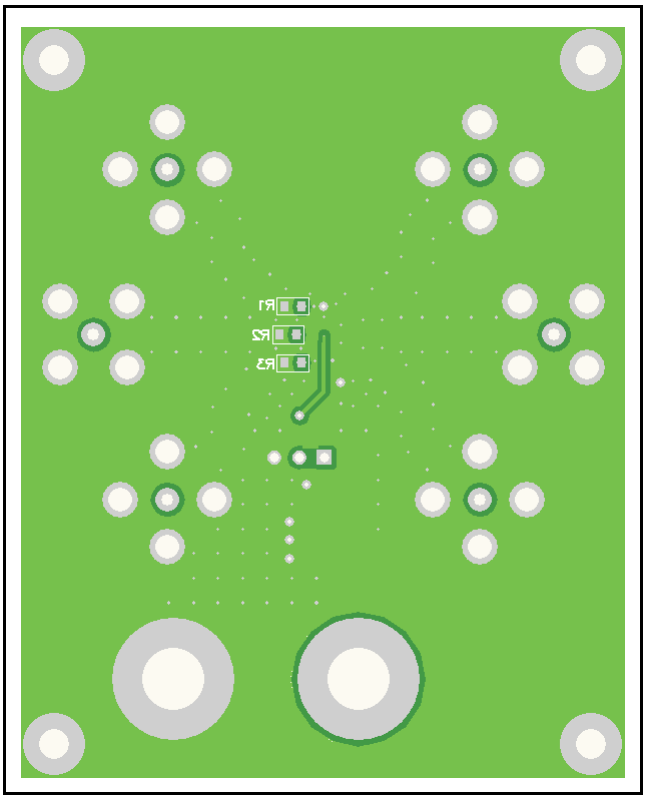


Figure 59. THS7319 EVM PCB Bottom Layer

THS7319EVM Bill of Materials

Table 5. THS7319 EVM

ITEM	REF DES	QTY	DESCRIPTION	SMD SIZE	MANUFACTURER PART NUMBER	DISTRIBUTOR PART NUMBER
1	FB1	1	Bead, Ferrite, 2.5 A, 330 Ω	0805	(TDK) MPZ2012S331A	(Digi-Key) 445-1569-1-ND
2	C1	1	Capacitor, 100 µF, Tantalum, 10 V, 10%, Low-ESR	D	(AVX) TPSD107K010R0100	(Garrett) TPSD107K010R0100
3	C2, C3	2	Capacitor, 0.01 µF, Ceramic, 16 V, X7R, 10%	0603	(AVX) 0603YC104KAT2A	(Garrett) 0603YC104KAT2A
4	R1-R6	6	Resistor, 75 Ω, 1/10 W, 1%	0603	(ROHM) MCR03EZPFX75R0	(Digi-Key) RHM75.0HCT-ND
5	R7	1	Resistor, 1 kΩ, 1/10 W, 1%	0603	(ROHM) MCR03EZPFX1001	(Digi-Key) RHM1.00KHCT-ND
6	J7, J8	2	Jack, Banana Receptance, 0.25" dia. hole		(SPC) 813	(Newark) 39N867
7	J1-J6	6	Connector, BNC, Jack, 75 Ω		(Amphenol) 31-5329-72RFX	(Newark) 93F7554
8	JP1	1	Header, 0.1" CTRS, 0.025" sq. pins	3 possible	(Sullins) PBC36SAAN	(Digi-Key) S1011E-36-ND
9	JP1	1	Shunts		(Sullins) SSC02SYAN	(Digi-Key) S9002-ND
10	U1	1	IC, THS7319	ZSV	(TI) THS7319ZSV	
11		4	Standoff, 4-40 HEX, 0.625" length		(Keystone) 1808	(Digi-Key) 1808K-ND
12		4	Screw, Phillips, 4-40, 0.250"		(BF) PMS 440 0031 PH	(Digi-Key) H343-ND
13		1	Printed Circuit Board		(TI) Edge# 6505721 Rev. A	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2009) to Revision A	Page
• Changed last Features bullet	1
• Changed last sentence of Description	1
• Changed last bullet of *Application Information* section	16
• Added *Printed Wiring Board (PWB) Design Guide* section	23

EVALUATION BOARD/KIT IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.5 V to 5.5 V and the output voltage range of 0 V to 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS7319IZSVR	ACTIVE	uCSP	ZSV	9	2500	Green (RoHS & no Sb/Br)	SN98.5/AG1/CU0.5	Level-2-260C-1 YEAR	-40 to 85	NXN	Samples
THS7319IZSVT	ACTIVE	uCSP	ZSV	9	250	Green (RoHS & no Sb/Br)	SN98.5/AG1/CU0.5	Level-2-260C-1 YEAR	-40 to 85	NXN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

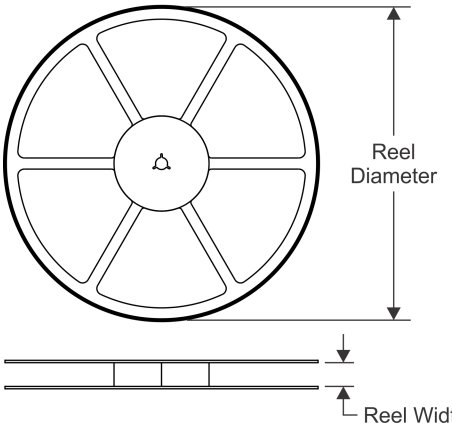
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

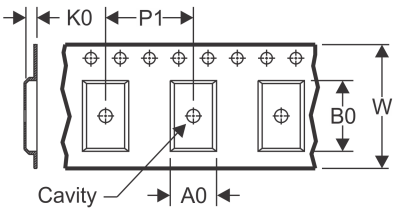
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

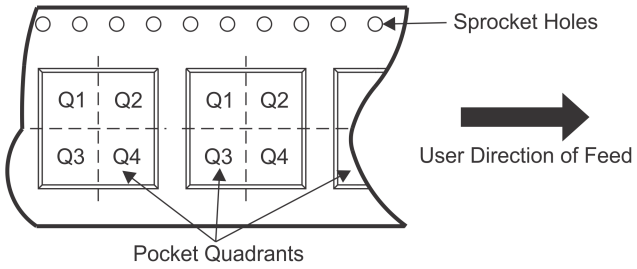


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

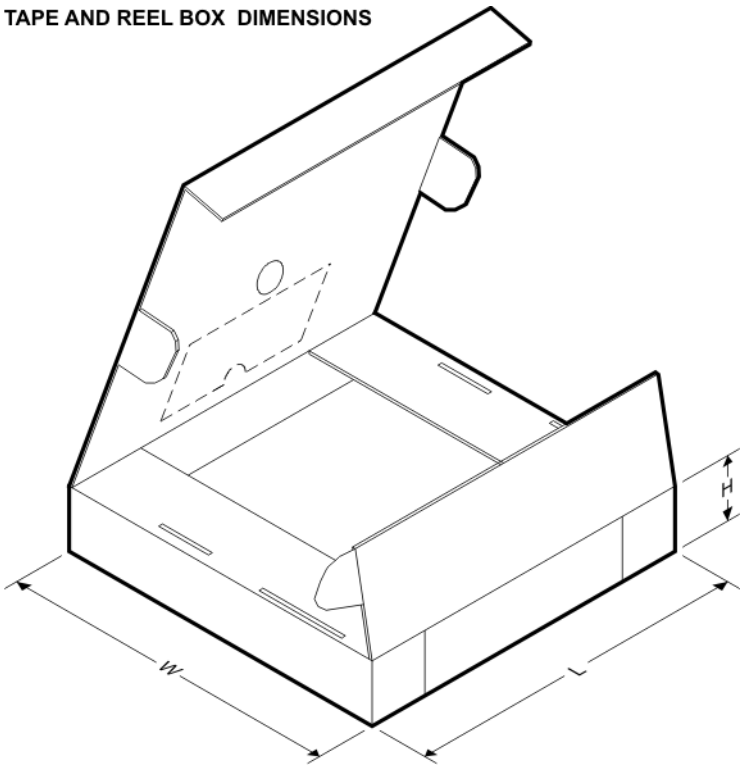
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS7319IZSVR	uCSP	ZSV	9	2500	330.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1
THS7319IZSVT	uCSP	ZSV	9	250	180.0	8.4	1.7	1.7	0.76	4.0	8.0	Q1

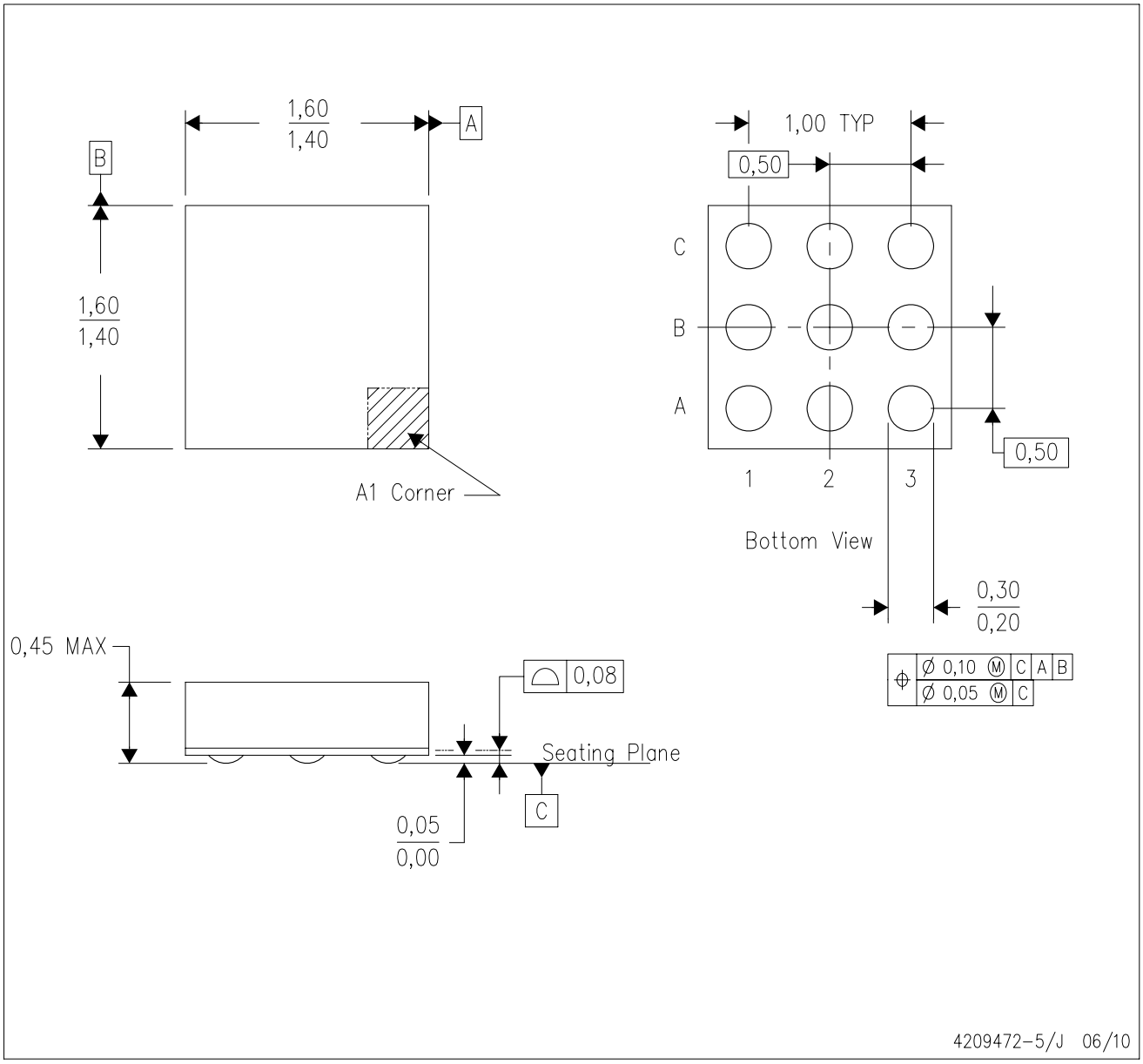
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS7319IZSVR	uCSP	ZSV	9	2500	336.6	336.6	28.6
THS7319IZSVT	uCSP	ZSV	9	250	210.0	185.0	35.0

ZSV (S–uCSP–N9) MicrostarCSP™



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. MicrostarCSP™ configuration.
D. This is a PB–free solder ball design.

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